Course Title: Computer Architecture

Course no: CSC-201

Credit hours: 3 Full Marks: 80+20
Nature of course: Theory (3 Hrs.) Pass Marks: 32+8

Course Synopsis: This course gives the fundamental knowledge concern with the way the hardware components are connected together to form a computer system and how they interact to provide the processing needs of the user.

Goals:

- Introduces the fundamental concepts behind the design working and organization of a computer system.
- Instruction set architecture, memory hierarchies and interconnection.

Unit	Topics	Hrs.
1.	**Data Representation**	**(5)**
	• Data Representation ➢ Data Types- number systems, alphanumeric representation, complements (r's and r-1's)	1.5
	• Fixed Point Representation ➢ Integer Representation ➢ Arithmetic addition, subtraction, overflows. ➢ Decimal fixed point representation	1
	• Floating Point Representation	1
	• Binary and Decimal Codes ➢ Gray, BCD, ASSCII ,Excess-3	1
	• Error Detection code ➢ Parity bit, parity checker and parity generator	0.5
2.	**Micro operations**	**(5)**
	• Arithmetic Micro operations ➢ Add micro operation, subtract micro operation ➢ Binary adder, binary subtractor, binary adder-subtractor, binary incrementor ➢ Arithmetic circuit	2
	• Logic Micro operations ➢ Logic microoperations ➢ Implementations and application	1
	• Shift Microoperations	

	➢ Logical shift, circular shift, arithmetic shift. ➢ Combinational circuit shifter • Arithmetic Logic Shift Unit	1 1
3.	**Fundamental of Computer Organization and Design** • Computer Register ➢ Registers for the basic computer and common bus system • Computer Instructions ➢ Instruction format, basic instructions, instruction set completeness, types of instructions (memory reference, register reference, i/o) • Instruction Cycle ➢ Phases of instruction cycle ➢ Fetch & decodes ➢ Flowchart for instruction cycle • Input and Output and Interrupt ➢ i/o configuration, Input-output instruction ➢ Types of interrupt, Program Interrupt, interrupt cycle • Basic computer Design and Accumulator Logic ➢ Basic Hardware components ➢ Flowchart for computer operations ➢ Control logic gates ➢ Control of registers and memory ➢ Control of common bus ➢ Control of Flip flop ➢ Design of accumulator logic (control of AC register, Adder and logic circuit)	**(7)** 1 1.5 1 1.5 2
4.	**Control Unit** • Control Memory ➢ Control word, control memory, stored program organization • Hardwired control ➢ Introduction, Timing and Control, Control unit of basic computer, timing signal • Micro programmed Control ➢ Microprogram control organization ➢ Address Sequencing ❖ Introduction, conditional branching, Mapping of instruction, subroutines	**(5)** 1 1 3

	➢ Microprograms ❖ Microinstruction and microoperation format, Symbolic Microinstructions, Symbolic microprogram, Binary microprogram ➢ Design of Control Unit ❖ F Field decoding, Microprogram sequencer	
5.	**Central Processing Unit**	**(6)**
	• Register Organization ➢ Bus System and CPU, Control word, ALU and Microoperation for CPU	0.5
	• Register Stack and memory Stack ➢ LIFO and Stack Pointer, Register Stack, Memory Stack	1
	• One address and two address instruction ➢ Instruction Format, One address instruction, two address instruction, three address instruction and zero address instruction	1.5
	• Addressing Modes ➢ Introduction, Implied Mode, Immediate Mode, Register Mode, Register Indirect Mode, autoincrement/autodecrement Mode, Direct Address Mode, Indirect Address Mode, Relative Address Mode, Indexed Addressing ModeBase Register Addressing Mode	1
	• Data transfer and Manipulation ➢ Basic Operations ➢ Data Transfer Instructions ➢ Data Manipulation Instructions ❖ Types, Arithmetic Instructions, Logical and Bit Manipulation Instruction, Shift Instruction	1
	• Introduction to RISC and CISC ➢ Introduction to RISC and CISC, Characteristics of RISC and CISC, Overlapped Register Window	1
6.	**Fixed point Computer Arithmetic**	**(5)**
	• Addition and Subtraction ➢ Introduction, Addition and subtraction with signed magnitude, Hardware Implementation, Hardware Algorithm ➢ Addition and subtraction with signed 2's complement	1.5
	• Multiplication ➢ Introduction, Hardware Implementation and Algorithm, Booth	2

	Algorithm, Array Multiplier • Division Algorithm ➢ Introduction, Hardware Implementation, Overflow, Hardware Algorithm, Restoring method, Comparision and nonrestoring Method.	 1.5
7.	**Input and Output Organization** • Introduction to Peripheral Devices ➢ I/O subsystem and peripherals • I/O interface ➢ Interface, I/O bus and interface module, Types of I/O Commands ➢ I/O and Memory bus, Isolated I/o, Memory Mapped I/O, I/O interface Unit • Direct Memory Access (DMA) ➢ Types of I/O, DMA, DMA Transfer • I/O Processor ➢ I/O Processing, CPU-IOP Communication • Data communication processor ➢ Serial and parallel Communication, data communication processor, Modes of data transfer, Protocol	**(6)** 0.5 1.5 1.5 1.0 1.5
8.	**Memory Organization** • Hierarchy of Memory System ➢ Types of Memory, Sequential, Random, Memory Hierarchy • Primary and Secondary Memory ➢ Primary memory-RAM, ROM, Bootstrap Loader, RAM and ROM Chips, Memory Address Map, Memory-CPU connection ➢ Auxiliary Memory-Types, Magnetic (Tape, Disk), Optical, Semiconductor • Virtual Memory ➢ Introduction, Address space, Memory space, Address Mapping using Pages, Associative Page Table , Page Replacement • Memory Management hardware ➢ Introduction, Segmented Page Mapping, Memory Protection	**(6)** 1 1.5 2.5 1

Text Books: M. Morris Mano, **Computer System Architecture**

References:

M. Morris Mano "Digital Design", Pearson Education, Third Edition

M. Morris Mano "Logic and Computer Design Fundamentals, Pearson Education, 2nd Edition Updated.

Members:

Name	Address	Signature
Dr. Subarna Shakya	Expert/Coordinator	
Hari Khadka	Patan Campus	
Bhoj Raj Ghimire	Amrit Science Campus A.	
N. Mishra	St. Xavier College	
Pratima Karki	Kathford College	

BCSIT—Third Semester Course Title: Computer Architecture
Course no: CSC-201

Full Marks: 80 **Pass Marks: 32**

Long Answer Questions

Attempt any two questions. **2 x 10=20**

1. What do you understand by interrupt? Draw and explain the flow chart for interrupt cycle. 2+8
2. State and explain the different types of data manipulation instructions used in a typical computer. 10
3. Why do computers need input-output interface? Explain the sequence of operations carried out during CPU-IOP Communication with the help of suitable flow chart. 3+7

Short Answer Questions

Attempt any ten questions. **12 x 5 = 60**

1. Derive the circuit for a 3-bit parity generator and a 4-bit parity checker using even parity bit. 6
2. Explain the shift micro-operation in brief. 6
3. Explain the difference between hardwired and micro-programmed control units. Is it possible to have a hardwired control with a hardwired control associated with a control memory? 4 + 2
4. Show using the concept of addition/subtraction algorithm that adding B after the operation A + B' + 1 restores the original value of A. What should be done with the end carry? 5 + 1
5. Describe the memory mapping table in a paged system. 6
6. Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift left, followed by a circular shift, followed by a logical shift-right and a circular shift left. 1.5 + 1.5 + 1.5 + 1.5
7. In your opinion, what different hardware components are required to design a basic computer? 6
8. What are the microinstructions needed for fetch routine? Write a symbolic microprogram for the fetch routine. 3 + 3
9. Differentiate between RISC and CISC computers. 6
10. What do you understand by the memory hierarchy in a computer system? 6
11. Why does DMA have priority over CPU when both request a memory transfer? 6
12. Write short notes on the following: 3+3

    a. Alphanumeric representation b. Divide overflow