Chapter 3

Operational Amplifiers and Simple Op-Amp Circuits

3.1 Introduction

In this chapter we study the characteristics of both ideal and real operational amplifiers. Ideal operational amplifiers (op-amps) behave according to a simplified, ideal set of characteristics described in section 3.2. While analysis using ideal op-amp device characteristics often can simplify circuit design and analysis, this assumption sometimes causes unexpected results in practice, since the ideal model may not accurately represent real-world devices. In this chapter we begin by introducing the characteristics of an ideal op-amp. Second, we will consider real op-amps, pointing out specific properties where differences occur relative to the ideal op-amp assumptions. For instance, we will learn that real op-amps do not have infinite gain, do not amplify all frequencies by a constant K, do not have infinite input impedance, do not have zero output impedance, and do not necessarily operate in a linear fashion, as do our simple ideal op-amps! In following chapters we will usually assume ideal op-amp characteristics (as do most analog design texts) for our filter designs. However, in a few applications the effects of non-ideal characteristics will be discussed in detail to highlight exactly how the use of real op-amps alters the characteristics of the designed filter.

Since op-amps will be an integral part of our active filter designs in later chapters, we must learn about some simple amplifier circuits. We will use these building blocks and analysis methods as foundations for discussions in later chapters when we implement more complex filter transfer functions.

3.2 Ideal Op-Amps and DC Circuits

An ideal op-amp is a differential amplifier with infinite voltage gain, infinite input impedance, and zero output impedance. By differential amplifier we mean a device whose voltage output is proportional to the difference between two input voltages as shown in Figure 3.1. The two inputs are referred to as the '+' (or non-inverting) input and the '-' (or inverting) input.

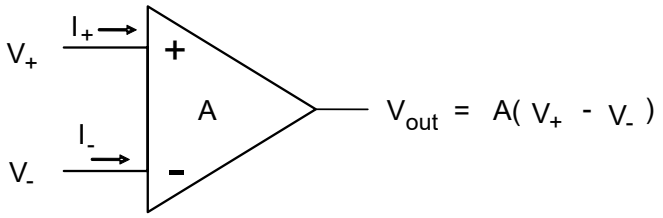


Figure 3.1. Ideal op-amp.

In an ideal op-amp the voltage gain A is very large, and may be considered almost infinite. As we will soon observe, for circuits connected in a particular manner, this implies that the differential voltage (V_+ minus V_-) is virtually zero, or that there is a 'virtual short' between the two input terminals. The assumption of infinite input impedance simplifies circuit design and analysis by allowing us to assume that the current into either input (I_+ or I_-) is zero. Zero output impedance implies the output voltage is independent of the output current. (Note that at first glance the circuit may appear to violate Kirchhoff's Current Law because current can flow through the output with no current in either input. What we have omitted in Figure 3.1 are the connections to the DC supply, supplying $\pm V_{cc}$ to our device.)

One final restriction is that the op-amp output voltage cannot exceed $\pm V_{cc}$. (If we attempt to exceed $\pm V_{cc}$ the output waveform becomes "clipped" so that the maximum magnitude is roughly $|V_{cc}|$.) A handy list of these ideal op-amp assumptions is provided in Table 3.1. To further understand these concepts we will consider several simple examples.

Table 3.1. Ideal op-amp assumptions.

$A \cong \infty$
$Z_{in} \cong \infty$
$Z_{out} \cong 0$
$V_+ \cong V_-$
$I_+ \cong I_- \cong 0$
$\lvert V_{out} \rvert \leq \lvert V_{cc} \rvert$

Example 3.1 Voltage Follower

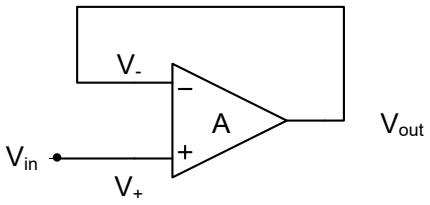


Figure 3.2. Voltage follower circuit.

In the circuit shown in Figure 3.2,

$$V_{out} = A(V_+ - V_-) = A(V_{in} - V_{out}) \tag{3.1}$$

or

$$V_{out} = \frac{A}{1+A} V_{in}$$

$$\cong V_{in} \tag{3.2}$$

as A tends to infinity. A typical value of gain (A) at low frequencies might be 10^5, therefore the gain of the voltage follower would be within one part in 10^5 of unity. Although a circuit with the output equal to the input may not appear to be useful, in fact such a circuit is particularly useful in that it is able to "drive" (supply current to) a load without drawing current from the input. (Recall that the op-amp itself has nearly infinite input impedance.)

Since the output is the differential input times the gain, it follows that the differential input is the output divided by the gain, or virtually zero for large gain and finite output voltage. This is true for all stable circuits (assuming ideal op-amps). We will examine the question of stability more completely later in section 3.5 where we consider real op-amps. For now let us focus on the important concept of negative feedback.

By connecting the output back to the inverting (-) input, any increase in output voltage (V_{out}) results in a decrease to the differential input voltage ($V_+ - V_- = V_{in} - V_{out}$), and hence a decrease in output voltage. Therefore the output shifts or "slews" until the differential input voltage becomes very small. (By way of analogy, one feedback signal to an automobile cruise control system would be an error signal which is the difference between *actual* speed and *desired* speed. If actual speed minus desired speed is a positive number, that information must be fed back to the control system in some way so as to supply a control input to *reduce* the vehicle speed. This corrective action can be thought of as negative feedback.) Had we connected the output to the non-inverting (+) input (positive feedback), a positive change in output voltage would have resulted in a positive change in differential input voltage and hence an even more positive output voltage, theoretically tending to infinity. In practice the output would slew until it approached the power supply voltage V_{cc}. (Again by way of analogy for our automobile cruise control, if *actual* speed minus *desired* speed is a positive number, and if that information is fed back and used as a control input to increase the vehicle speed, that is called positive feedback. Naturally most successful control systems implement negative feedback!) In the case where the circuit output slews until it approaches the power supply voltage V_{cc}, the differential input voltage would in general be non-zero. Such circuits do have practical uses as Schmitt triggers, voltage comparators, and oscillators, but these applications are non-linear and outside the scope of this linear text.

Example 3.2 Non-Inverting Amplifier

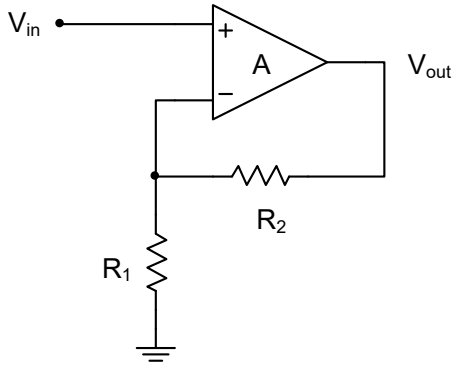


Figure 3.3. Non-inverting amplifier.

In order to analyze the circuit in Figure 3.3, we employ the concept of voltage division to obtain V_- (since essentially zero current enters the inverting terminal). This means

$$V_- = \left(\frac{R_1}{R_1 + R_2}\right) V_{out} \cdot \tag{3.3}$$

Then

$$V_{out} = A(V_+ - V_-) = A\left(V_{in} - \left(\frac{R_1}{R_1 + R_2}\right)V_{out}\right),$$

so

$$V_{out} = \frac{A}{1 + \left(\frac{R_1}{R_1 + R_2}\right)A} V_{in}$$

$$\cong \left(1+\frac{R_2}{R_1}\right)V_{in} \tag{3.4}$$

as A tends to infinity. A second (simpler) method of analyzing the circuit in Figure 3.3 is to assume that due to the negative feedback, the differential input voltage is zero (i.e., a virtual short). Now

$$V_{in} = V_+ = V_- = \left(\frac{R_1}{R_1+R_2}\right)V_{out}\,. \tag{3.5}$$

Hence for a non-inverting amplifier configuration, the gain is given by

$$\boxed{\frac{V_{out}}{V_{in}} = \left(1+\frac{R_2}{R_1}\right)} \tag{3.6}$$

Example 3.3 Inverting Amplifier

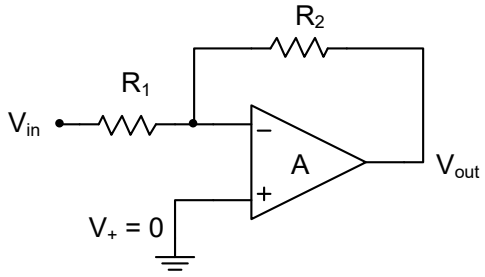


Figure 3.4. Inverting amplifier.

In this case we will assume $V_+ = V_-$, and since V_+ is grounded, we call V_- a "virtual ground." We now write a node voltage equation for the inverting input, setting the sum of currents equal to zero. (The assumption of infinite input impedance for the device itself results in no current entering the inverting terminal.) Therefore,

$$\frac{V_{in}}{R_1} + \frac{V_{out}}{R_2} = 0 \tag{3.7}$$

so the gain for the inverting amplifier configuration is given by

$$\boxed{\frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}} \tag{3.8}$$

Example 3.4 Analog Summer

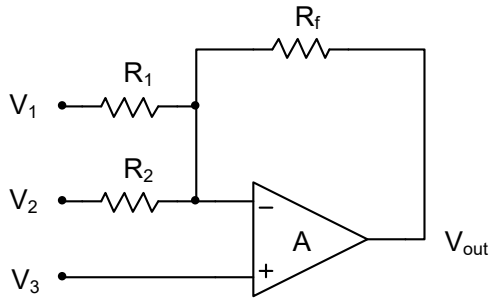


Figure 3.5. Analog summer.

In this example we will incorporate superposition and the results of the previous examples to analyze a slightly more complicated circuit. Superposition states that the output of a multiple input linear system is equal to the sum of the outputs due to each input (with all other inputs set to zero.) That is, the output due to several inputs is just the sum of the individual outputs! For this example

$$V_{out} = k_1 V_1 + k_2 V_2 + k_3 V_3 , \tag{3.9}$$

where

$$k_1 = \left.\frac{V_{out}}{V_1}\right|_{V_2, V_3 = 0} ,$$

$$k_2 = \left.\frac{V_{out}}{V_2}\right|_{V_1, V_3 = 0} ,$$

and

$$k_3 = \left.\frac{V_{out}}{V_3}\right|_{V_1, V_2 = 0} . \tag{3.10}$$

In order to ensure that V_2 and V_3 are in fact at zero potential, we will ground them. Observe that if we ground V_2 and V_3, our circuit is exactly that of the previous example. The resistor R_2 carries no current as both ends are at ground potential, one virtual and one physical (Figure 3.5a). (We can therefore eliminate resistor R_2.)

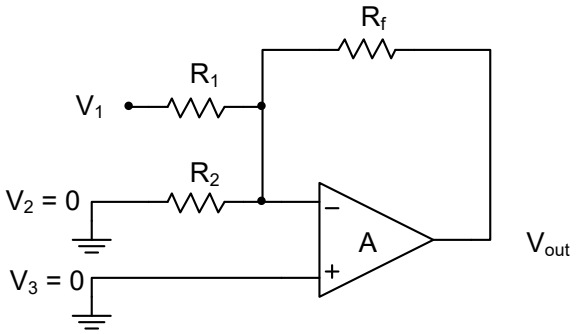


Figure 3.5a. Summer from Figure 3.5 with V_2 and V_3 deactivated.

Therefore

$$\boxed{k_1 = -\frac{R_f}{R_1}}. \tag{3.11}$$

Similarly, if we deactivate (ground) V_1 and V_3,

$$\boxed{k_2 = -\frac{R_f}{R_2}}. \tag{3.12}$$

If we ground V_1 and V_2 (Figure 3.5b), our circuit is exactly that of the non-inverting amplifier example (Figure 3.3).

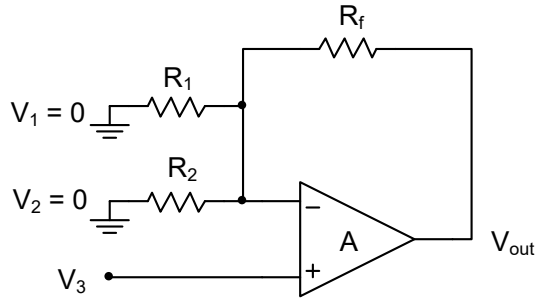


Figure 3.5b. Summer from Figure 3.5 with V_1 and V_2 deactivated.

The resistance between the inverting terminal and ground is now the parallel combination of R_1 and R_2 (called R_{12}), and

$$\boxed{k_3 = 1 + \frac{R_f}{R_{12}}} \tag{3.13}$$

where

$$R_{12} = \frac{R_1 R_2}{R_1 + R_2}. \tag{3.14}$$

Finally

$$\boxed{V_{out} = -\frac{R_f}{R_1} V_1 - \frac{R_f}{R_2} V_2 + \left(1 + \frac{R_f}{R_{12}}\right) V_3}. \tag{3.15}$$

3.3 Circuits for Synthesizing Real Poles and Zeros

Inverting circuits to implement transfer functions with real poles and zeros can be represented in general as shown in Figure 3.6.

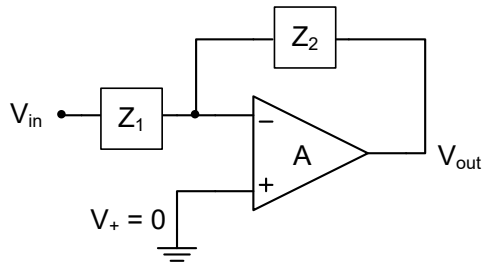


Figure 3.6. General inverting amplifier configuration for synthesizing real poles and zeros.

This circuit can be analyzed exactly as that in Figure 3.4 by replacing the real resistances (R's) with the complex impedances (Z's).

$$\frac{V_{in}}{Z_1} + \frac{V_{out}}{Z_2} = 0 \tag{3.16}$$

or

$$V_{out} = -\frac{Z_2}{Z_1} V_{in} \tag{3.17}$$

where the ratio $-\frac{Z_2}{Z_1}$ is now a function of the Laplace transform variable "s" (or complex frequency), and the ratio is the *transfer function* of the circuit. (By *transfer function*, we mean that function which "transfers" the input to the output. In this case, the input V_{in} is multiplied by the function $-\frac{Z_2}{Z_1}$ to produce the output V_{out}.) Since the impedance (Z) is the reciprocal of the admittance (Y), the transfer function can also be written

$$\frac{V_{out}}{V_{in}} = -\frac{Y_1}{Y_2}, \tag{3.18}$$

$$= -\frac{1}{Z_1 Y_2}, \tag{3.19}$$

or

$$= -Z_2 Y_1 . \tag{3.20}$$

While all these expressions are correct, component configuration (series or parallel connection) will dictate which is easiest to use. (Recall that admittances add in parallel and impedances add in series.)

Example 3.5 Ideal Integrator

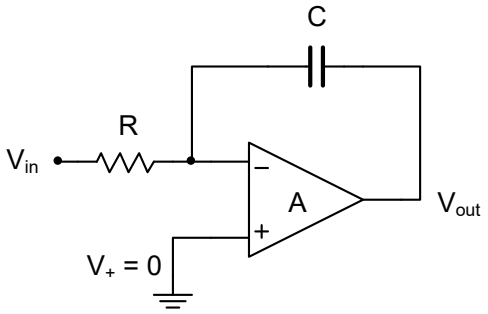


Figure 3.7. Ideal integrator circuit.

Using 3.19 the transfer function is

$$\frac{V_{out}}{V_{in}} = -\frac{1}{Z_1 Y_2} = -\frac{1}{RCs}. \tag{3.21}$$

The Bode magnitude plot is shown in Figure 3.8.

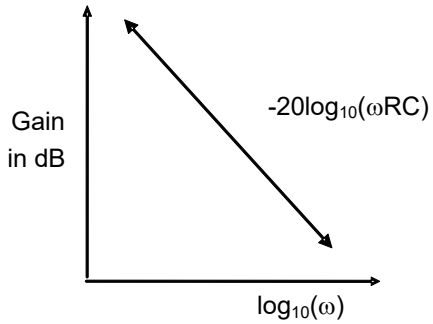


Figure 3.8. Bode magnitude plot for the ideal integrator.

If we prefer to think about the circuit in the time domain, we know that the voltage across a capacitor is

$$V_c(t) = \frac{q_c(t)}{C} = \frac{1}{C}\int_{-\infty}^{t} i_c(\tau)d\tau, \tag{3.22}$$

where $q_c(t)$ represents the capacitor charge in Coulombs as a function of time. If we define the output as the "plus" side the of the capacitor, the negative side of the capacitor (connected to the inverting op-amp input in Figure 3.7) is virtual ground, and

$$V_{out}(t) = V_c(t), \tag{3.23}$$

$$i_c(t) = -\frac{V_{in}(t)}{R}, \tag{3.24}$$

and

$$V_{out}(t) = -\frac{1}{RC}\int_{-\infty}^{t} V_{in}(\tau)\, d\tau \,. \qquad (3.25)$$

Hence the circuit output is a negative constant times the integral of the input, thereby producing our "integrator." (As a matter of interest, this circuit, together with summing amplifiers, forms the basic building blocks for analog computers that could be used to simulate or synthesize a system characterized by linear differential equations!)

One final practical note we should make is that the circuit in this example (Figure 3.7), when implemented using real op-amps without additional negative feedback, is not stable. It will slew (drive) to a limiting voltage and remain there due to voltage offsets associated with the real op-amp, and the lack of a DC negative feedback path. In the following section on biquad filters we will use integrators as building blocks in a more complicated circuit with a DC negative feedback path. If one wants to integrate signals (without DC components), a practical method is to use the low-pass filter in Example 3.7. In that case one can use a large feedback resistor and capacitor to set the filter break frequency to a value much less than the smallest significant frequency of the incoming signal. This will result in the magnitude response behaving similar to Figure 3.8 over the frequency range of interest.

Example 3.6 Differentiator

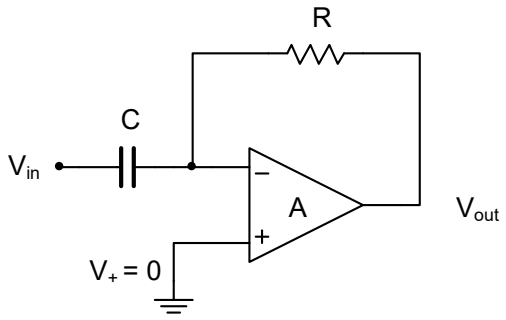


Figure 3.9. Ideal differentiator circuit.

Using 3.20

$$\frac{V_{out}}{V_{in}} = -Z_2 Y_1$$

$$= -RCs \qquad (3.26)$$

The Bode magnitude plot is shown in Figure 3.10.

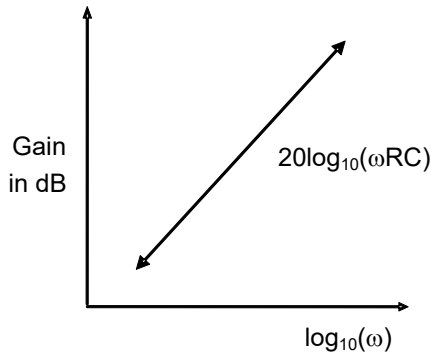


Figure 3.10. Bode magnitude plot for differentiator.

As with the case of the integrator, we can analyze this circuit in the time domain. The node equation at the inverting terminal is

$$C\ \frac{dV_{in}(t)}{dt} + \frac{V_{out}(t)}{R} = 0\ . \qquad (3.27)$$

Solving for $v_{out}(t)$ we obtain

$$V_{out}(t) = -RC\ \frac{dV_{in}(t)}{dt}, \qquad (3.28)$$

where the output is a negative constant times the derivative of the input voltage, thereby producing our differentiator.

Example 3.7 Low-pass Filter

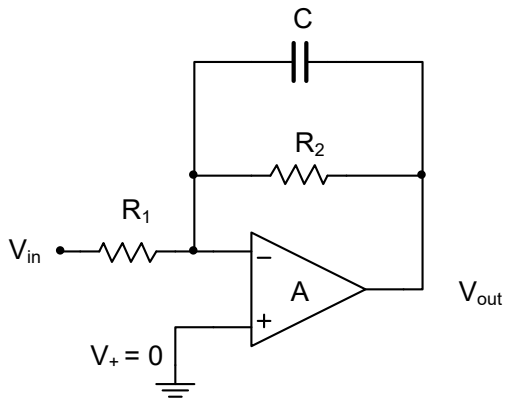


Figure 3.11. Low-pass filter circuit.

Solving for our transfer function $\frac{V_{out}}{V_{in}}$ we obtain

$$\frac{V_{out}}{V_{in}} = -\frac{1}{Z_1 Y_2} = -\frac{1}{R_1\left(\frac{1}{R_2}+Cs\right)} = -\frac{\frac{1}{R_1 C}}{s+\frac{1}{R_2 C}}, \tag{3.29}$$

or a first order low-pass filter with a DC gain of $-\frac{R_2}{R_1}$ and a break frequency of $\frac{1}{R_2 C}$ rad/sec. The Bode magnitude plot is shown in Figure 3.12. At frequencies below the break frequency, the admittance of R_2 is greater than that of C, the parallel combination looks like R_2, and the circuit looks like the inverting amplifier in Example 3.3. At frequencies above the break frequency the admittance of C is greater than that of R_2, the parallel combination looks like C, and the frequency response looks much like that of the integrator in Example 3.5.

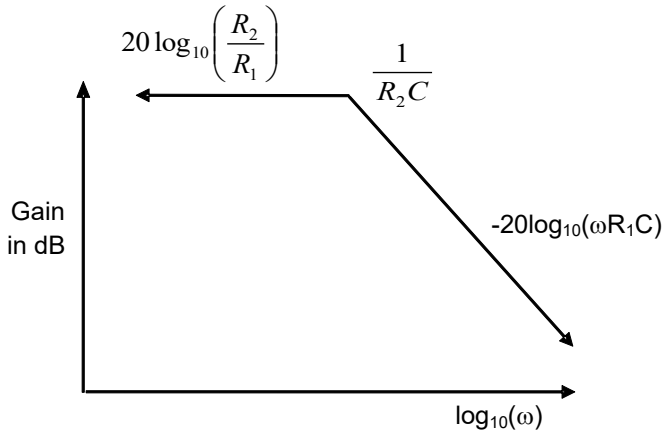


Figure 3.12. Bode magnitude plot for low-pass filter.

Example 3.8 High-pass Filter

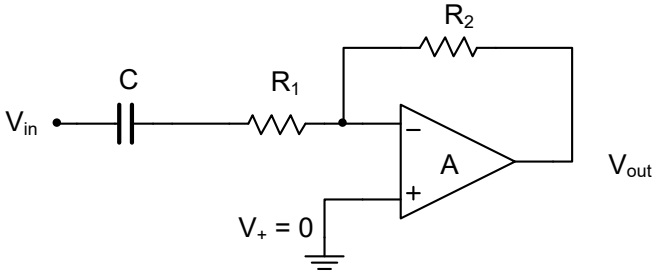


Figure 3.13. High-pass filter circuit.

From 3.17 the transfer function of the high-pass filter shown in Figure 3.13 is

$$\frac{V_{out}}{V_{in}} = -\frac{Z_2}{Z_1} = -\frac{R_2}{R_1 + \frac{1}{sC_1}} = -\frac{\frac{R_2}{R_1}\, s}{s + \frac{1}{R_1 C_1}}, \qquad (3.30)$$

or a first order high-pass filter with a break frequency of $\frac{1}{R_1 C_1}$ rad/sec and a high frequency gain of $-\frac{R_2}{R_1}$. The Bode magnitude plot is shown in Figure 3.14.

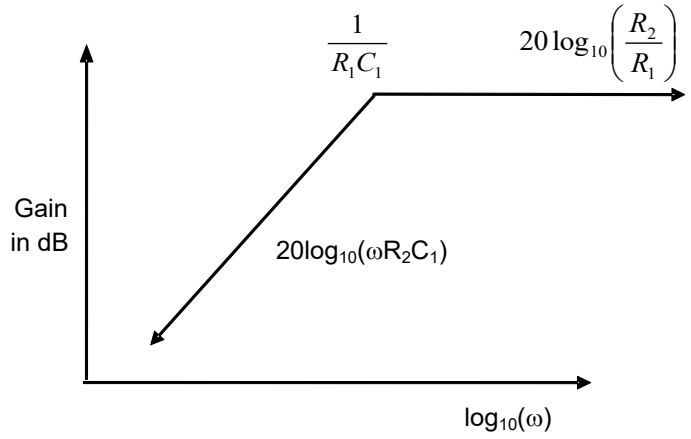


Figure 3.14. Bode magnitude plot for high-pass filter.

At low frequencies ($<\frac{1}{R_1 C_1}$) the impedance of C_1 dominates the impedance of R_1 and the circuit looks like the differentiator of Example 3.6. At frequencies above $\frac{1}{R_1 C_1}$, R_1 dominates and the circuit looks like the inverting amplifier of Example 3.3.

Example 3.9 Band-pass Filter

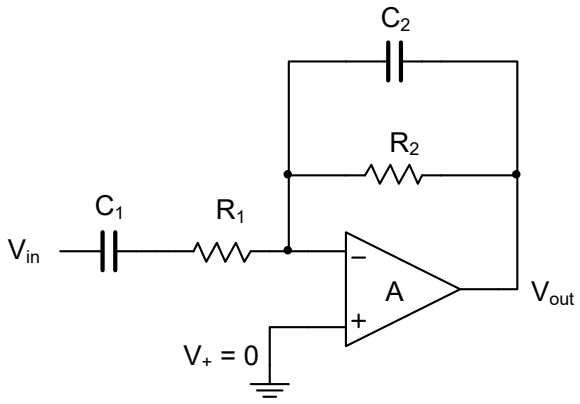


Figure 3.15a. Band-pass filter circuit.

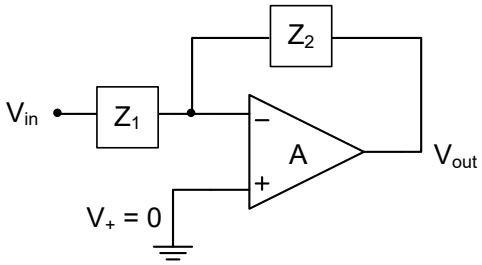


Figure 3.15b. Block diagram for Figure 3.15a, band-pass filter.

Using 3.19 the transfer function is,

$$\frac{V_{out}}{V_{in}} = -\frac{1}{Z_1 Y_2}$$

$$= -\frac{1}{\left(R_1 + \frac{1}{sC_1}\right)\left(\frac{1}{R_2} + C_2 s\right)}$$

$$= -\frac{\frac{1}{R_1 C_2} s}{\left(s + \frac{1}{R_1 C_1}\right)\left(s + \frac{1}{R_2 C_2}\right)}$$

$$= -\frac{\frac{1}{R_1 C_2} s}{s^2 + \left(\frac{1}{R_2 C_2} + \frac{1}{R_1 C_1}\right) s + \frac{1}{R_1 C_1 R_2 C_2}} \quad . \tag{3.31}$$

The circuit can be viewed as the cascade of a high-pass filter and a low-pass filter. The high-pass filter is the transfer function from the input voltage to the input current, $\left(\frac{1}{Z_1}\right)$ and has a break frequency of $\left(\frac{1}{R_1C_1}\right)$ rad/sec. The low-pass filter is the transfer function from input current to the output voltage $\left(-\frac{1}{Y_2}\right)$ and has a break frequency of $\left(\frac{1}{R_2C_2}\right)$ rad/sec. At low frequencies (much less than either break frequency) the circuit looks like the differentiator of Example 3.6. At high frequencies (much greater than either break frequency) the circuit looks like the integrator of Example 3.5. What the frequency response looks like at intermediate frequencies depends on the relative magnitudes of these two break frequencies. Tables 3.2a and 3.2b summarize the behaviors for two specific cases, $\frac{1}{R_2C_2} >> \frac{1}{R_1C_1}$ and $\frac{1}{R_2C_2} << \frac{1}{R_1C_1}$, respectively. The Bode magnitude plots for these two cases are shown in Figures 3.16 and 3.17.

Table 3.2a. Summary of band-pass filter behavior, for $\frac{1}{R_2C_2} >> \frac{1}{R_1C_1}$.

Low Frequencies	Mid Frequencies	High Frequencies
$\omega << \frac{1}{R_1C_1}$	$\frac{1}{R_1C_1} << \omega << \frac{1}{R_2C_2}$	$\omega >> \frac{1}{R_2C_2}$
$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong \frac{1}{sC_1}$	$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong R_1$	$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong R_1$
$Y_2 = \frac{1}{R_2} + sC2$ $\cong \frac{1}{R_2}$	$Y_2 = \frac{1}{R_2} + sC_2$ $\cong \frac{1}{R_2}$	$Y_2 = \frac{1}{R_2} + sC_2$ $\cong sC_2$
$H(s) = -\frac{1}{Z_1Y_2}$ $\cong -C_1R_2s$	$H(s) = -\frac{1}{Z_1Y_2}$ $\cong \frac{-R_2}{R_1}$	$H(s) = -\frac{1}{Z_1Y_2}$ $\cong \frac{-1}{sC_2R_1}$

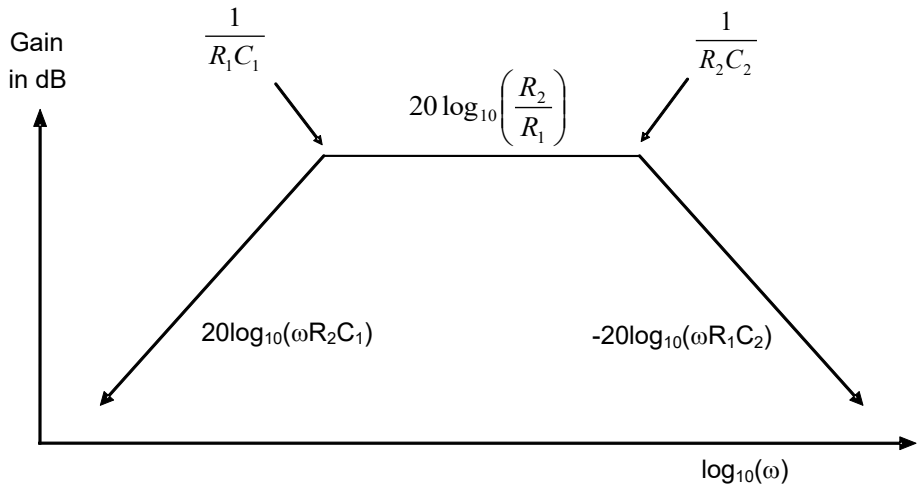


Figure 3.16. Bode magnitude plot for band-pass filter, $\frac{1}{R_2C_2} >> \frac{1}{R_1C_1}$.

Table 3.2b. Summary of band-pass filter behavior, for $\frac{1}{R_2C_2} << \frac{1}{R_1C_1}$.

Low Frequencies	Mid Frequencies	High Frequencies
$\omega << \frac{1}{R_2C_2}$	$\frac{1}{R_2C_2} << \omega << \frac{1}{R_1C_1}$	$\omega >> \frac{1}{R_1C_1}$
$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong \frac{1}{sC_1}$	$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong \frac{1}{sC_1}$	$Z_1 = R_1 + \frac{1}{sC_1}$ $\cong R_1$
$Y_2 = \frac{1}{R_2} + sC_2$ $\cong \frac{1}{R_2}$	$Y_2 = \frac{1}{R_2} + sC_2$ $\cong sC_2$	$Y_2 = \frac{1}{R_2} + sC_2$ $\cong sC_2$
$H(s) = -\frac{1}{Z_1Y_2}$ $\cong -C_1R_2s$	$H(s) = -\frac{1}{Z_1Y_2}$ $\cong \frac{-C_1}{C_2}$	$H(s) = -\frac{1}{Z_1Y_2}$ $\cong \frac{-1}{sC_2R_1}$

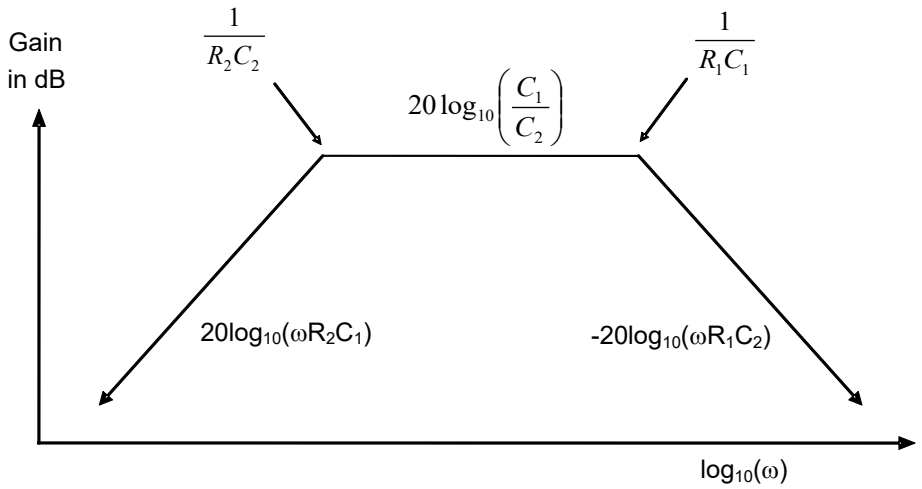


Figure 3.17. Bode magnitude plot for $\frac{1}{R_2C_2} << \frac{1}{R_1C_1}$.

If the two break frequencies are equal (meaning $\frac{1}{R_2C_2} = \frac{1}{R_1C_1}$) the high and low frequency asymptotes intersect at a point, and the actual gain (Figure 3.18) is 6 dB lower (Q = 0.5).

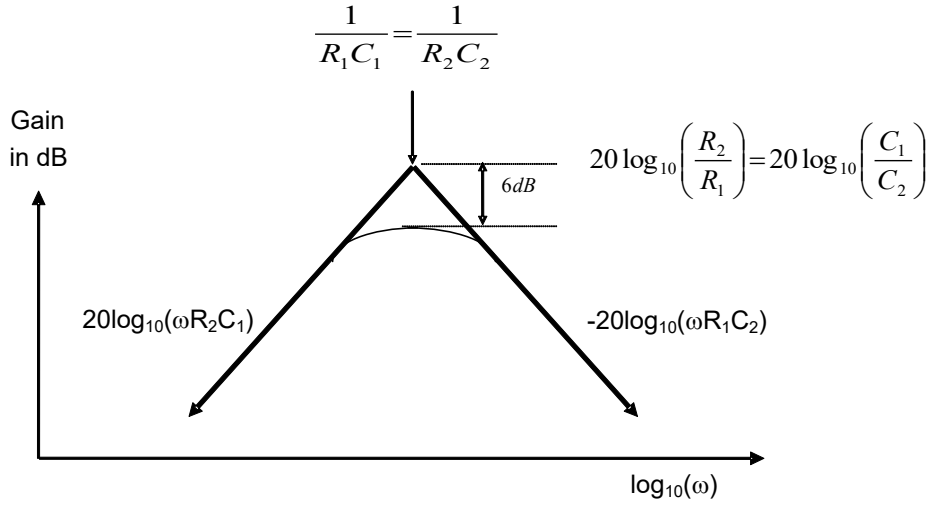


Figure 3.18. Bode magnitude plot for $\frac{1}{R_2C_2} = \frac{1}{R_1C_1}$.

Virtually all practical band-pass filters have complex poles, and thus far we have only discussed methods of synthesizing real poles and zeros. In the following section and in later chapters we will consider circuits for synthesizing complex poles.

3.4 Biquad Filters

In almost all cases the filters we will design in the following chapters will require complex poles and/or zeros. Various circuits for implementing second order low-pass, high-pass and band-pass sections with complex poles will be introduced in those chapters. In this section we will introduce a very general second order section called a *biquad* or *state variable filter*. We will analyze it by recognizing each part of it as a circuit we have already studied in this chapter, and then we will use block diagram algebra to analyze the entire circuit.

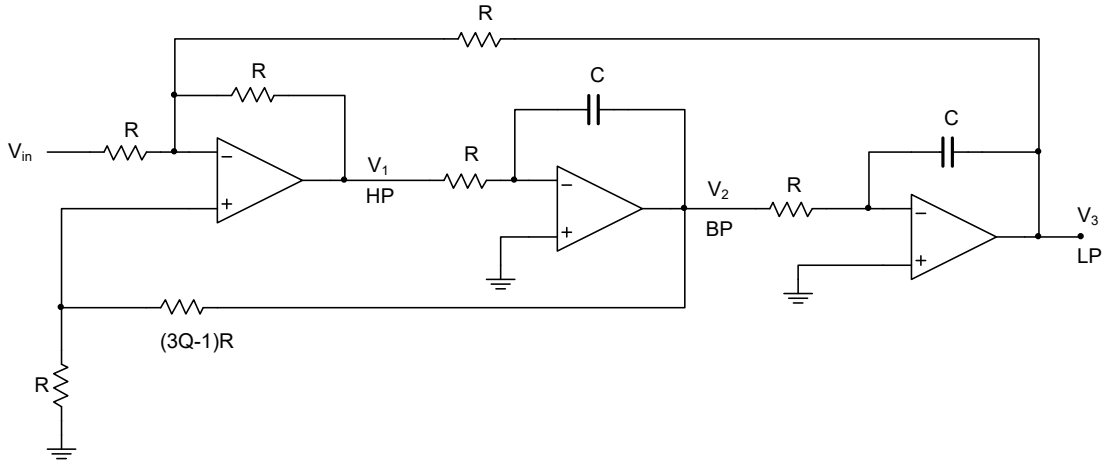


Figure 3.19. Biquad filter circuit.

The first step towards analyzing this circuit is to recognize the first op-amp as a summer (see Example 3.4 or Figure 3.5) with two inverting inputs (V_{in} and V_3) and one non-inverting input (V_2). The gain from each inverting input is -1 because the feedback resistor is the same value as the input resistors. Using superposition to determine the non-inverting gain, we ground V_{in} and V_3. The resistance between the inverting terminal and ground is R/2 and the gain from the non-inverting input (V_+) to the output (V_1) is

$$1+\frac{R}{\left(R/2\right)}=3 \tag{3.32}$$

Using voltage division, the voltage at the non-inverting terminal is

$$\left(\frac{R}{R+\left(3Q-1\right)R}\right)V_2=\frac{V_2}{3Q} \tag{3.33}$$

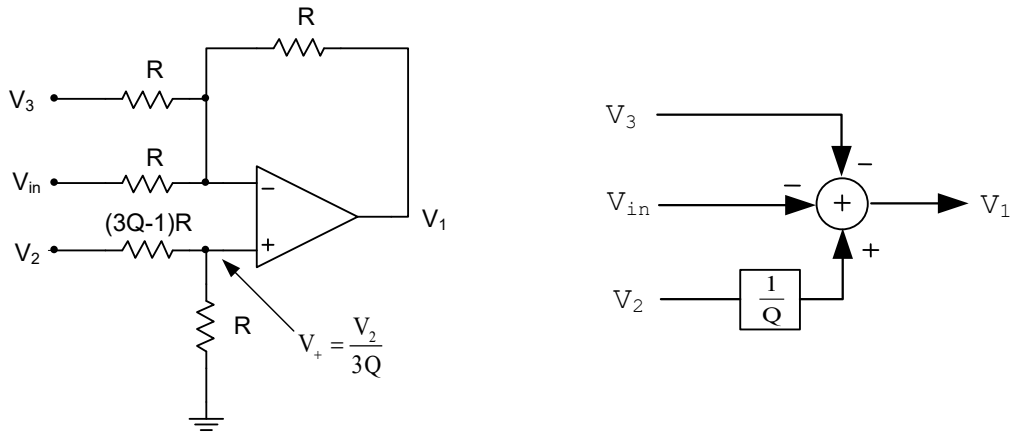


Figure 3.20. Summer section of biquad filter: Circuit (left) and block diagram (right).

As shown in Figure 3.20 (left), and recalling 3.15 (which solves for the output of an analog summer) we can find V_1 as

$$V_1 = -V_3 - V_{in} + \left(1 + \frac{R}{R \| R}\right)\left(\frac{V_2}{3Q}\right)$$

$$= -V_3 - V_{in} + \left(1 + \frac{R}{(R/2)}\right)\left(\frac{V_2}{3Q}\right)$$

or

$$V_1 = -V_3 - V_{in} + \left(\frac{V_2}{Q}\right). \qquad (3.34)$$

Figure 3.20 (right) shows the block diagram which represents 3.34. Recognize from Figure 3.21 (left) that each of the next two op-amp stages are ideal integrators (see Example 3.5 or Figure 3.7), so

$$V_2 = -\frac{1}{RCs} V_1 \qquad (3.35)$$

and

$$V_3 = -\frac{1}{RCs} V_2 . \qquad (3.36)$$

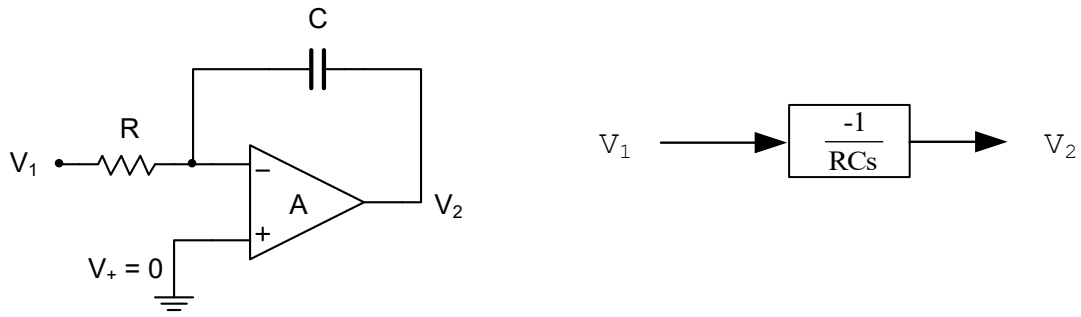


Figure 3.21. First integrator section of biquad filter: Circuit (left) and block diagram (right).

Next we define ω_o by

$$\omega_o = \frac{1}{RC}, \tag{3.37}$$

and we can reconfigure (and simplify) Figure 3.19 to the block diagrams as shown in Figure 3.22(a) and 3.22(b).

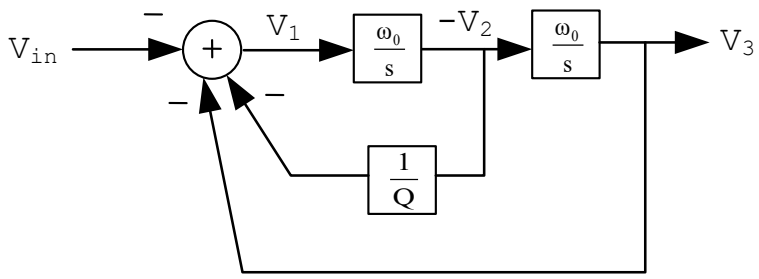


Figure 3.22a. Block diagram of biquad filter (first simplification).

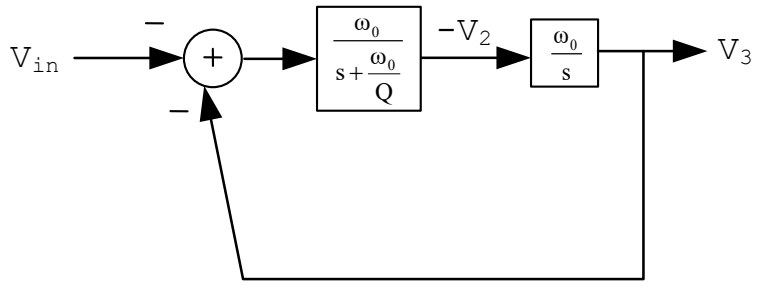


Figure 3.22b. Block diagram of biquad filter (second simplification).

Finally we note that

$$\frac{V_3}{V_{in}} = \frac{-\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} \tag{3.38}$$

or just a general second order low-pass transfer function with a DC gain of -1. Similarly using the relationships between V_1, V_2, and V_3 from 3.35 and 3.36 we obtain

$$\frac{V_2}{V_{in}} = \frac{\omega_o s}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}, \tag{3.39}$$

and

$$\frac{V_1}{V_{in}} = \frac{-s^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}. \tag{3.40}$$

The transfer functions in 3.39 and 3.40 are general second order band-pass and inverting high-pass filters respectively. By summing a linear combination of these low-pass, band-pass, and high-pass outputs, the biquad circuit of Figure 3.19 can be used to implement any second order transfer function. In Chapters 4, 5, and 6 we will study other circuits that will be more "economical" in that only a single op-amp and fewer resistors will needed for a second order section. In Chapter 7 we will return to the biquad circuit for the purpose of implementing elliptic filters.

3.5 Real Op-Amps

To study the effects of finite gain, finite input impedance, and non-zero output impedance, we look in detail at the example of a non-inverting amplifier shown in Figure 3.23. If you compare this circuit with that shown in Figure 3.3 for the non-inverting amplifier, you will note that we have replaced the pure gain A with a more general transfer function A(s).

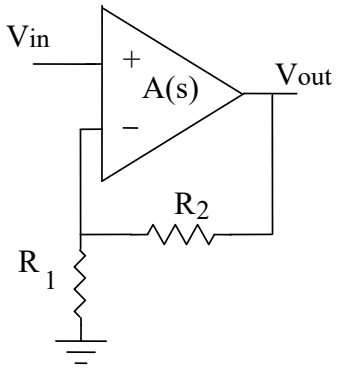


Figure 3.23. Non-inverting amplifier circuit

For our example we will use a μA741 op-amp. This op-amp is quite inexpensive and has been popular for many years. Among its typical specifications listed are:

Open Loop DC Gain	200,000
Gain Bandwidth Product	1 MHz
Output Impedance	75 Ω
Input Resistance	2 MΩ
Input Capacitance	1.4 pF

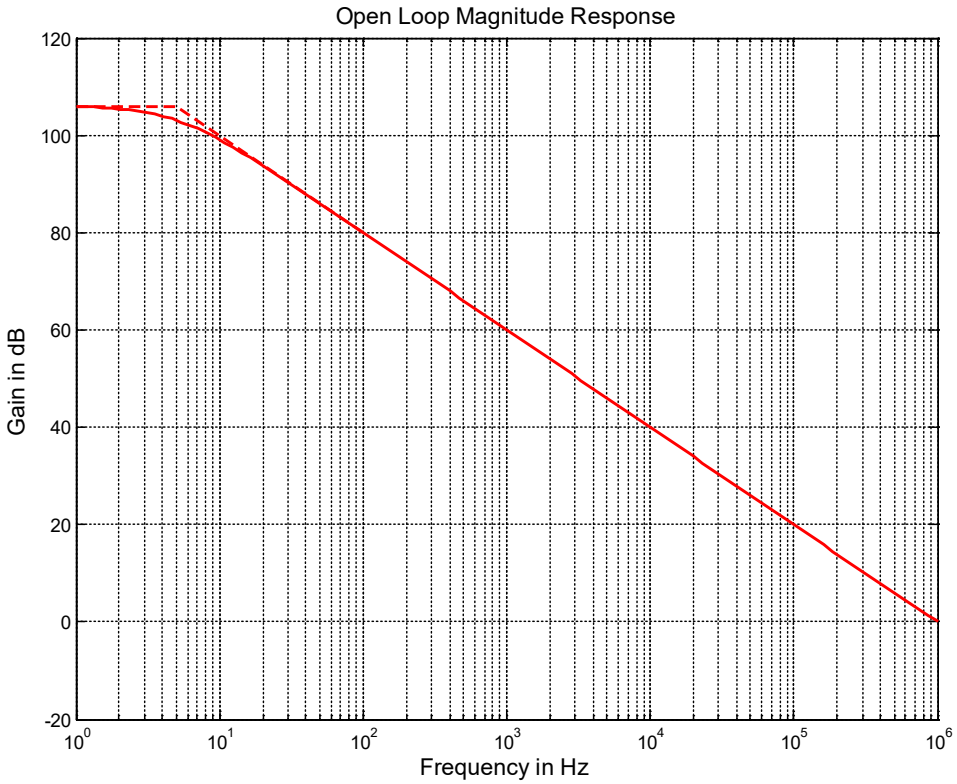
For stability reasons the μA741 (as well most other op-amps today) is "internally compensated." This means that above a certain frequency the μA741's gain is made to decrease, with an asymptotic slope of -20 dB/decade. A slope of -20 dB/decade implies that gain is inversely proportional to frequency, or the product of frequency and the gain at that frequency is a constant, commonly referred to as the *gain bandwidth product*. For a μA741 this constant is typically 1 MHz, which limits its use mainly to audio frequencies. Other op-amps may have larger gain bandwidth products and can be used at correspondingly higher frequencies. Typical gain versus frequency curves for a μA741 op-amp are shown in Figure 3.24. Figure 3.24a shows the theoretical response from 1 Hz to 1 MHz assuming a DC gain of 200,000 and a gain bandwidth of 1 MHz. The magnitude plot starts flat at 106 dB (200,000), and then breaks downward to a slope of -20 dB/decade, passing through 0 dB (gain of 1) at 1 MHz. The intersection of these two asymptotes occurs at a break frequency of

$$\frac{1\,\text{MHz}}{2 \times 10^5} = 5\ \text{Hz} = 31.4\ \text{rad/sec.}$$

From this information we can model A(s) in Figure 3.23 as a first order low-pass filter with a DC gain of 200,000 and a pole at s = -31.4, or

$$A(s) = \frac{2\pi \times 10^6}{s + 31.4} \tag{3.41}$$

Figure 3.24b shows the measured response of an actual op-amp from 1 Hz to 400 Hz. For this particular device, the DC gain is approximately 106 dB (200,000), and above 10 Hz the response decreases with a slope of -20 dB/decade. By measuring the gain at 100 Hz, we can observe that the actual gain bandwidth product for this particular device is approximately 700 kHz.




```
hold off;clf;
f=logspace(0,6,100);                    %100 logarithmically spaced points
                                        %from 10^1 to 10^6
b=[6.28e+06];                           %numerator   = 6.28e+06
a=[1 31.4];                             %denominator = s + 31.4
w=2*pi*f;
h=freqs(b,a,w);
mag=20*log10(abs(h));
semilogx(f,mag,'r-');
xlabel('Frequency in Hz'); ylabel('Gain in dB');grid;
title('Open Loop Magnitude Response')
```

Figure 3.24a. Open loop frequency response of μA741 op-amp (top) and short MATLAB code segment which produced this plot (bottom). (Plot assumes a device gain-bandwidth product of 1 MHz.) (The dashed line indicates asymptotes.)

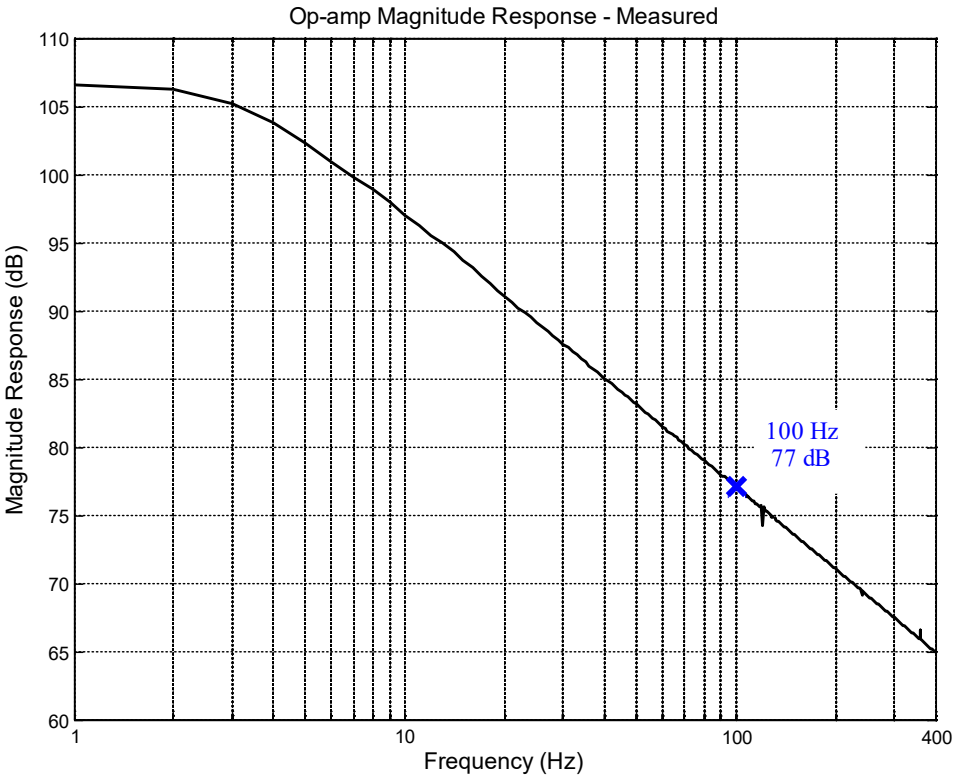


Figure 3.24b. Measured μA741 op-amp frequency response.

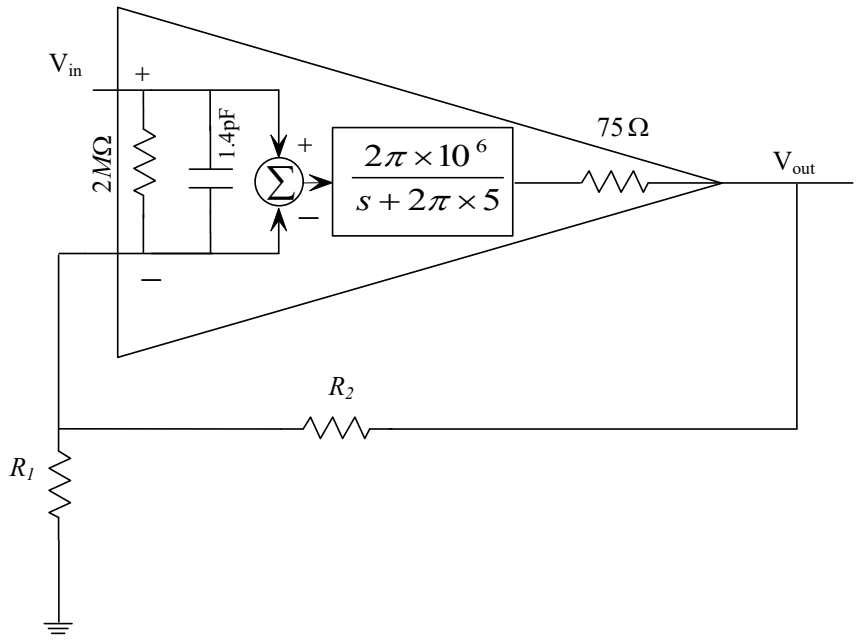


Figure 3.25. Revised model of non-inverting amplifier.

Figure 3.25 shows a more complete representation of our non-inverting amplifier circuit from Figure 3.23. Figure 3.25 takes into account the frequency response plus the input and output impedances of the op-amp. What we are interested in are the closed loop frequency response, and the input and output impedances as functions of op-amp (open loop) parameters. By "closed loop" frequency response we mean that we are considering the entire circuit transfer function from V_{in} to V_{out} in Figure 3.23. By "open loop" frequency response we mean that we are considering only the frequency response characteristics of the op-amp device itself. While it is possible to analyze the complete system, it will be simpler and more intuitive to demonstrate three important points. First, we will observe that (finite) op-amp input impedance affects only the closed loop input impedance, and does not affect closed loop frequency response or output impedance. Second, we will observe that (non-zero) output impedance affects only the closed loop output impedance, and does not affect closed loop frequency response or input impedance. Finally we will conclude that the frequency response is the dominant (linear) departure from the ideal in most practical circuits.

We will first assume that the equivalent parallel resistance of R_1 and R_2 in Figures 3.23 and 3.25 is much less than the open loop input impedance of the op-amp. (This is not an overly restrictive assumption. We will see later that op-amp input bias and offset currents usually require us to design circuits using resistors much smaller than a MΩ, hence making this assumption valid for useful circuits.)□□ This implies the voltage at the inverting terminal is

$$V_- = V_{out}\left(\frac{R_1}{R_1 + R_2}\right) = \frac{V_{out}}{G_{dc}}, \tag{3.42}$$

where G_{dc} is the closed loop DC gain, $\left(1+\frac{R_2}{R_1}\right)$. Note that V- is not a function of the input impedance of the op-amp.

In Figure 3.25 if we assume no extra load is connected to the output, the load that the op-amp "sees" is a series resistance of (R_1+R_2). If we further assume this resistance is very large in comparison to the nominal 75Ω open loop output resistance of the device itself, the system in Figure 3.25 can be drawn in block diagram form as shown in Figure 3.26.

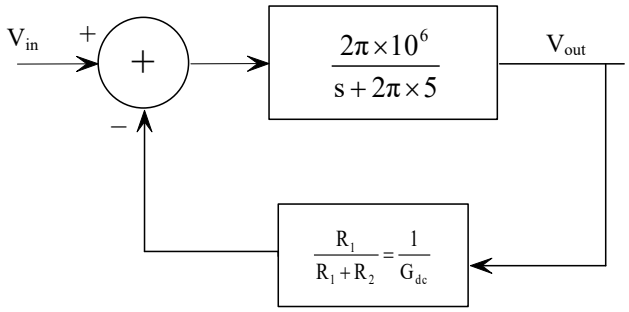


Figure 3.26. Block diagram of circuit from Figure 3.25 assuming no load.

The transfer function follows from this block diagram as

$$\begin{aligned}\frac{V_{out}}{V_{in}} &= \frac{\left(\frac{2\pi\times10^6}{s+2\pi\times5}\right)}{1+\left(\frac{1}{G_{dc}}\right)\left(\frac{2\pi\times10^6}{s+2\pi\times5}\right)} \\ &= \frac{2\pi\times10^6}{s+2\pi\times5+\left(\frac{2\pi\times10^6}{G_{dc}}\right)} \\ &\cong \frac{2\pi\times10^6}{s+\left(\frac{2\pi\times10^6}{G_{dc}}\right)} \quad , \end{aligned} \tag{3.43}$$

or a first order low-pass filter with a DC gain of G_{dc} and a bandwidth of $\left(\frac{1MHz}{G_{dc}}\right)$.

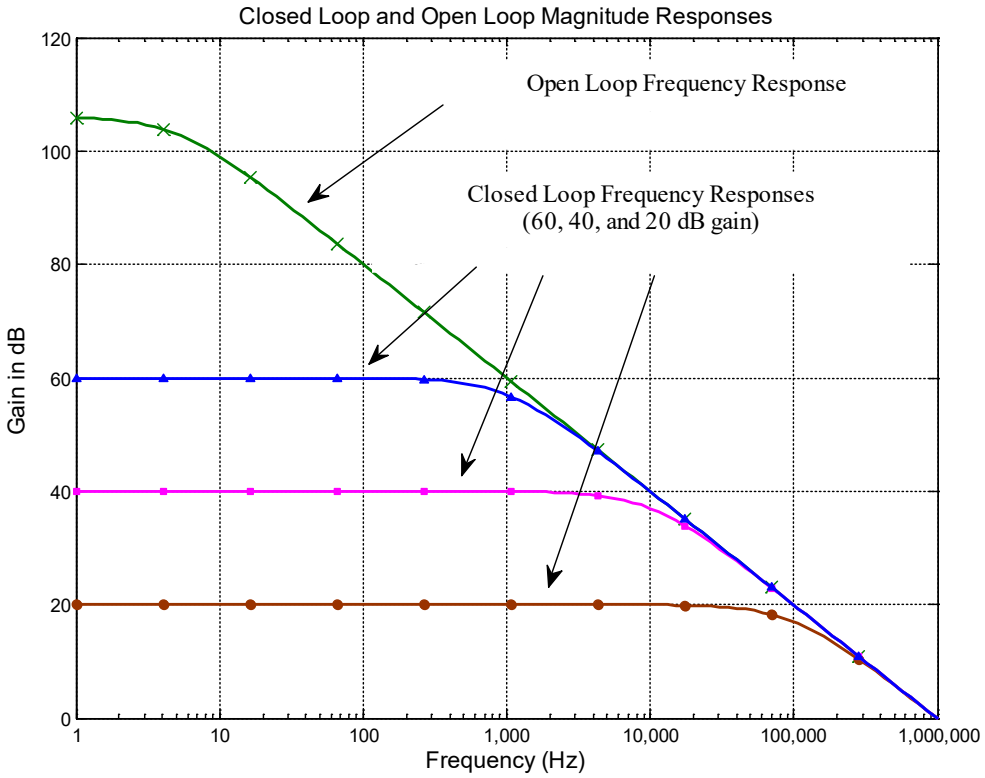


Figure 3.27. Frequency response as a function of DC gain.

Figure 3.27 compares the closed loop frequency response characteristics for a family of non-inverting amplifiers from 3.43. More specifically, we compare closed loop frequency responses designed for gains of $G_{dc} = 10$, $G_{dc} = 100$, and $G_{dc} = 1000$ to the open loop response shown in Figure 3.24 for that same op-amp. Notice how the gain equals the desired value at low frequencies, and at high frequencies each closed loop gain curve bends downward to follow the open loop gain characteristic. Another interpretation for the gain bandwidth product of the op-amp is that the product of the DC gain and the 3 dB bandwidth of a non-inverting amplifier is 1 MHz. For example, if you want a gain of 100, you may only amplify by this (constant) amount to a 3dB bandwidth of 10 kHz.

Gain	x	Bandwidth	=	Gain Bandwidth Product
10	x	100 kHz	=	1 MHz
100	x	10 kHz	=	1 MHz
1000	x	1 kHz	=	1 MHz

Example 3.10 Real Differentiators

The finite gain bandwidth product of real op-amps can result in strange behavior in seemingly innocent looking first order circuits. As an example consider the scaled differentiator transfer function from 3.44,

$$H(s) = \frac{-s}{100}, \tag{3.44}$$

shown in Figure 3.28. Since we will be using actual data to illustrate the behavior, and we will be using the same op-amp (μA741) as shown in Figure 3.24(b), we will use a gain bandwidth product of 700 kHz (4.4 x 10^6 rad/sec) and a DC gain of 200,000 in our model. (How did we get these numbers? Note that the cursor "x" in Figure 3.24b marks a point on the constant gain bandwidth curve, specifically 100 Hz and 77 dB, and the product of this gain and this bandwidth is approximately 700 kHz. We judge the low frequency gain to be approximately 106 dB, or a gain of 200,000.) Given the gain bandwidth product and DC gain, the "open loop" magnitude response starts out at low frequency at 106 dB, and then rolls off to a slope of minus 20 dB/decade at ω = 22 rad/sec.

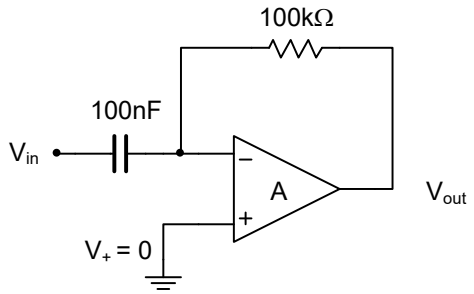


Figure 3.28. Differentiator circuit.

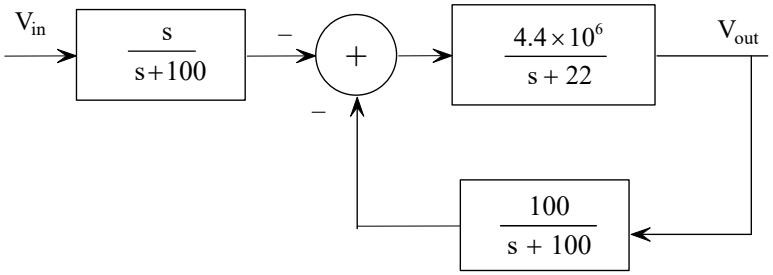


Figure 3.29. Block diagram of differentiator circuit.

Using block diagram algebra the transfer function is

$$H(s) = -\left(\frac{s}{s+100}\right)\left(\frac{\frac{4.4\times10^6}{s+22}}{1+\frac{4.4\times10^6}{s+22}\left(\frac{100}{s+100}\right)}\right)$$

$$= -\frac{4.4\times10^6 s}{s^2+122s+4.4\times10^8} \tag{3.45}$$

or a very narrow band (high Q) second order band-pass filter with a center frequency of

$$\omega_o = \sqrt{4.4\times10^8} = 2.1 \text{ x } 10^4 \text{ rad/sec or 3.34 kHz,} \tag{3.46}$$

a Q given by

$$122 = \frac{\omega_0}{Q}$$

$$Q = \frac{2.1\times10^4}{122} = 172\,, \tag{3.47}$$

and a center frequency gain of

$$\frac{4.4\times10^6}{122} = 3.6 \text{ x } 10^4 \text{ or 91 dB.} \tag{3.48}$$

At this point we note that in most cases, a closed loop transfer function typically does not have a larger gain at a particular frequency than the open loop response at that same frequency. The result from 3.48 seems counter-intuitive in the sense that it suggests a center frequency gain of approximately 40 dB *more* than the open loop response of the same op-amp (Figures 3.24a and 3.24b). In fact, our analysis in 3.45-3.48 is correct, and this example is not typical of "most cases." Actual measurement shown in the upper curve in Figure 3.30 shows that the measured frequency response exhibits a gain of 75.5 dB at the center frequency, thereby verifying the results of our analysis.

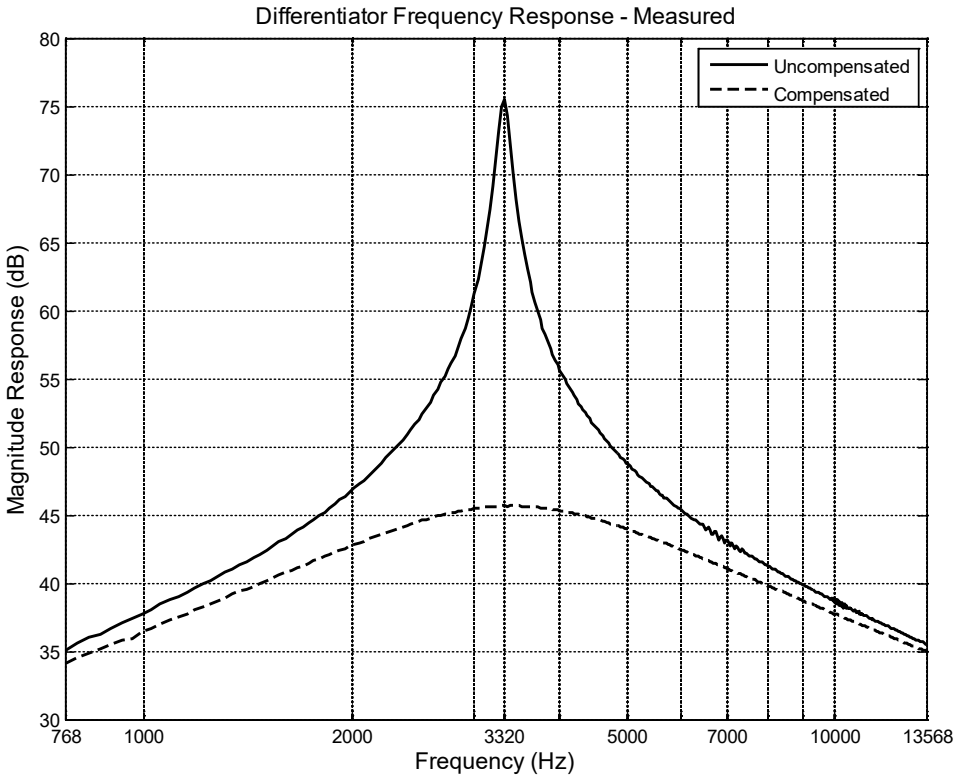


Figure 3.30. Frequency response of real differentiator.

At this point we might ask:

(1) Does this circuit perform the differentiation function?
(2) If not, can one differentiate incoming signals using op-amp circuits?

Figure 3.31a shows the resulting output if one uses the circuit from Figure 3.28 to differentiate a 100 Hz triangular waveform. (The ideal output would be a 100 Hz square wave.) The ringing (oscillation) is due to the highly underdamped (high Q) transfer function from 3.45, which was produced using our "real-world" op-amp. The circuit looks like a differentiator to input signals band-limited to 0-1 kHz, but does not look like a differentiator to input signals with spectral components near the circuit's resonant frequency, or much higher than 1 kHz. As a result, if we want a circuit that will look like a differentiator over a reasonably wide frequency range, one solution is to design a high-pass filter from the beginning. By this we mean that we will make our classic ideal op-amp assumption and place the pole frequency at approximately the intersection of the low frequency differentiator (+20 dB/decade) asymptote and the open loop frequency response (minus 20 dB/decade) asymptote. This can be done by either adding a resistor in series with the capacitor (see Figure 3.13), or by adding a capacitor in parallel with the feedback resistor (see Figure 3.32). The result of differentiating the same 100 Hz triangular input waveform using the compensated circuit is shown in Figure 3.31b. The frequency response of this compensated circuit is shown in the lower trace of Figure 3.30.

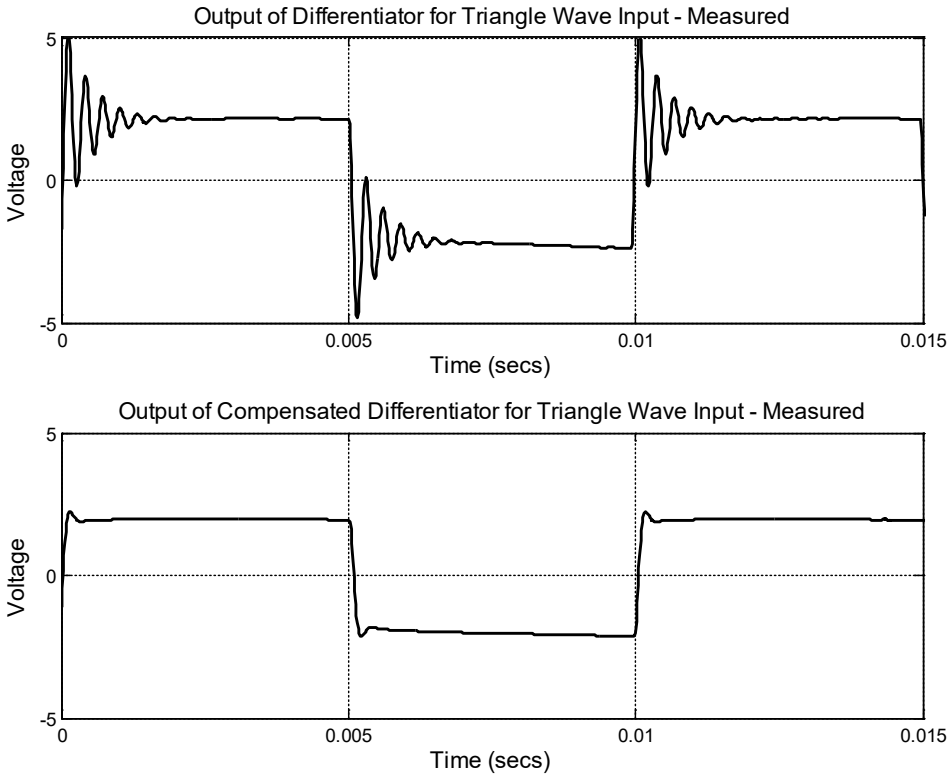


Figure 3.31. Output of differentiator circuit for triangle wave input at 100Hz. Figure 3.31a, above, shows the output for the uncompensated design in Figure 3.28, while Figure 3.31b, below, shows the output for the compensated design from Figure 3.32.

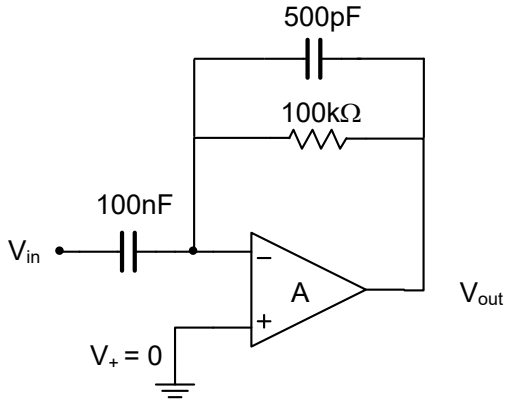


Figure 3.32. Compensated differentiator.

Closed Loop Output Impedance

To determine the output impedance of the closed loop system from Figure 3.25 we will determine the transfer function between V_{in} and the short circuit output current (I_{sc}), and compare it to the voltage transfer function $\frac{V_{out}}{V_{in}}$. More specifically, we will soon calculate the closed loop output impedance as $Z_{outc} = \frac{\left(V_{out} / V_{in} \right)}{\left(I_{sc} / V_{in} \right)}$. In order to find the short circuit output current (I_{sc}) we "ground" the op-amp output. Since both V_{out} and therefore V_- are at ground potential, referring to Figure 3.25 we calculate the short-circuit current as

$$I_{sc} = \frac{V_{in}\left(\frac{6.28 \times 10^6}{s + 31.4} \right)}{75}$$

so that

$$\frac{I_{sc}}{V_{in}} = \frac{8.37 \times 10^4}{s + 31.4} \tag{3.49}$$

Please note that this result is for analysis purposes only. We are not suggesting that one could actually ground the output of a μA741 op-amp, apply 1 volt to the non-inverting input, and obtain $\frac{8.37 \times 10^4}{31.4}$ or 2667 Amps of output current. The maximum output current for a μA741 is approximately 25 mA, and our linear model is accurate only for output currents significantly less than that maximum.

The closed loop output impedance (Z_{outc}) is then

$$Z_{outc} = \frac{\left(V_{out} / V_{in} \right)}{\left(I_{sc} / V_{in} \right)} = \frac{\left(\frac{6.28 \text{ x } 10^6}{s + \frac{6.28 \text{ x } 10^6}{G_{dc}}} \right)}{\left(\frac{8.37 \text{ x } 10^4}{s + 31.4} \right)}$$

$$= \frac{75\,(s + 31.4)}{s + \frac{6.28 \text{ x } 10^6}{G_{dc}}} \text{ Ohms} \quad . \tag{3.50}$$

The closed loop DC output resistance (evaluating at s=0) is then

$$Z_{outc}\Big|_{s=0} = \frac{75\,(31.4)}{\frac{6.28 \text{ x } 10^6}{G_{dc}}} = \frac{75}{\left(2 \times 10^5 / G_{dc} \right)}$$

so that the closed loop output resistance is reduced from the open loop output resistance by a factor of:

$$\frac{\text{OpenloopDCgain}}{\text{ClosedloopDCgain}} = \frac{2\times10^5}{G_{dc}} \tag{3.51}$$

for this example. Said another way, the output impedance is virtually zero for all practical non-inverting amplifier circuits! From 3.50 we see the output impedance then increases proportional to frequency from 5 Hz to the 3 dB bandwidth and then remains constant at 75Ω. Output impedance as a function of frequency for G_{dc} = 10, 100, and 1000 is shown in Figure 3.33.

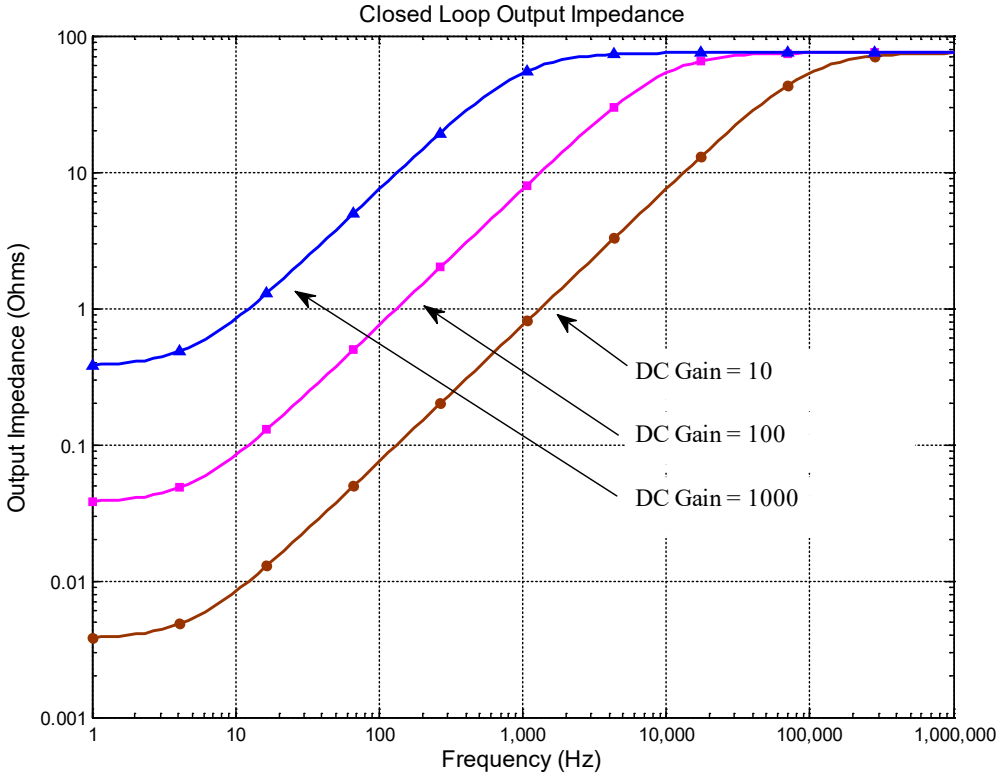


Figure 3.33. Closed loop output impedance as a function of frequency and DC gain.

When we design multiple stage filters in following chapters, we can conclude that if the load impedance or the input impedance to the following stage is in excess of 1 kΩ the output impedance is negligible and will be ignored.

Closed Loop Input Impedance

To determine input impedance we first determine the differential input voltage, then the input current using our circuit from Figure 3.25. We will assume the load impedance does not affect output voltage.

$$\frac{V_d}{V_{in}} = \frac{\left(\frac{V_{out}}{V_{in}}\right)}{\left(\frac{V_{out}}{V_d}\right)} = \frac{\left(\frac{6.28\times10^6}{s+\frac{6.28\times10^6}{G_{dc}}}\right)}{\left(\frac{6.28\times10^6}{s+31.4}\right)}$$

$$= \frac{s+31.4}{s+\frac{6.28\times10^6}{G_{dc}}} \tag{3.52}$$

Furthermore,

$$I_{in} = Y_{ino}\, V_d \tag{3.53}$$

where V_d is the differential input voltage, and

$$Y_{ino} = \frac{1}{2M\Omega} + s\left(1.4\times10^{-12}\right)$$

is the open loop input admittance. (Remember that parallel admittances are additive!) The closed loop input impedance is given by

$$Z_{inc} = \frac{V_{in}}{I_{in}} = \frac{V_{in}}{(V_d)Y_{ino}} \tag{3.54}$$

$$= \frac{1}{\left(\frac{s+31.4}{s+\frac{6.28\times10^6}{G_{dc}}}\right)\left(\frac{1}{2M\Omega} + s(1.4pF)\right)}$$

$$= \frac{7.14\times10^{11}\left(s+\frac{6.28\times10^6}{G_{dc}}\right)}{(s+31.4)\left(s+3.57\times10^5\right)} \quad . \tag{3.55}$$

This says that the closed loop DC input resistance is *increased* from the open loop input resistance (2MΩ) by the factor

$$\frac{\text{OpenloopDCgain}}{\text{ClosedloopDCgain}} = \frac{2\times10^5}{G_{dc}}. \tag{3.56}$$

Note that this is the same factor by which the output resistance was reduced! The magnitude of the impedance begins at $\left(\frac{4\times10^{11}}{G_{dc}}\right)$ Ohms at DC, and then decreases inversely proportional to frequency above 5 Hz. Eventually the impedance is dominated by the input capacitance. A plot of input impedance as a function of DC gain and frequency is shown in Figure 3.34.

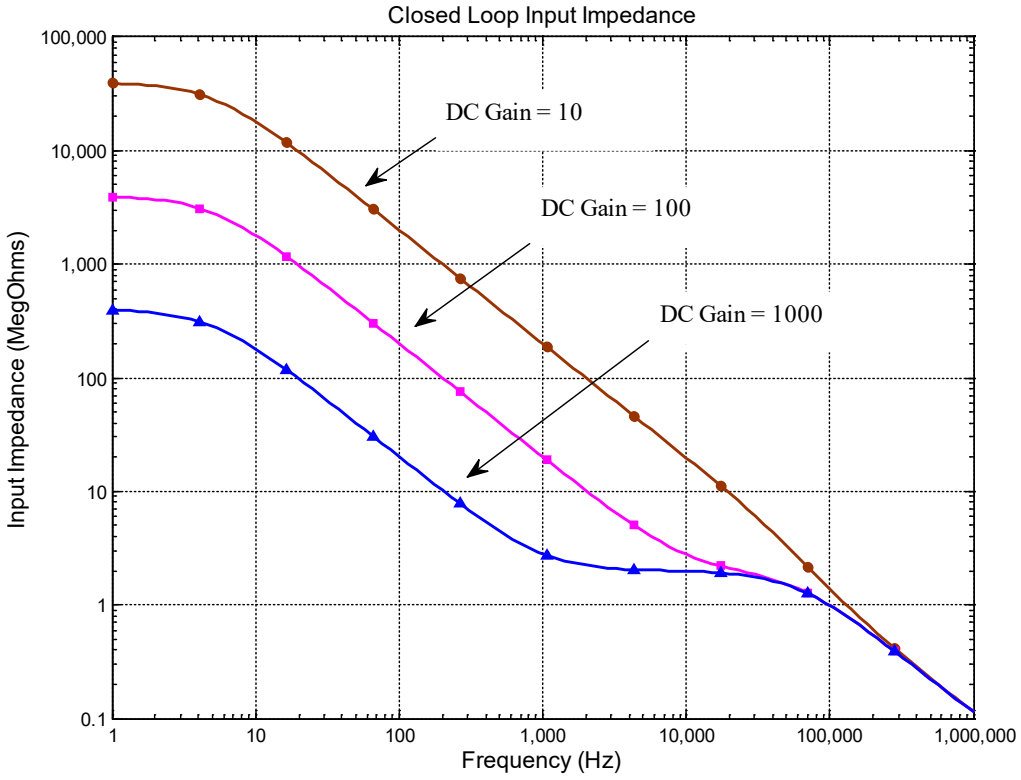


Figure 3.34. Input impedance as a function of frequency and DC gain.

It should be noted that these very large values of DC resistance are somewhat misleading. They do not imply that the current into the non-inverting input is zero. As we will see later, bias currents of several nanoamps do exist. If extremely high input impedance is necessary for a particular application, other op-amps with much smaller bias currents and higher input impedance are available.

Just as with the closed loop output impedance case, the closed loop input impedance at audio frequencies is close enough to the ideal that we will ignore these effects in our designs. We should note, however, that our analysis was conducted only on non-inverting amplifier configurations. The input impedance of circuits connected in an *inverting* configuration (such as shown in Figure 3.6) is simply the impedance between the input and the inverting terminal, since the inverting terminal is a virtual ground. This is a disadvantage for inverting op-amp configurations, in that the input impedance can be much smaller than the large values we saw for closed loop input impedance for non-inverting op-amp configurations.

Although the finite gain bandwidth product limitation of our op-amp is the principal linear effect we must consider in our design work, there are offsets, biases, and non-linearities we need to consider as well.

Slew Rate

Op-amps are limited in how fast the output voltage can change (or slew) with respect to time. This maximum transition rate or slew rate is specified as 0.5 V/μsec for a μA741. Other wider bandwidth op-amps have faster slew rates. Figure 3.35 illustrates voltage waveforms observed when a non-inverting amplifier is driven by a high frequency square wave.

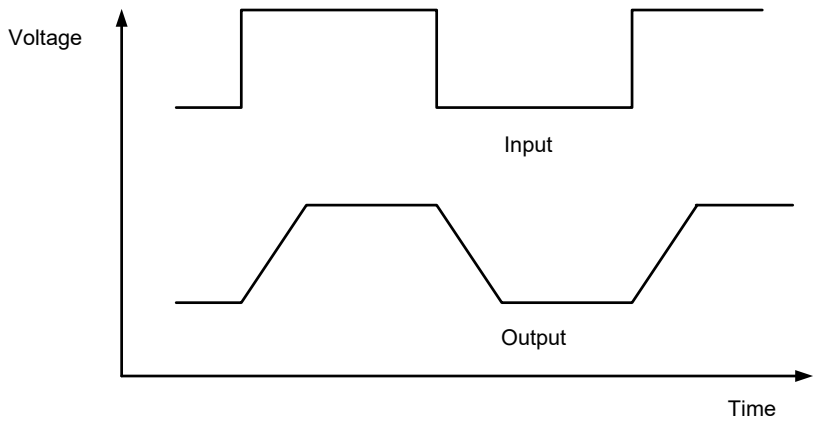


Figure 3.35. Effect of finite slew rate on output waveform.

We can easily calculate the maximum output amplitude sinusoid the μA741 can "track" at a certain frequency. For example to avoid a slew-rate non-linearity, we must insist that

$$\left|\frac{dV_{out}(t)}{dt}\right| < 0.5\ V/\mu sec \tag{3.57}$$

and if the output waveform is of the form

$$V_{out}(t) = M\sin(\omega t) \tag{3.58}$$

then

$$\left|\frac{dV_{out}(t)}{dt}\right| = M\omega\cos(\omega t) < 0.5\ V/\mu sec$$

and

$$M < \frac{0.5V/\mu sec}{\omega}\ . \tag{3.59}$$

As we saw in the non-inverting amplifier from Figure 3.23, when designed for a DC gain of 10, it had a -3 dB bandwidth of 100 kHz (Figure 3.27). Unfortunately, at that frequency, our op-amp only can track sinusoids of output amplitude less than

$$\frac{0.5\times10^{6}\,\text{V/s}}{2\pi\times10^{5}} = 0.8 \text{ Volts.} \tag{3.60}$$

This means we have an upper amplitude limitation for our *input* sinusoid of about 0.08 volts at a frequency of 100 kHz before our device becomes slew-rate limited. Hence, although our *linear* analysis suggested that our device would be useful for amplifying signals with frequency components up to 100 kHz, this non-linear effect of slew rate limitation essentially limits the μA741's usefulness to audio frequencies.

Offsets and Biases

The input offset voltage is the differential input voltage when the output voltage is zero. For a μA741 it is typically 1 mV. It presents problems when designing amplifiers with very large DC gains. For example, an amplifier with a gain of 1000 might have a 1 Volt output with a zero input. Straightforward methods of eliminating this offset exist.

DC currents (in addition to any currents due to the input signal) exist in the input terminals. The input bias current is the average of these two currents and the input offset current is their difference. Typical values for a μA741 op-amp are 80 nA and 10 nA respectively. Other op-amps have typical values of less than 1 nA. These bias currents tend to limit the size of the resistors that can be used in circuits, however methods do exist to compensate. To illustrate these concepts, consider the following example.

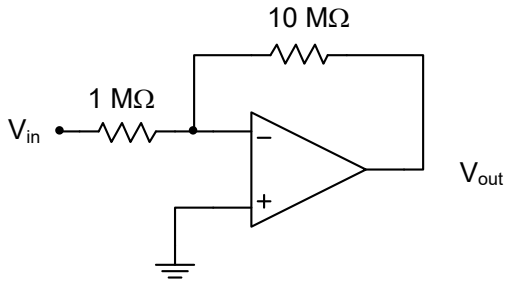


Figure 3.36. Inverting amplifier subject to bias.

Assuming an 80 nA current in the inverting terminal, the node equation at that point is

$$\frac{V_{in}}{1\text{M}\Omega} + \frac{V_{out}}{10\text{M}\Omega} = 80 \text{ nA} \tag{3.61}$$

Solving for V_{out} we obtain

$$V_{out} = -10\, V_{in} + 0.8\,, \tag{3.62}$$

or a constant error of the bias current times the feedback resistance (i.e. +0.8V). If we add a resistor between the non-inverting terminal and ground as in Figure 3.37 and assume the same current flows in both terminals, ($I_{offset} << I_{bias}$), we can compensate for this bias. The voltage at the non-inverting terminal is

$$V_+ = (-80\text{ nA})\,R$$

This voltage is amplified by a factor of +11, therefore R should be approximately 910 kΩ to cancel the bias due to the input bias current. This resistance is merely the parallel equivalent of the two resistors connected to the inverting terminal.

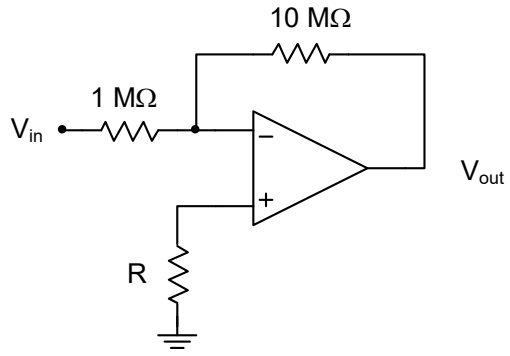


Figure 3.37. Inverting amplifier compensated for bias currents.

Another consequence of non-zero bias currents is that we cannot use integrators by themselves without an external DC feedback path (as in the biquad circuit.) Without DC feedback the output of circuit in Figure 3.7 would slew at a constant rate of $\frac{I_{bias}}{C}$ until it reached the maximum output voltage of the op-amp and then would remain constant. Adding a large feedback resistor will eliminate this problem but the circuit will not look like an integrator below a few 10^{ths} of a Hz. Therefore, for applications such as analog computers where we need to integrate very low frequency signals, op-amps with much lower bias currents are required.

Reasonable Values of Components

The range of resistance values we will choose in our circuit designs is primarily a function of the maximum output current and the input bias current of the op-amp being used. Since the maximum output current of a μA741 is 25 mA, we should design using 1 kΩ or larger resistors and the power rating of the resistor is not an issue. Designs using other op-amps with larger current outputs can use smaller resistor values, but 1/4 watt resistors may not suffice. We would like our signal currents to be much larger than any bias currents, therefore 100 kΩ is considered a reasonable upper limit when using a μA741. When using other op-amps with much lower bias currents, resistors up to 10 MΩ may be reasonable.

The range of reasonable capacitance values is primarily a function of stray capacitance at the small end and space and cost at the high end. A value of 100 pF is a reasonable lower limit, since much less becomes comparable to stray capacitance. A value of 1 μF is a reasonable upper limit as larger bipolar, low leakage capacitors are expensive and dimensionally large.

As we have already seen and will see throughout the book, time constants are the product of resistance and capacitance. If we need time constants of less than 100 kΩ x 1 μF = 0.1 sec (or cutoff frequencies of less than 10 rad/sec) our choices are to use either a better op-amp or a large, expensive

capacitor. At the opposite end of the limits, 1/(100 pF x 1 kΩ) = 10^7 rad/sec is well beyond the frequency response of the device.

Non-Linearities

One important feature of op-amps with negative feedback is that the closed loop system will be highly linear even if the op-amp itself is non-linear. Since data sheets provide little guidance on the non-linearity of the op-amp, the best illustration is data from an actual op-amp. The circuits used to measure non-linearities are shown in Figure 3.38. The normal method for measuring the linearity of an amplifier is to use a pure sinusoid as an input and measure the Total Harmonic Distortion (THD) of the output. The effect of non-linearities is to generate harmonics of the input frequency. Total Harmonic Distortion relates the root-squared sum (RSS) of the harmonic components to the amplitude of the fundamental, and is usually expressed either in dB or as a percent. ($\%THD = (100)\frac{\sqrt{V_2^2+V_3^2+V_4^2+...+V_n^2}}{V_1}$, where V_1 represents the amplitude of the fundamental frequency and V_k represents the amplitude of the k^{th} harmonic.)

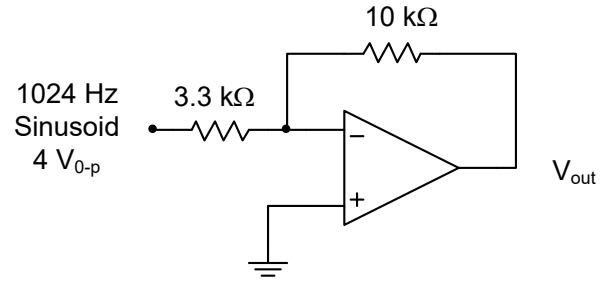


Figure 3.38a. Inverting amplifier under no load conditions.

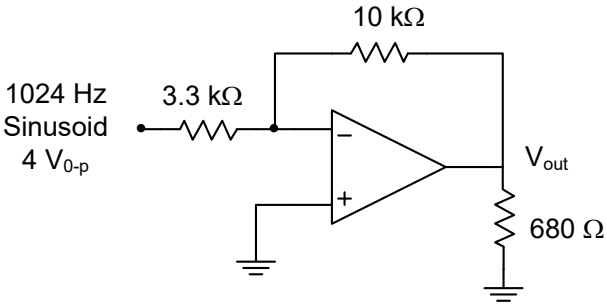


Figure 3.38b Inverting amplifier with 680Ω load drawing 18 mA zero to peak.

Figure 3.39 shows the spectra of both the output (top trace) and the differential input (V_-) (bottom trace) for the unloaded circuit in Figure 3.38a. Note that the output is almost a perfect sinusoid (THD = 0.008%) indicating the closed loop system is highly linear. The differential input is significantly more distorted (THD = 0.194%). This indicates the combination of large open loop gain and negative feedback produces the appropriate distorted signal at the op-amp's input resulting in an undistorted output. *A non-linear open loop system becomes a linear closed loop system.*

Note also that the op-amp itself becomes much more non-linear when connected to a load. The maximum output current in the circuit in Figure 3.38b is 18 mA, which is well within the 25 mA maximum possible. Figure 3.40 shows the output and differential input spectra for this circuit. The closed loop system is still quite linear (THD = 0.038%) even though the open loop system is now much more non-linear than before, as evidenced by the 7.8% THD in the differential input. Figure 3.41 shows the time domain waveforms of the output and differential input for the loaded circuit in Figure 3.38b. Note the significant distortion in the differential input, while the output is relatively undistorted.

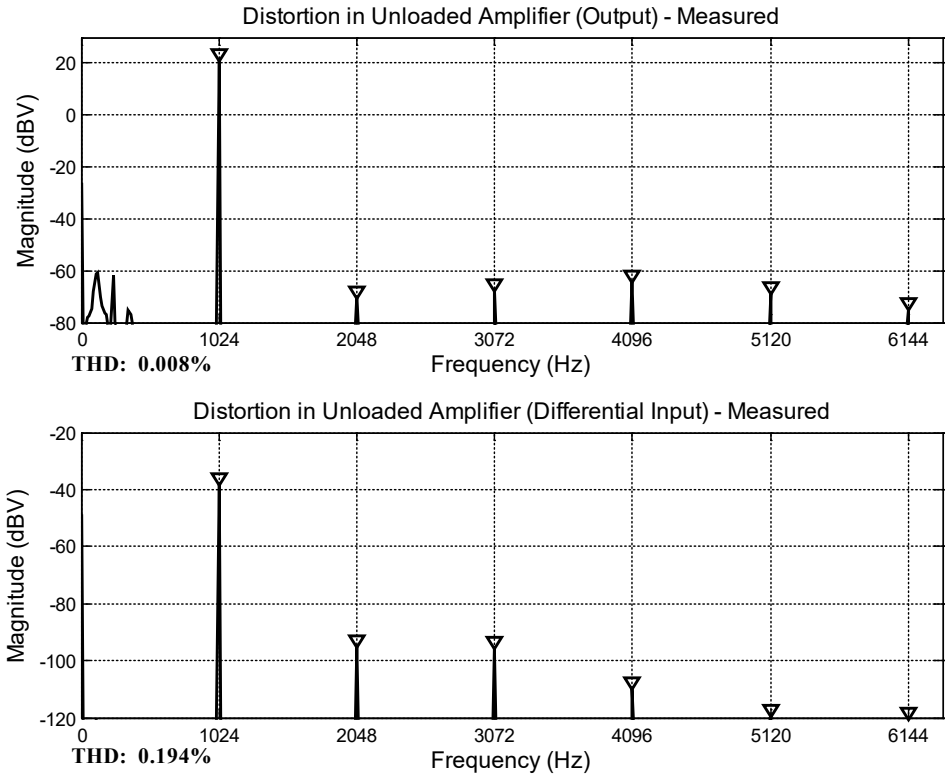


Figure 3.39. Distortion in Unloaded Amplifier

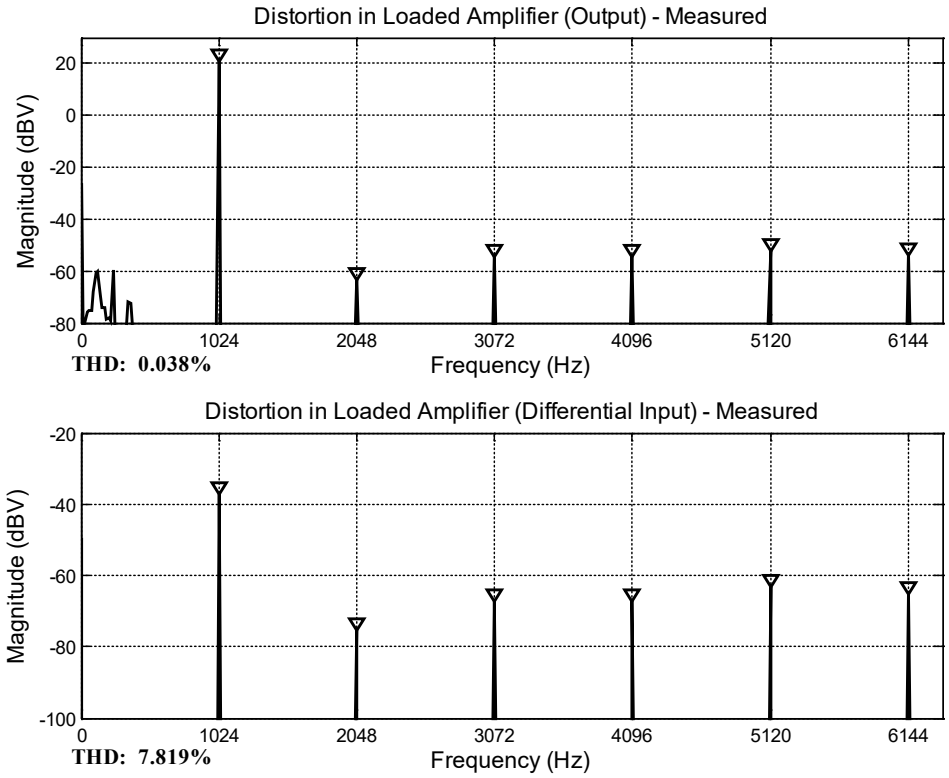


Figure 3.40. Distortion in Loaded Amplifier

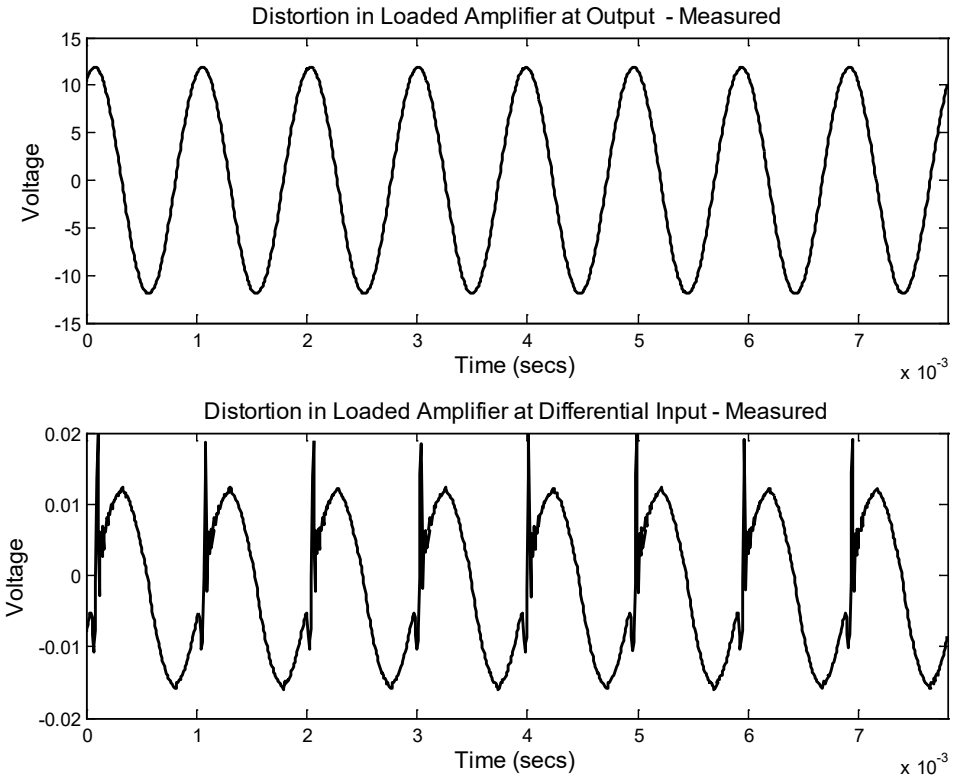


Figure 3.41. Distortion in Loaded Amplifier (Time Domain)

Stability

Stability in continuous time, linear, time-invariant (LTI) systems can easily be determined from pole locations. We know from linear system theory, a necessary and sufficient condition for a causal system (filter) to exhibit "Bounded Input Bounded Output" (BIBO) stability is that the poles of that system's transfer function must lie in the left half of the complex frequency plane (s plane). When we design filters we want the circuits to be stable. Assuming ideal op-amps and a virtual short between the differential inputs we will analyze circuits and solve for those poles. However, note that if we were to exchange the inverting and non-inverting inputs (but leave the remainder of the circuit unchanged), and still assume a virtual short between these inputs, the transfer function and therefore the poles would remain exactly the same. Is the circuit now stable? Our intuitive feel for positive feedback (where increasing output further increases differential input which in turn further increases output) suggests instability. If so, where is the unstable pole? Also, in later chapters we will analyze circuits with both positive and negative feedback. Since exchanging differential inputs doesn't change our ideal op-amp based analysis, how can we determine which connection is correct?

In partial answer to the questions above, since the op-amp itself can be modeled as a first order system, the total *actual* number of poles is one greater than that of our desired transfer function. This extra pole will lie in the right half of the s-plane (unstable) or the left half of the s-plane (stable), depending on how we have connected the circuit. In later chapters we will analyze the effect of using real op-amps by determining the third order transfer functions and poles of circuits originally designed as second order circuits.

To illustrate this point, consider the non-inverting amplifier in Figure 3.23, designed for a gain of ten. If we exchange inputs we have the circuit of Figure 3.42a.

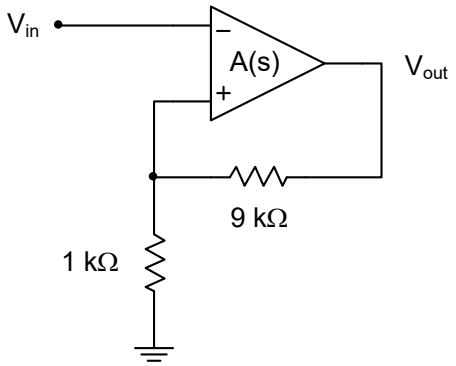


Figure 3.42a. Circuit for non-inverting amplifier with positive feedback.

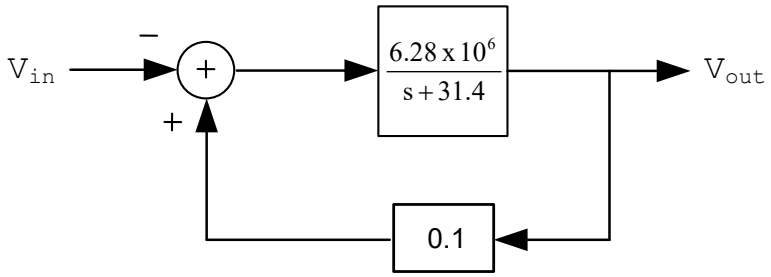


Figure 3.42b. Block diagram for non-inverting amplifier with positive feedback.

If we assume an ideal op-amp and a virtual short between differential inputs,

$$V_{in} = V_- = V_+ = \frac{V_{out}}{10}. \tag{3.63}$$

Therefore just as before

$$V_{out} = 10\, V_{in}.$$

If we take into account the transfer function of the op-amp itself, the block diagram in Figure 3.26 becomes that in Figure 3.42b, where the signs on the summer inputs have changed.

Employing standard block diagram algebra as we did before, we obtain

$$\frac{V_{out}}{V_{in}} = -\frac{\dfrac{6.28\times10^6}{s+31.4}}{1-0.1\left(\dfrac{6.28\times10^6}{s+31.4}\right)}$$

$$= -\frac{6.28\times10^6}{s+31.4-6.28\times10^5}$$

$$= -\frac{6.28\times10^6}{s-6.28\times10^5}, \tag{3.64}$$

Note that this represents the transfer function for an unstable system (due to the right half-plane pole).

This type of analysis may become quite tedious as we consider more complex circuits. For example, the biquad circuit in Figure 3.19 becomes fifth order if we model each of the three op-amps as a first order system. One way to simplify the analysis a bit is to ignore the pole in the open-loop transfer function at s = -31.4, and to model the open loop transfer function more simply as G/s. In this case, G is a constant which represents the gain bandwidth product in rad/sec. Such a simplification will keep the algebra somewhat less tedious. Another simplifying alternative is to analyze the circuit using a computer linear circuit analysis program. This has other benefits in that it allows the user to verify design validity, and it allows one to analyze the effects of using real (vice ideal) op-amps.

Resolving the stability issue from frequency response data is somewhat subtle. The magnitude response plot for the circuit in Figure 3.42a is exactly the same as that for the circuit in Figure 3.23. As shown in Figure 3.43, however, the phase plot changes in the *positive* direction for an unstable pole and in the *negative* direction for a stable pole. Therefore, if from our understanding of Bode plots we know what the phase plot should look like, we can detect instability.

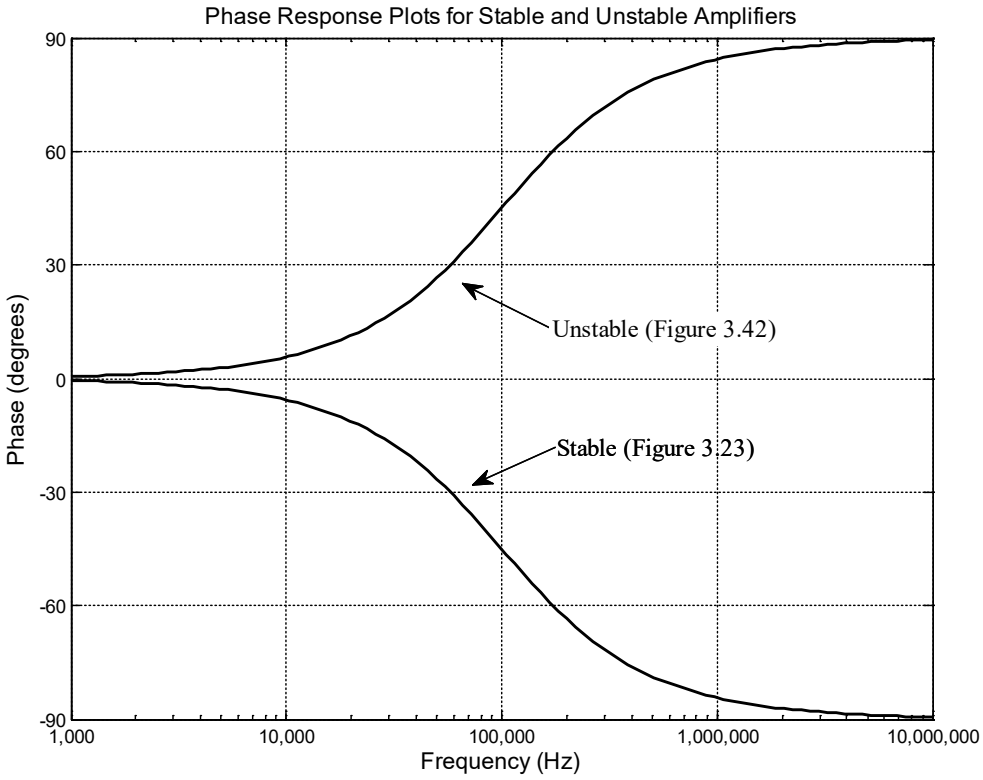


Figure 3.43. Phase plots for stable and unstable amplifiers.

If we try to analyze our design using a typical linear circuit analysis program, we first need a model of the op-amp suitable for the program. For example, if voltage controlled current sources are the only dependent sources allowed, we first determine the Norton equivalent of a voltage gain of 200,000 in series with an output resistance of 75 Ω. The transconductance is

$$g_m = \frac{2 \times 10^5}{75\,\Omega} = 2667 \text{ mhos}, \tag{3.65}$$

and the circuit model is shown in Figure 3.44.

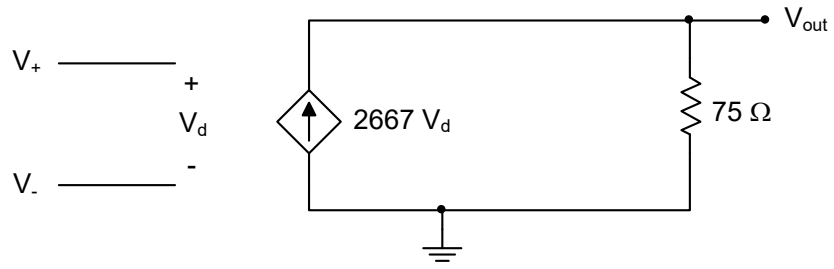


Figure 3.44. Op-amp model for use in linear circuit analysis program.

At this point, however, the finite gain bandwidth product of the op-amp is not explicitly modeled in the circuit of Figure 3.46. Many circuit analysis programs will allow the entry of a specific cutoff frequency for the dependent source, and that model will be adequate. If such an option does not exist in your analysis software, the cutoff frequency of 31.4 rad/sec can be modeled as a capacitor in parallel with the dependent source and resistance (Figure 3.45). That is, since we know the open-loop transfer function has a cutoff at

$$\frac{1}{RC} = 31.4 \text{ rad/sec}, \tag{3.66}$$

with an output resistance of 75Ω, our model needs a capacitance value of

$$C = \frac{1}{(31.4 \text{ rad/sec})\,(75 \text{ W})} = 425\ \mu\text{F} \tag{3.67}$$

in order to produce the proper open-loop cutoff frequency.

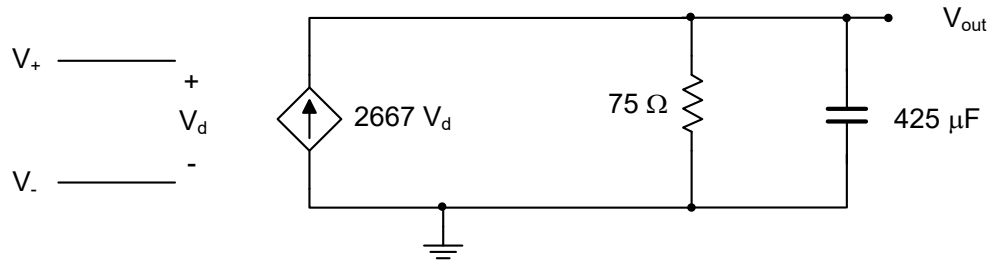


Figure 3.45. Op-Amp equivalent circuit explicitly modeling finite gain bandwidth.

Unfortunately, this model does not result in 75 Ω of output impedance for frequencies above the cutoff frequency. If analysis of the effects of output impedance is required, a series RC low-pass filter with the same cutoff frequency (31.4 rad/sec) could be added at the input instead, and the 425 μF capacitor could be removed from the op-amp model.

We should note also that the input impedance of the op-amp could be included as well. As we saw earlier, though, input impedance can be ignored in virtually all filter designs, and in the interest of keeping our model as simple as possible, we will ignore it here.

As an example of circuit modeling, we show Figure 3.46, which is a circuit model of the op-amp circuit of Figure 3.42a using the op-amp model of Figure 3.45.

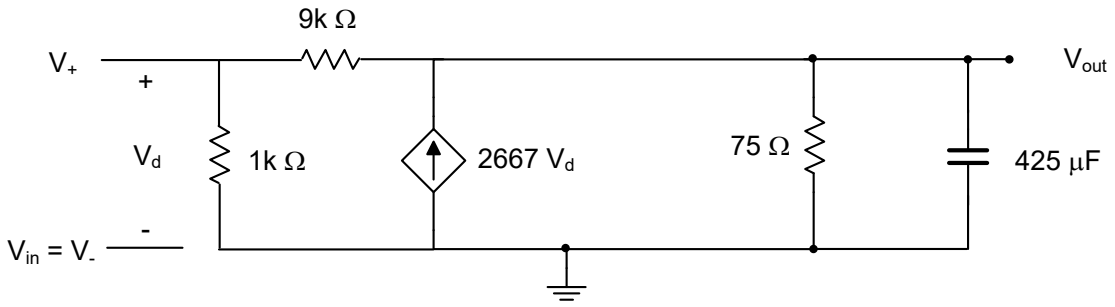


Figure 3.46. Model of positive feedback amplifier of Figure 3.42a.

Let us consider one additional example, and we will model the open loop transfer function simply as G/s, where G is a constant which represents the gain bandwidth product of our device in rad/sec. (Again, such simplification will keep the algebra somewhat less tedious.) For this example let us examine the circuit shown in Figure 3.47. Note that this circuit's stability is not immediately obvious, especially considering the combination of both positive and negative feedback.

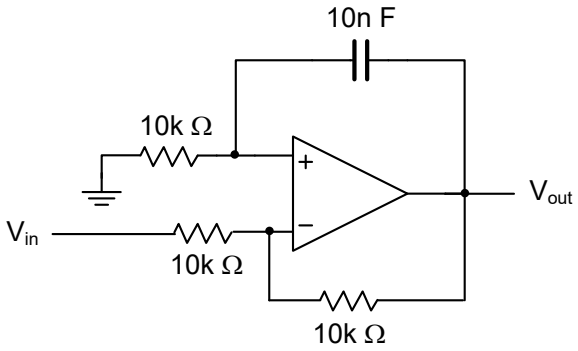


Figure 3.47 Circuit with both positive and negative feedback.

Using voltage division (coupled with superposition),

$$V_- = \frac{V_{out}}{2} + \frac{V_{in}}{2}. \tag{3.68}$$

The transfer function from V_{out} to V_+ is a first order high-pass filter, or

$$V_+ = \frac{s}{s + 10^4} V_{out}. \tag{3.69}$$

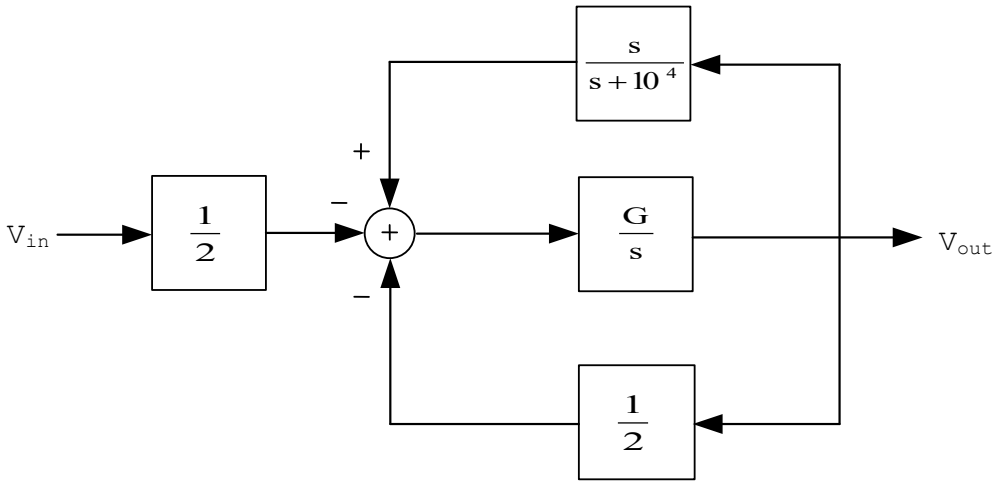


Figure 3.48a. Block diagram of circuit in Figure 3.47.

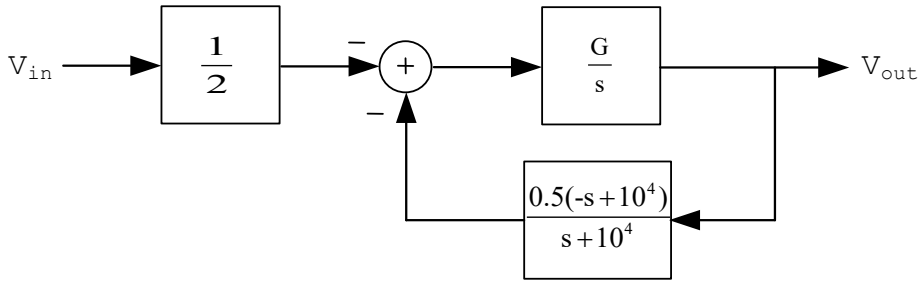


Figure 3.48b. Simplified block diagram of circuit in Figure 3.47.

Using block diagram algebra,

$$\frac{V_{out}}{V_{in}} = \left(-\frac{1}{2}\right)\frac{\frac{G}{s}}{1+\left(\frac{G}{s}\right)\left(\frac{0.5(-s+10^4)}{s+10^4}\right)} = \left(-\frac{1}{2}\right)\frac{G(s+10^4)}{s^2+(10^4 - 0.5G)s+G(5x10^3)} \tag{3.70}$$

Note that this transfer function is unstable for any op-amp with a gain bandwidth product in excess of 2 x 10^4 rad/sec. For G = 2π x 10^6 rad/sec (i.e. for a μA741 op-amp), both poles are unstable, at locations s = π x 10^6 and at s = 10^4. The phase response plot for the transfer function in 3.70 is shown in Figure 3.49.

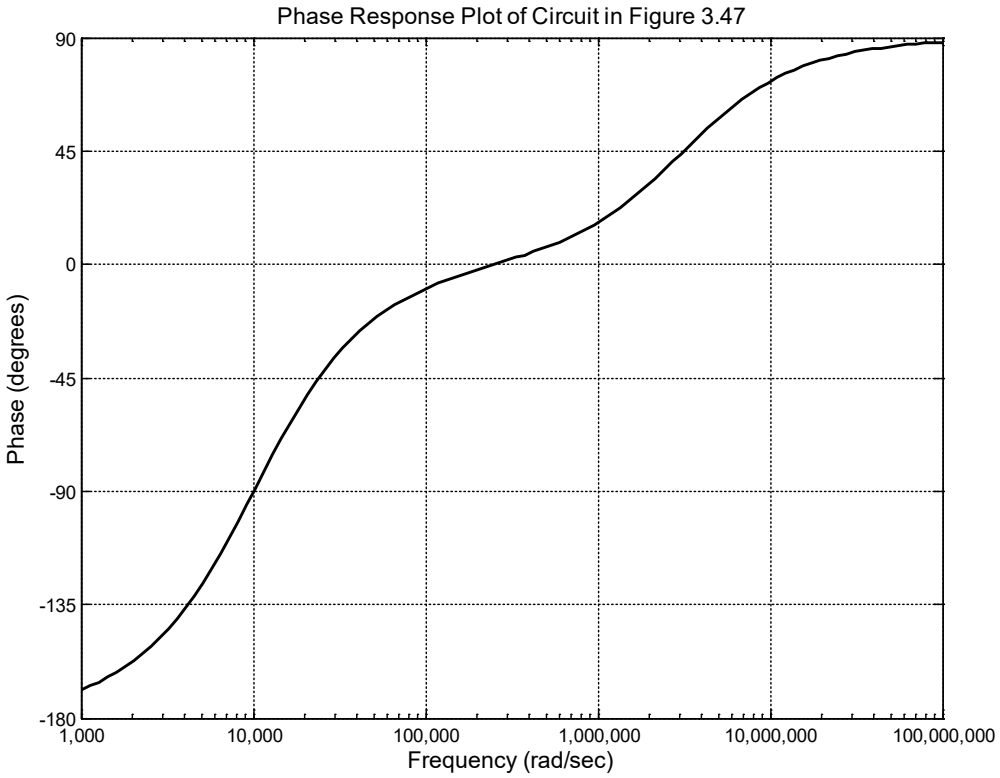


Figure 3.49. Phase plot of circuit in Figure 3.47.

As discussed, filter stability can always be determined from pole locations. As shown in the examples provided, it is important to remember that such analysis of pole locations must include the 1st order transfer function of that "real-world" op-amp in order to accurately predict stability.

3.6 Concluding Remarks

In this chapter we studied characteristics of both ideal and real operational amplifiers. We learned that ideal op-amps behave according to a simplified, ideal set of characteristics described in section 3.2 (Table 3.1). We also learned that if we operate a real-world op-amp well within the gain bandwidth constraints for that specific device, the ideal op-amp assumptions represent very good first-approximations to real world behavior. When one chooses to "push the envelope" in an operational amplifier application (e.g. designing a non-inverting amplifier for high gain and large bandwidth), we find that the resulting closed-loop response deviates significantly from ideal behavior. In the case of designing for both high gain and high bandwidth, suddenly gain is not constant as a function of frequency (Figure 3.27), closed loop output impedance is no longer almost zero (Figure 3.33), and closed loop input impedance is no longer near infinity (Figure 3.34), because the closed loop characteristics are being impacted significantly by the 1st order open-loop characteristic of the (real-world) op-amp itself! We also learned that real-world op-amps do not exhibit infinite slew rate capabilities, cannot supply an infinite amount of current, and do not have input currents that are exactly zero. As we will see in later chapters, this knowledge of real-world op-amp behavior will help us choose realistic component values and appropriate op-amp types, and it will help us understand and overcome some of the non-ideal limitations imposed.

Problems

3.1 For the circuit in Figure P3.1, find V_{out} as a function of V_1, V_2 and V_3.

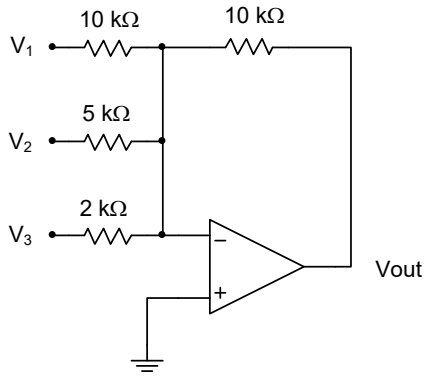


Figure P3.1

3.2 For the circuit in Figure P3.2, find V_{out} as a function of V_1, V_2 and V_3.

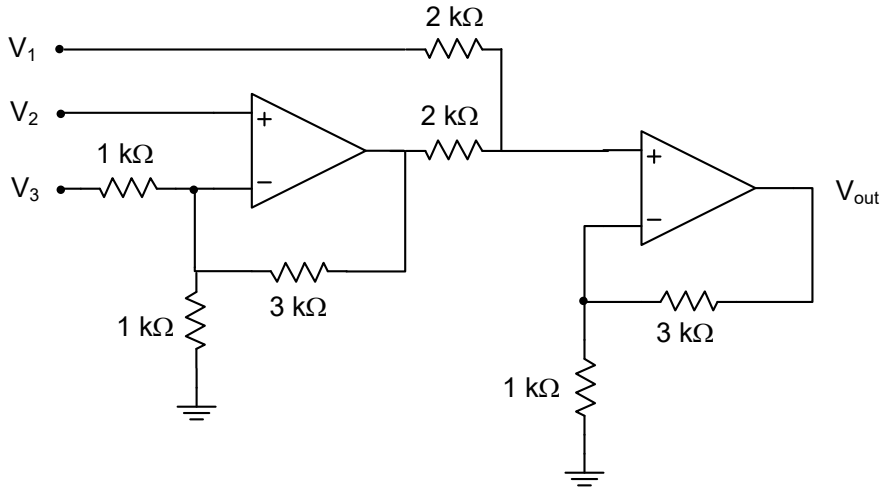


Figure P3.2

3.3 Design circuits such that V_{out} =

a. $3\ V_{in}$
b. $-20\ V_{in}$
c. $V_1 - V_2$
d. $-V_1 - 10\ V_2$
e. $-V_1 - 4\ V_2 + 3\ V_3$

3.4-7 For the circuits below

a. Find the transfer function $\frac{V_{out}}{V_{in}}$.

b. Plot the Bode Plot.

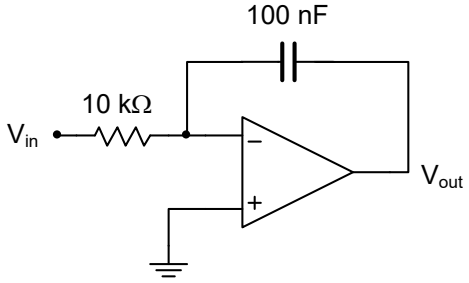


Figure P3.4

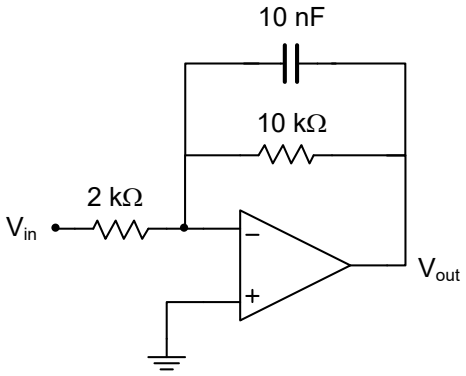


Figure P3.5

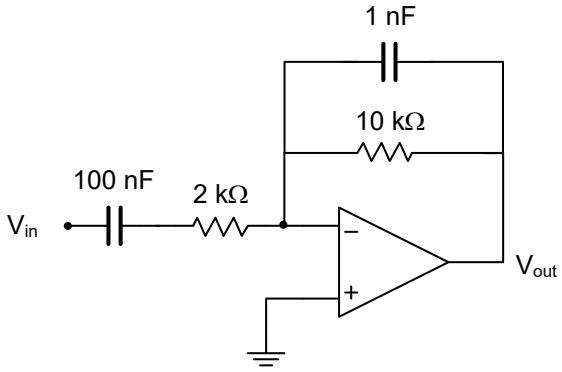


Figure P3.6

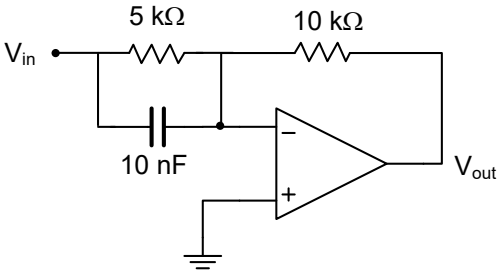


Figure P3.7

3.8 Design circuits such that $\frac{V_{out}}{V_{in}} =$

a. $-\frac{s}{1000}$ b. $-\frac{1000}{s}$ c. $-\frac{1000}{s+500}$

d. $-\frac{5s}{s+2000}$ e. $-\frac{5 \times 10^4 s}{(s+1000)(s+5000)}$

3.9-13 For the frequency response plots in Figures P3.9-13
a. What is the transfer function?
b. Design a circuit with that frequency response.

Problem 3.9

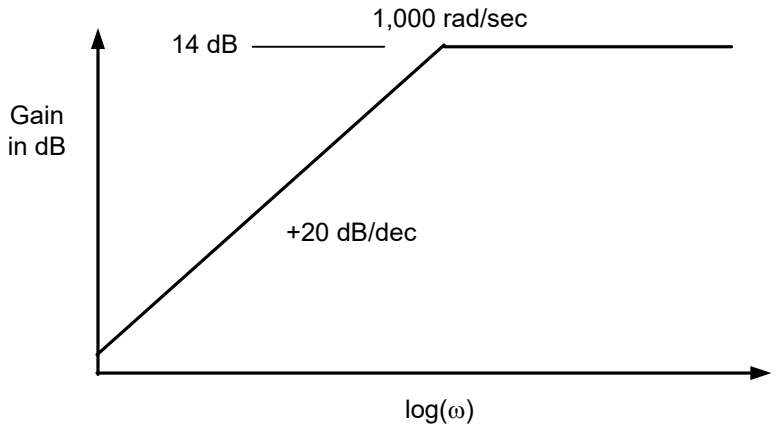


Figure P3.9

Problem 3.10

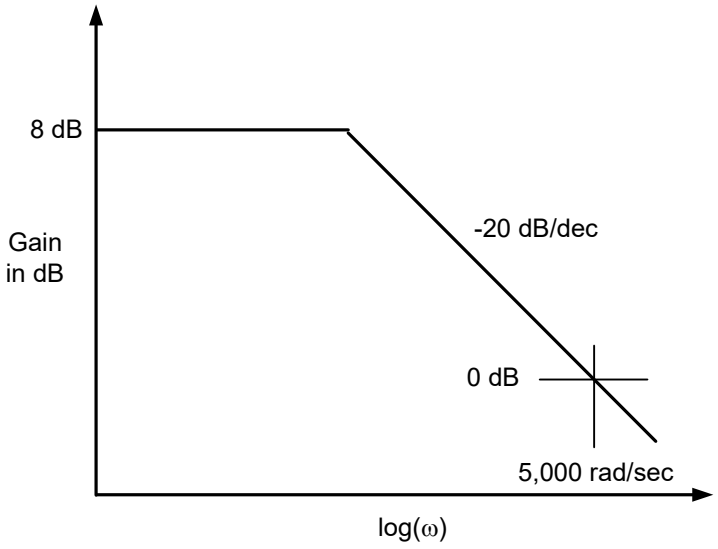


Figure P3.10

Problem 3.11

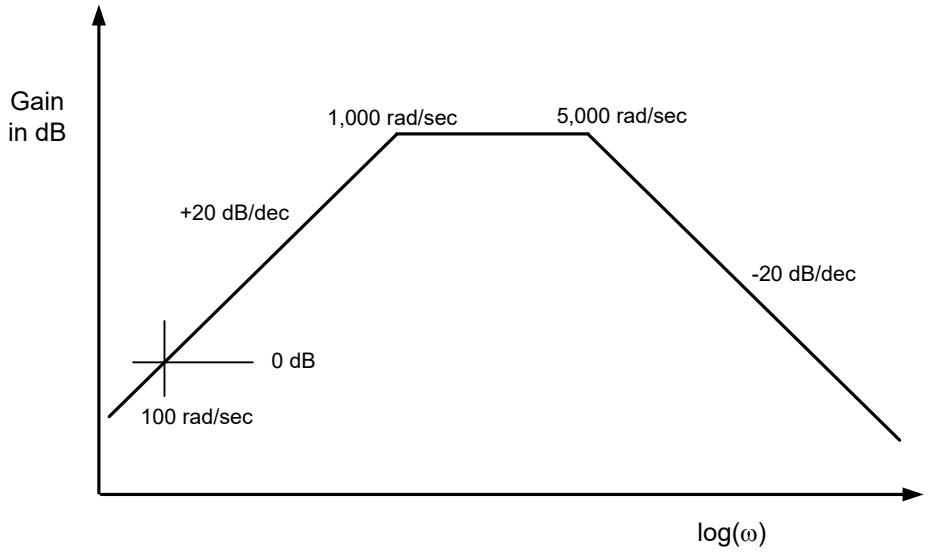


Figure P3.11

Problem 3.12

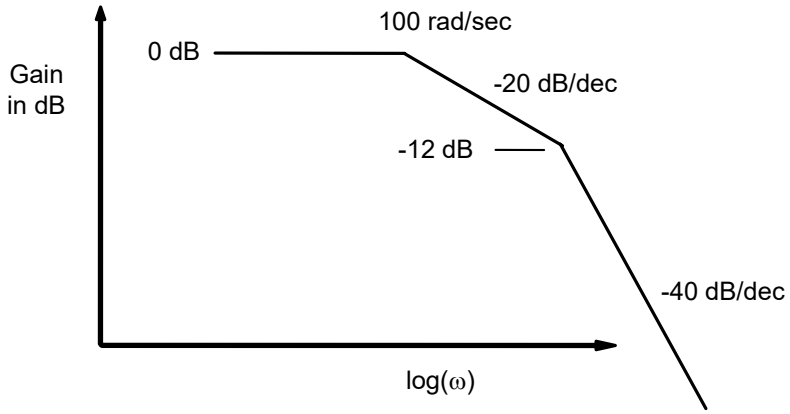


Figure P3.12

Problem 3.13

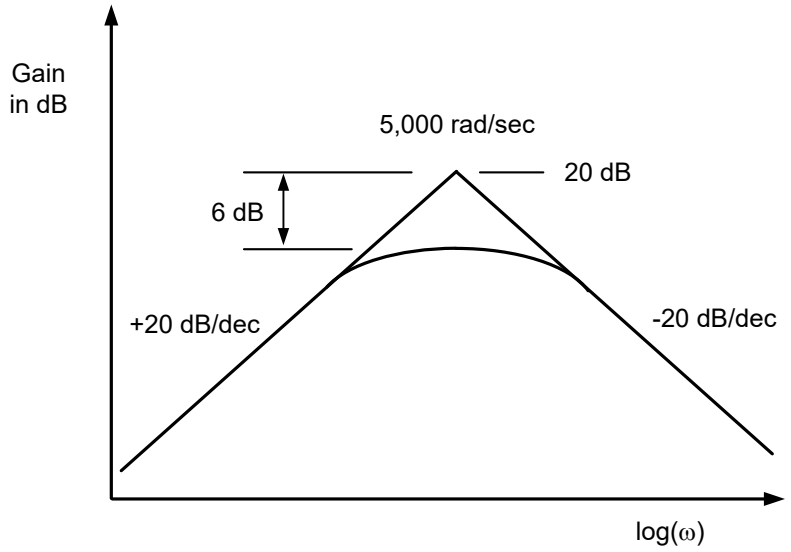


Figure P3.13

3.14 Design a biquad filter with the magnitude response plotted in Figure P3.14.

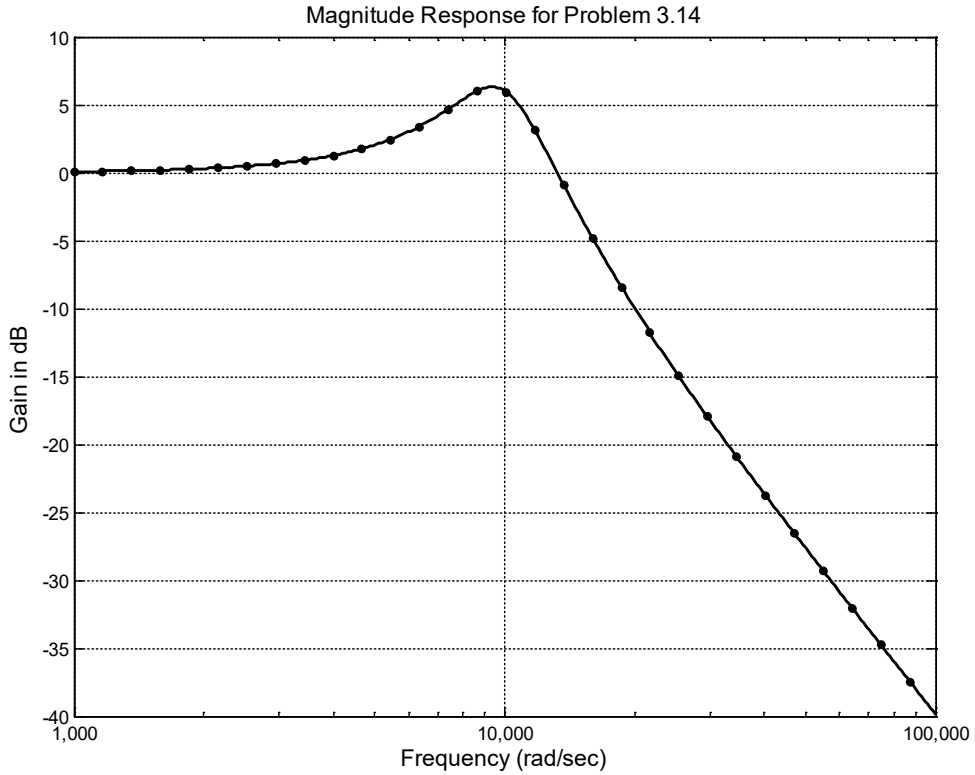


Figure P3.14

3.15-16 Estimate the transfer function and plot the frequency response of the circuits below. Assume the op-amps used have a gain bandwidth product of 1 MHz, zero output impedance, and infinite input impedance.

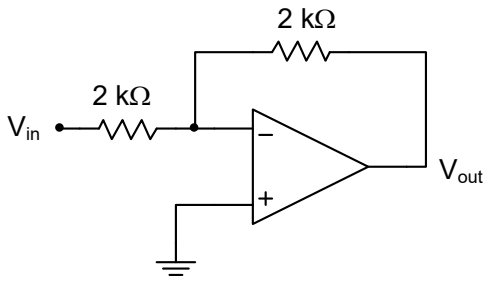


Figure P3.15

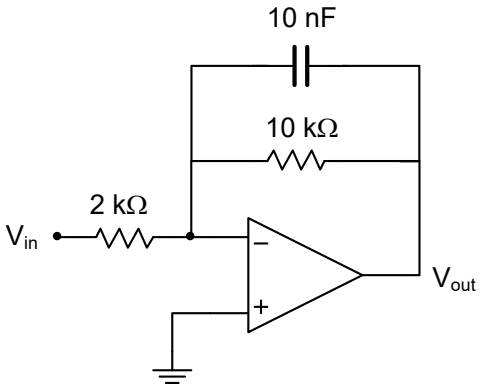


Figure P3.16

3.17 Estimate the DC closed loop output resistance and the DC input resistance for the circuit below. Assume the op-amp has open loop DC gain of 10^6, output resistance of 10 Ω and differential input resistance of 10 MΩ.

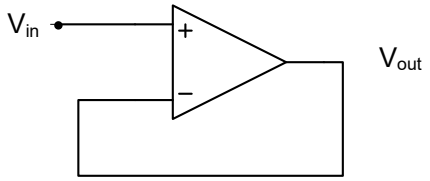


Figure P3.17

3.18 It is desired to design a single stage non-inverting amplifier with a gain of 26 dB and a bandwidth of 500 kHz. The amplifier should be able to amplify (linearly) sinusoidal inputs of up to 0.5 volts in amplitude. Estimate the minimum gain bandwidth product and slew rate specifications of the op-amp.

3.19 Design a circuit with a gain of +10 where $V_{in} = 0$ results in $V_{out} = 0$ even if I_{bias} is large. Assume $I_{bias} >> I_{offset}$.

3.20-22 Analyze the stability of the illustrated circuits. Assume the op-amp has a gain bandwidth product of 1 MHz and the input and output impedances can be ignored.

a. By explicitly calculating the transfer function.

b. By analyzing the circuit using a linear circuit analysis program.

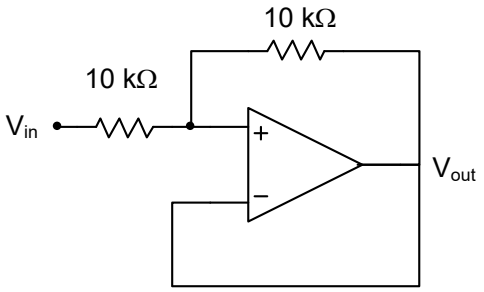


Figure P3.20

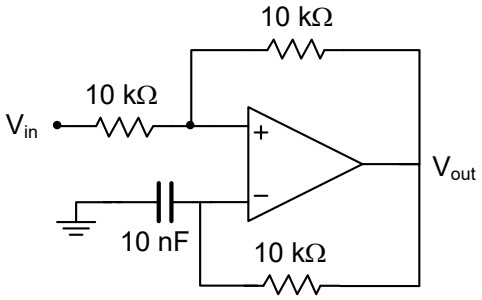


Figure P3.21

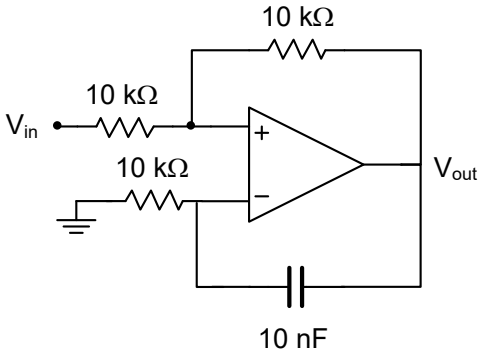


Figure P3.22