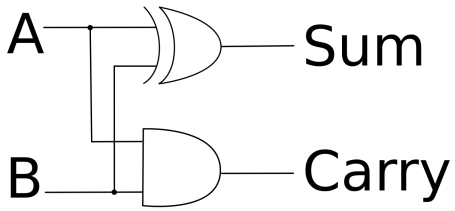
Combinatorial logic

Circuits whose output relies fully on it's current inputs.

1-bit Half Adder

Adds two bits, outputing a sum and a carry.

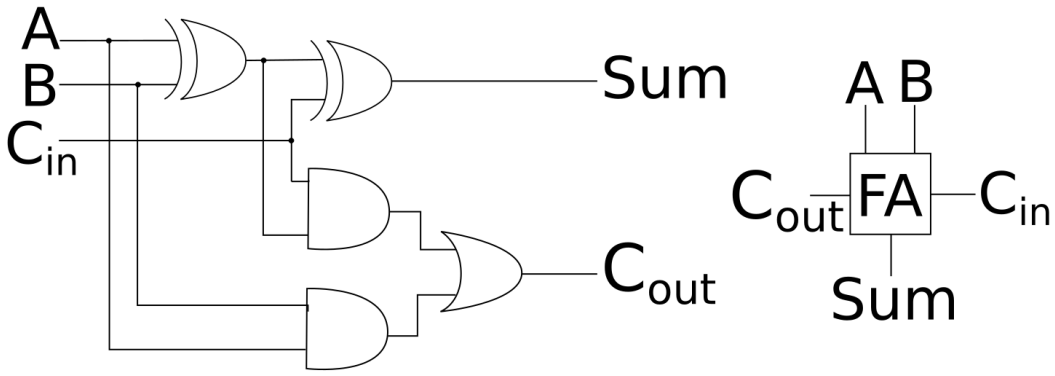
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



1-bit Full Adder

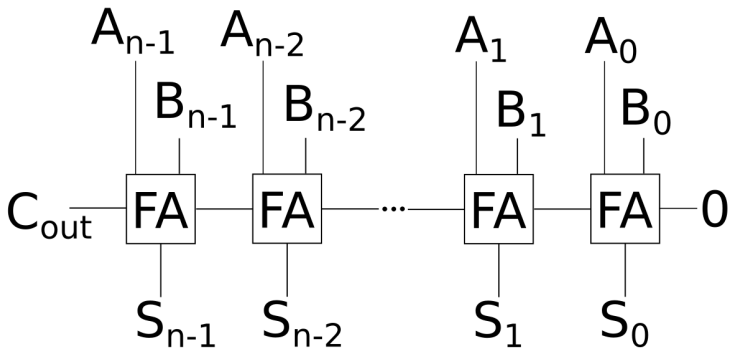
Adds three bits, outputing a sum and carry - can be chained together.

C_{in}	A	B	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



n-bit Full Adder

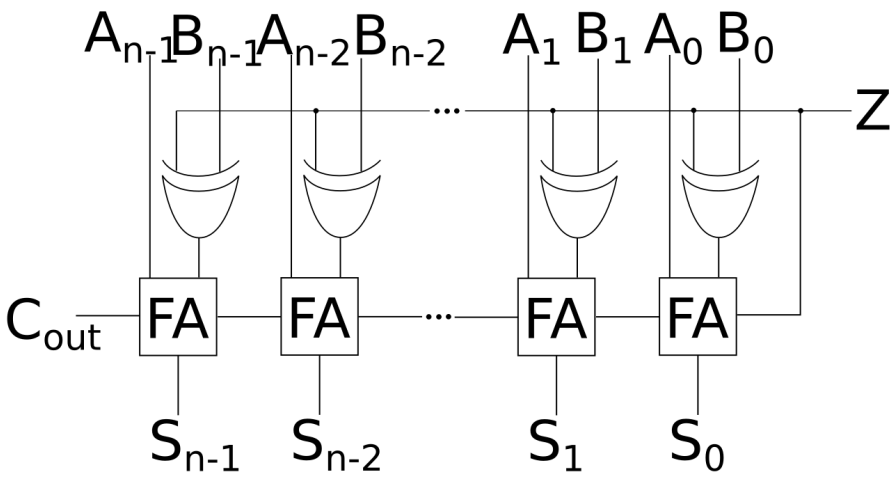
1-bit full adders chained together, to add together two n-bit numbers, A and B.
If C_{out} is high, there has been an overflow.



n-bit Full Adder-Subtractor

Addition to n-bit Full Adder which allows subtraction.
When Z is high, B is effectively turned into negative in two's compliment - bits are inverted, and 1 is added via C_{in}.

Z	Function
0	A+B
1	A-B



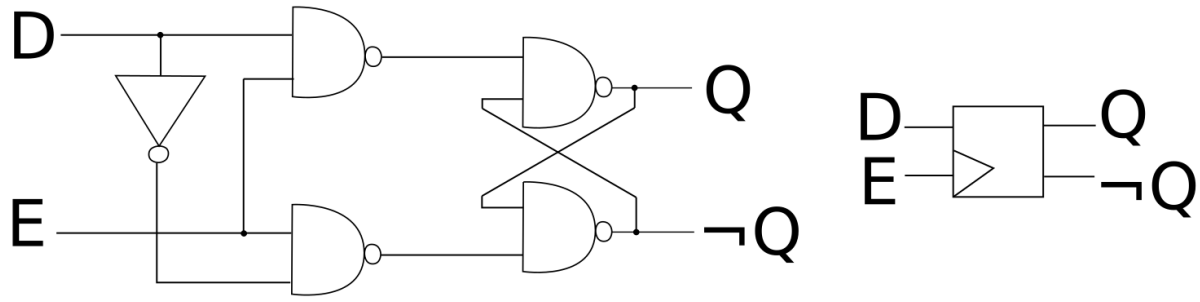
Sequential logic

Logic circuits encorporating a "memory" element, and whose output depends on the prior state.

D-type latch (flip-flop)

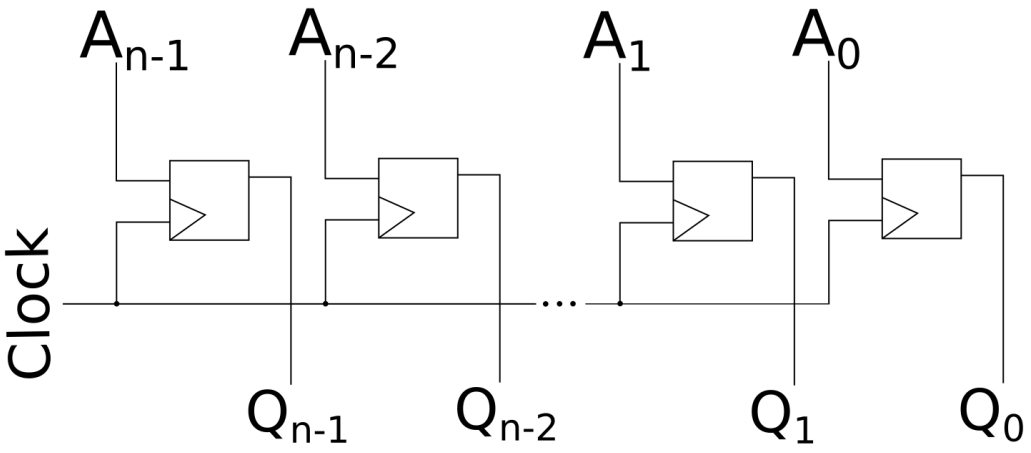
When E is low, the current state is retained. The input at D is "saved" in the latch as the circuit is enabled i.e. when E transitions from 0 to 1. This makes it edge-triggered.

Enable	D	Q	¬Q
0	0	Q	¬Q
0	1	Q	¬Q
1	0	0	1
1	1	1	0



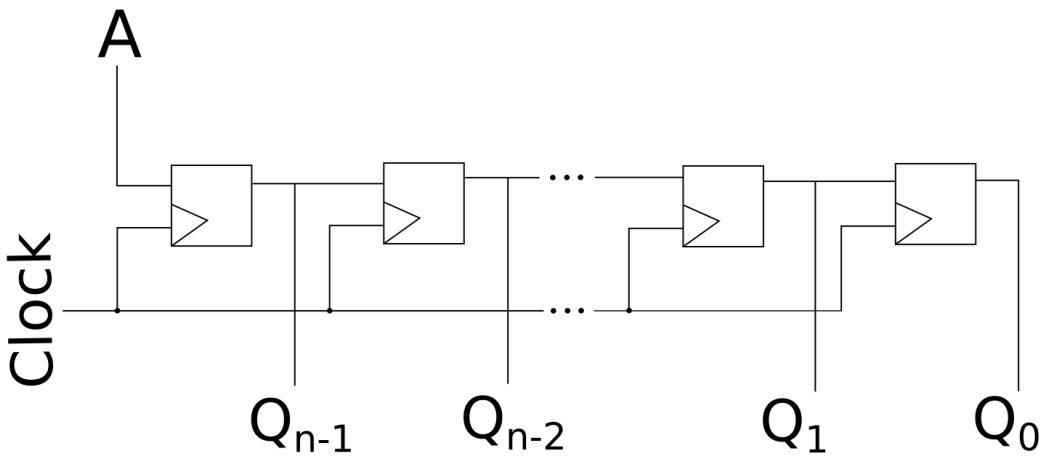
Parallel Load Register

Register requiring a data line for each bit.
On clock enable, the value on A is "saved" to the relevant D-type.



n-bit Shift Register

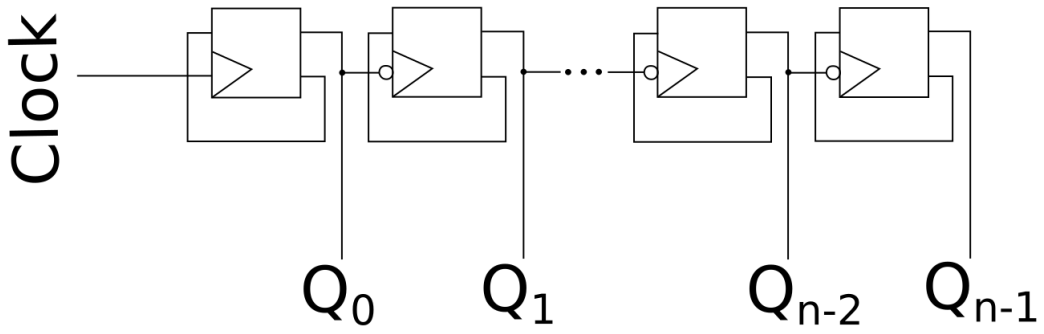
Alternative register requiring only 1 data line.
On clock enable, A is saved to D_{n-1}, D_{n-1} is shifted to D_{n-2}, D_{n-2} is shifted to D_{n-3}, etc.



n-bit Counter

Effectively counts up 1 every clock cycle.
NB. Circles on D-type enable input denote triggered by falling edge i.e. by transition from high to low.

Clock #	Q_0	Q_1	Q_2
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1
7	0	1	1
8	1	1	1



Felix B 2021.