Engineering Sciences 31 • Computer Science 56
DIGITAL ELECTRONICS

Professor: Eric W. Hansen, MacLean M143, 646-2205 / eric.hansen@dartmouth.edu
Office hours: after class; TWTh 2:30-4:30 PM (drop-in); or by appointment (contact Kathy).

Lab director: David Picard, Cummings 006, 646-0774 / David.Picard@dartmouth.edu

Administrative Assistant: Kathy Crowe, MacLean M133, 646-3557 / kathleen.crowe@dartmouth.edu

TAs:

Name	Room	Hours (TBA)
Sarah Pasternak		
Harrison Hall		

Class hours: Lecture — MWF 8:45-9:50 AM, X-hour Th 9:00-9:50 AM, MacLean MB01; X hours will be used for most of the course.

Lab — There will be 4-6 sections Tuesday-Friday. Sign-ups on Monday, June 24. The digital lab is Cummings 011.

Help sessions — TAs will be in the Great Hall M-W evenings to assist you with pre- and post-lab problems.

Text: Frank Vahid, *Digital Design with RTL Design, Verilog, and VHDL* — available from Wheelock Books or online. Also available as an eBook from the publisher, http://www.wiley.com/WileyCDA/WileyTitle/productCd-0470595256,miniSiteCd-ENGINEERING.html

Software: Xilinx *ISE* version 14.4, Digilent *Adept* 2.13.1 (Windows 7 or XP, native or under Parallels), requires at least 1 gigabyte of main memory and about 12 gigabytes of hard disk space — download installers from ThayerFS (see instructions on Blackboard, under "Dartmouth only") before Friday, June 28.

Prerequisites: Engs 20 or CoSc 1 or 5 (*i.e.*, programming experience)

Web page: Blackboard

Learning Objectives

At the end of this course, you will know how to:

1. Create a functional specification of a digital system and translate this description to a "paper" design.
2. Use computer-aided tools for design, simulation, and implementation in programmable logic.
3. Implement a medium-scale digital system efficiently with programmable logic and ancillary components.
4. Do the physical layout of a small-scale system and construct a hand-wired prototype.

5. Debug a digital system using simulation, electronic test equipment, and common sense.
6. Manage a digital design project from concept to working prototype.

Major topics

1. **Combinational logic:** AND, OR, and NOT gates and combinations of them; their functions, and how they are implemented as electronic circuits.

2. **Sequential logic:** Systems having *memory*, which move through a time sequence of logic states. A simple example is a counter.

3. **State Machines:** These are specialized sequential systems for data processing and control. A state machine is at the heart of every digital system, including calculators, computers of all sizes, iPods, cell phones, and more.

4. **Digital processor design:** A digital processor is a *datapath*, which performs a set of basic processing operations (*e.g.,* arithmetic), and a *controller*, a state machine that sequences the datapath operations in the proper order to execute an algorithm.

5. **Contemporary design techniques:** Top-down system design; computer-aided design and simulation; implementation with programmable logic devices.

6. **Project:** Your assignment is to design, justify, build, debug, and document a digital system of moderate complexity. Practical construction techniques and well-known pitfalls will be discussed along the way.

Organization

Grading: This course is graded on the basis of pre-class reading questions, six lab assignments, one exam, and a major project, weighted as follows:

Pre-class questions	5
Labs (6)	30
Exam	30
Project	35

Disabilities: Students with documented physical or learning disabilities (including chronic diseases) needing academic adjustments or accommodations should meet with Prof. Hansen by Friday, June 21. All discussions will remain confidential, although the Academic Skills Center may be consulted to verify the documentation of the disability.

Schedule: See attached.

Nota bene: This course covers a lot of ground and follows a strict schedule. Things simply will not work, for you or for the teaching staff, if you fall behind.

Readings: Daily reading assignments are shown on the course schedule. You are responsible for all the material in each reading, even if I don't cover it in class. Before coming to class (*i.e.,* the night before unless you rise very early), please complete the pre-class reading questions posted on Blackboard. Your responses will assist me in shaping the day's lecture and ultimately benefit

your learning. These surveys will be ungraded, but five percent of your grade is based on the fraction of them that you complete.

Lectures: I intend for the lectures to complement the readings, not duplicate or replace them. From your responses to the pre-class surveys, I hope to learn what you already understand from the reading, and what topics I should spend time on in class with further explanation and examples.

Labs: There are seven labs (0-6) in this course, the first six of which are graded. They are intended to acquaint you with both the theoretical and the practical (hands-on) aspects of digital design. With the exception of Labs 0 and 6, each lab assignment consists of a pre-lab part, an in-lab hands-on part, and a post-lab report that includes additional problems from the textbook or other sources. *Note that most of the post-lab questions take a considerable amount of time and should not be left to the last minute!*

For Labs 1–5, you will work in *pairs*. You and your lab partner will work together in the lab and may collaborate on the pre-lab design and the post-lab writeup. The post-lab will include homework problems in addition to questions about the lab itself.

You and your lab partner will hand in separate reports. Include the name of your lab partner in your report. The honor principle (see below) applies to collaboration with your partner.

During the three-hour lab sections, the members of the teaching staff will be in the lab to help you with construction and testing. *It is normal for the construction and testing phase of a lab to take more than the three hours*, and you may work in the lab at any other time that does not interfere with another scheduled lab. You will get the most out of the lab period if you *complete the pre-lab design work ahead of time*.

Please do not bring food or drink into the Digital Lab, except for drinks in covered cups; there are other common areas in the building more suitable for dining and refreshment. Please clean up after yourself (tools, wire, chips, test equipment). *For your own safety, do not work alone.*

Contemporary digital design is supported by electronic design automation (EDA) software tools. The EDA tools used in this course are installed on the Windows 7 computers in the digital lab, Cummings 011, on several of the Windows computers in MacLean 210, and on the Linux computers in Cummings 218. The software is also available for you to install on your personal computer, if you would like to have it. Plan on needing at least 1 gigabyte of main memory (for the operating system and EDA software) and 12 gigabytes of free hard drive space. It runs under Windows 7 and XP (SP3), and also on Intel Macintosh computers running Windows under either Boot Camp or a virtualization program (I use Parallels, but it should also work with VMware Fusion).

Late Work: Lab reports are due *at the beginning* of the designated lab period. Papers turned in after that will be considered late. A report up to 24 hours late will receive a 10 percent deduction. A report 24-48 hours late will receive a 50 percent deduction. If your report is more than 48 hours late, you will receive a 0 for the assignment. Note that a 0 on a lab assignment corresponds to a 5-point drop in your final course average. Exceptions will be made only if illness or a family emergency has prevented you from completing the assignment on time. If you do not hand in your assignment on time, you are on your honor that you will not look at the solutions until after you have submitted your work.

Exam: The exam is scheduled for the evening of **Monday, July 22 (6-9 PM).** It is a comprehensive examination on the fundamental material covered through Friday, July 19. The exam is closed-book.

Project: This is the most significant part of the course. You will specify, design, build, test, and document a digital system. There are six major milestones in the project: forming project groups, preliminary proposal, datapath design, comprehensive design review, final parts list, and the final demonstration and report. The purpose of these checkpoints is to help you move in an orderly and effective way through the phases of the project.

1. Form your **project group** by **July 8**. The project is to be done in *groups of two*. Your project partner need not be the person you do the labs with, but should be someone you get along well with (you will be spending a lot of time together).

2. The **preliminary proposal** is a functional description of your project — what it does, what switches and lights it has, how a user operates it, etc. You will submit a written proposal on **July 15** and discuss it with the teaching staff that week. This meeting will be about fifteen minutes long.

3. The **datapath** is the core of your comprehensive design. On **July 29**, you will turn in the plan for your datapath.

4. At the **design review** on **August 5-7**, you will meet with the teaching staff to present your complete design (datapath + controller) and answer questions about it. You will hand in a complete paper design where every component is defined and specified. It is likely that you will have already begun building a portion of your project. This meeting will be about thirty minutes long.

5. Your final **parts list** is due on **August 9**, following any revisions recommended made during the design review. This is the last day for which we can guarantee a timely arrival of any parts you order for your project.

6. The **final presentation** is a short (5 minute) description delivered before the entire class (and anyone else who wants to come) on **August 19-21**. Following the description, you will have an opportunity to **demonstrate your working project** at this time**.** As a courtesy to your classmates, please try to attend **all** of the project presentations.

   The **written report**, which consists of a narrative description of the design and a complete set of supporting documents, is due by **3:00 PM on Tuesday, August 27** (end of exam period).

You will receive comments on your technical writing for Checkpoints 2 and 4, and have opportunities for revision and rewriting. Your final report will be graded in part on the writing, including drawings as well as prose style.

Your group will be assigned a locker and can check out tools for the project phase of the course. You are responsible for returning these tools in good order at the end of the course; otherwise, no grade will be sent to the Registrar.

Honor Code: The Honor Principle is an integral part of the academic program at the Thayer School. Consult the ORC (http://dartmouth.smartcatalogiq.com/2012/orc/Regulations/Undergraduate-Study/Academic-Honor) or the Thayer School Student Handbook (http://engineering.dartmouth.edu/graduate/honor.html). Specifically, in Engs 31:

You are encouraged to collaborate on the lab assignments, within reasonable limits. However, when you turn in a paper with your name on it you are saying to me that the final work is yours and that you understand your solution and can explain it to me in a conversation. Copying another person's work is a violation of the Honor Principle and will have serious consequences. It is also a poor way to learn. Remember that you will work alone with no reference materials on the exam, which constitutes 30% of the grade.

Acknowledge your lab and study partners by giving their names on your papers, just as you would acknowledge any other source (such as a book or journal article) outside the usual course readings.

It is not permitted to receive aid from any unauthorized source on an exam, nor is it permissible to give aid to a classmate on an exam.

The project is a collaborative effort of the group members, and the same grade will be assigned to all members of the group.

The Honor Principle extends in the obvious way to library reserve books, computer resources, lab equipment and supplies, and other facilities associated with the course. We expect you to help each other with these things. To hoard, "borrow" without authorization, damage, or in any other way restrict the access of your fellow students to these public resources is clearly in violation of the spirit of the Honor Principle.

Ethical behavior is essential in the professional practice of engineering. The Institute of Electrical and Electronics Engineers has approved a code of ethics that may be read at http://www.ieee.org/portal/pages/iportals/aboutus/ethics/code.html.

References (on reserve in Feldberg Library):

S. Brown and Z. Vranesic, *Fundamentals of Digital Logic with VHDL Design*
R.H. Katz, *Contemporary Logic Design*
V. Pedroni, *Circuit Design and Simulation with VHDL*
D. Perry, *VHDL Programming by Example* (eResource)
C.H. Roth, *Fundamentals of Logic Design*
K. Short, *VHDL for Engineers*
K. Skahill, *VHDL for Programmable Logic*
J.F. Wakerly, *Digital Design: Principles and Practices*

Other reference materials are available in the lab.

How to get the most out of this course

1. Don't fall behind.
2. Come to every class, come on time, and sit where you can see what's going on.
3. Choose your project early, well before the **July 14** proposal deadline. The TAs and I are available to consult.
4. Keep up with the assigned reading and pre-class reading questions.
5. Do the pre-lab design work *before* coming to lab. Don't put off doing the post-lab problems.
6. Talk to me. Ask questions in class, come to office hours, and send email. You can be sure that if you ask about something you don't understand, you are not the only one and someone else in the class will secretly thank you for asking the question. Discuss your graded lab reports with me or a TA to iron out things you have not yet mastered.
7. Have fun. Trust me—you will be amazed at the end of the term at how much you have learned and how cool it all is. Especially if you don't fall behind.