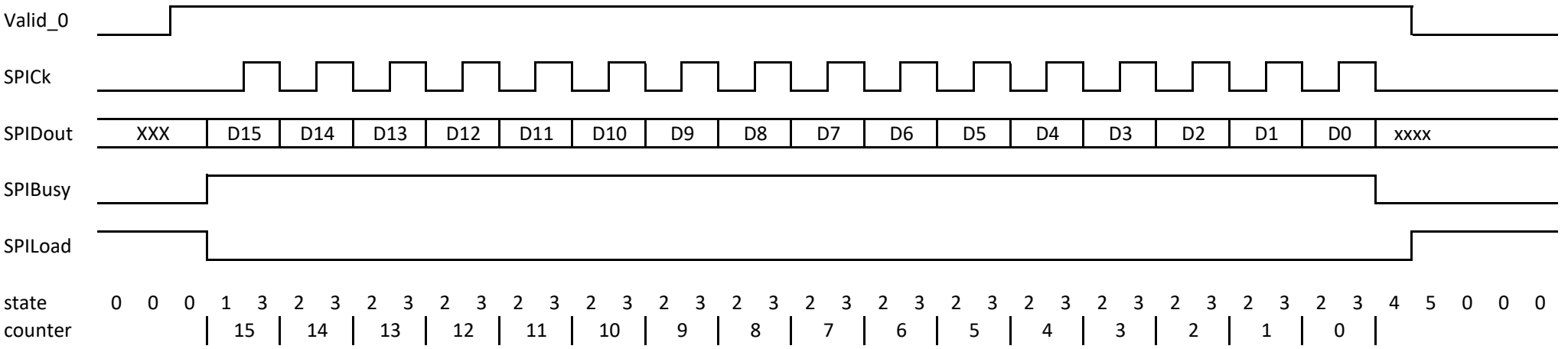
AXI SPI Writer /timing Diagram

"normal" AXI write registers present Valid_0 or Valid_1 bits if a register written.
These bits are cleared when the SPI writer deasserts SPIBusy.
The AXI register interface will not accept another transaction until SPIBusy is cleared.
1st register: signals 16 bit SPI write. Assersts Valid_0
2nd register: signals 32 bit SPI write. Assersts Valid_1
This timing diagram drawn for a 16 bit write.

Timing Diagram



Notes

SPICk target frequency approx 10MHz; divided from master clock.
SPI target device loads data on rising edge of SPILoad. It gets approx 100ns setup time since last shift.
SPIDout is a wire from the shift register

on entry to state 1: load counter; load shift register; assert SPIBusy; Deassert SPILoad
on entry to state 2: shift the register left one place, decrement counter
on entry to state 4: deassert SPIBusy
on entry to state 5: assert SPILoad