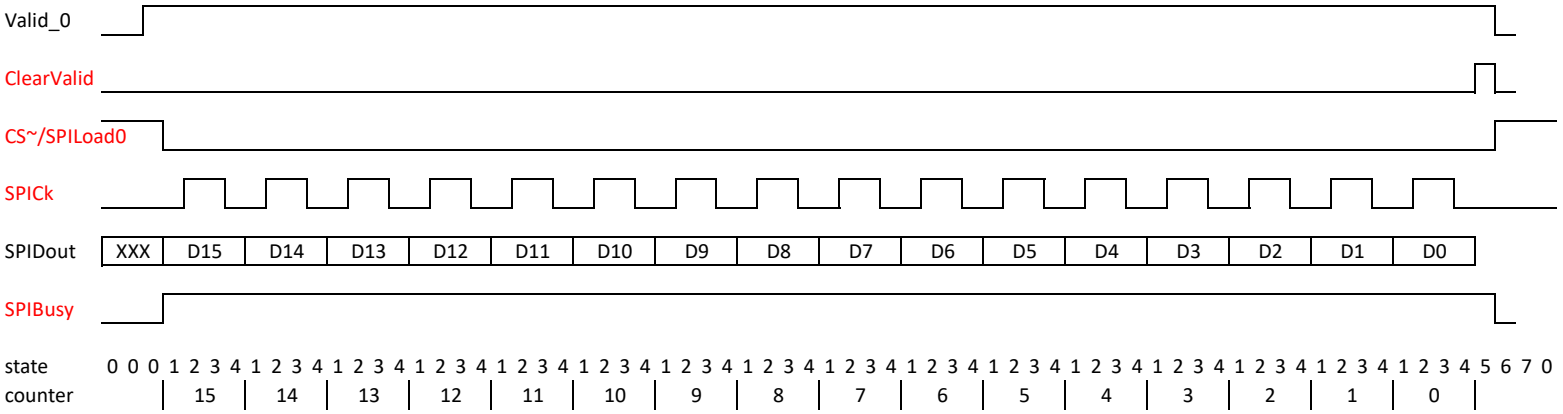
AXI SPI Writer /timing Diagram

"normal" AXI write registers presents Valid_0 bit if a register written.
This bit is cleared when the SPI writer deasserts SPIBusy.
The AXI register interface will not accept another transaction until SPIBusy is cleared.
1st register: signals 16 bit SPI write. Asserts Valid_0
Both CODECs use 16 bit writes.

Timing Diagram



Notes

Valid_0 set by the AXI transfer logic when a register has been written; cleared by ClearValid
SPIBusy is read back through a processor register. 1 if interface busy.
SPICk target frequency approx 10MHz; divided from master clock.
TLV320AIC3204 Codec clocks input data on falling edge of SPI Clock.
TLV320AIC3204 Codec clocks output data on rising edge of SPIClock.
IP should clock data in on falling edge of clock.
TLV320AIC23B Codec clocks input data on rising edge of SPI Clock.
Both Codec loads data on rising edge of SPILoad. It gets approx 100ns setup time since last shift.
SPIDout is a wire from the shift register

on exit from state 0: load counter; load shift register; assert SPIBusy; Deassert SPILoad
on entry to state 2: assert SCLK
on exit from state 4: shift register one place right; decrement counter
on entry to state 4: deassert SCK; shift in input bit & move input SR one place right
on entry to state 4, if counter 0: assert clearvalid
on entry to state 5: deassert clearvalid
on entry to state 6: assert SPILOAD0
on entry to state 6: deassert SPIBusy