Final project

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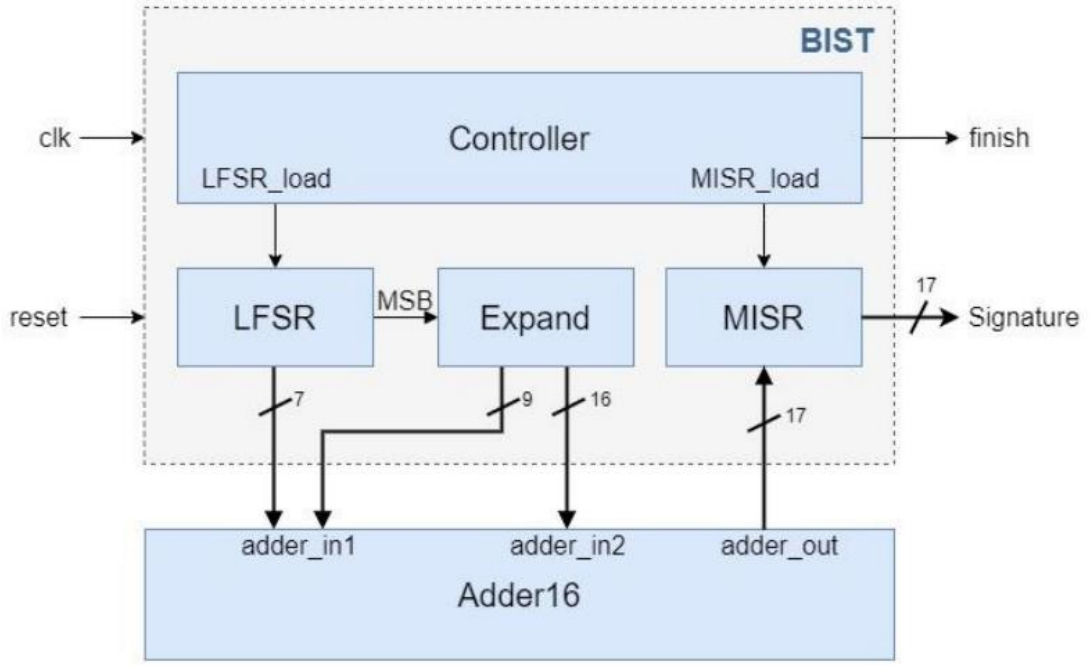
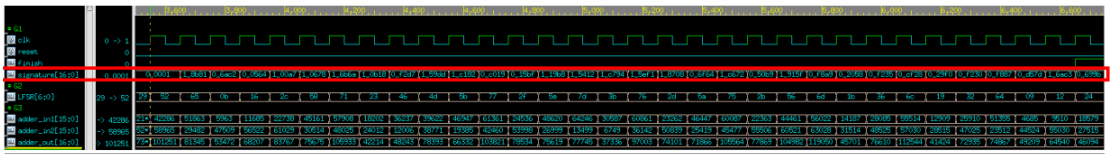
Block diagram:



Golden Signature

1.The golden signature of fault free circuit is “0699b”.



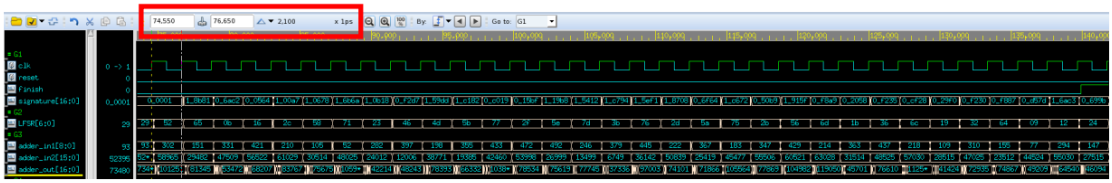
Initial	Pattern0	Pattern1	Pattern2	Pattern3	Pattern4	Pattern5	Pattern6
00001	18b81	06ac2	00564	100a7	10678	16b6a	10b18
Pattern7	Pattern8	Pattern9	Pattern10	Pattern11	Pattern12	Pattern13	Pattern14
0f2d7	159dd	1c182	0c019	015bf	119b8	15412	1c794
Pattern15	Pattern16	Pattern17	Pattern18	Pattern19	Pattern20	Pattern21	Pattern22
15ef1	18708	06f64	1c672	050b9	1915f	0f8a9	02058
Pattern23	Pattern24	Pattern25	Pattern26	Pattern27	Pattern28	Pattern29	Pattern30
0f235	0cf28	029f0	0f230	0f887	0d57d	16ac3	0699b

3. 1GHz Verification

In Design Complier, I set the clock period to 1ns. In this condition, the signature is “xxxxx”, but the golden signature is “0699b”. From the execution window, we can know that timing violation happens. So, my adder can’t operate at the speed of 1GHz.

4. maximum operating speed

The maximum operating speed of my circuit is 476MHz (clock period = 2.1ns). The simulation waveform is shown below. From the cursor measurement, we can clearly see the clock period is 2.1ns.

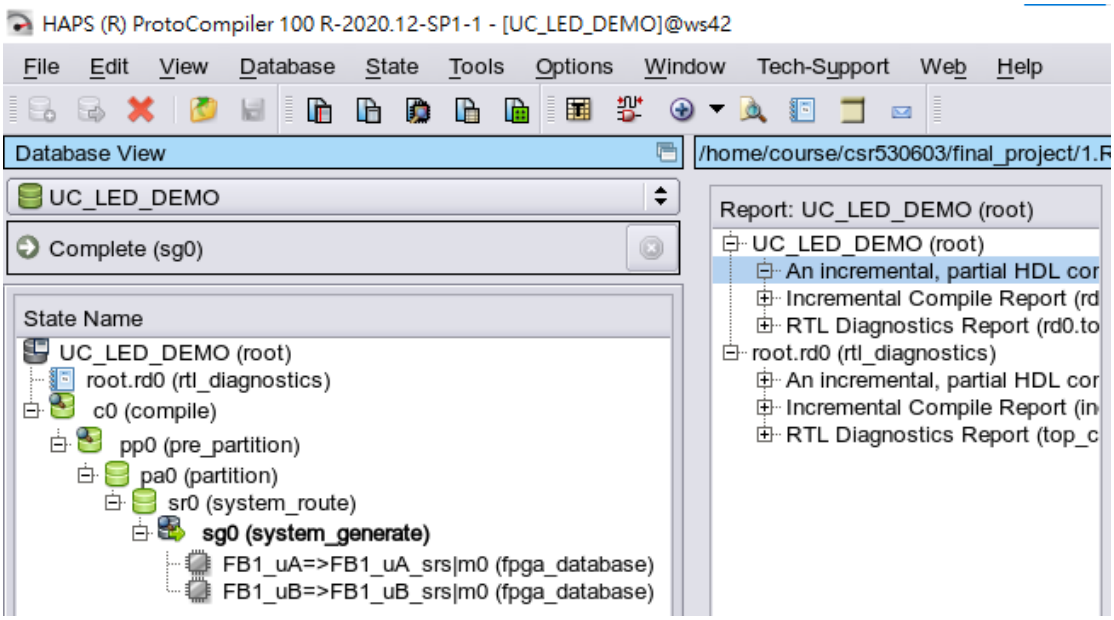


Procedure :

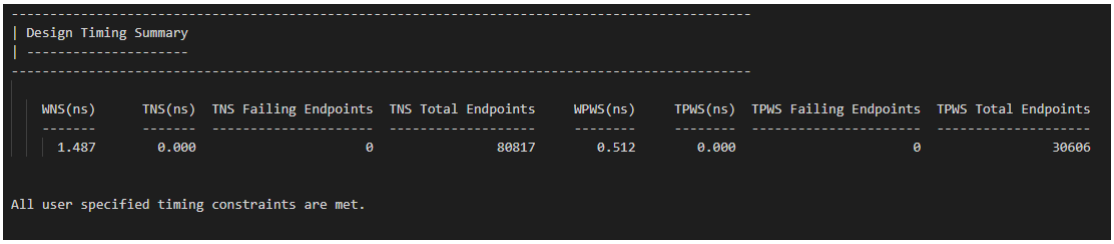
First, I set the clock period to 1ns. From the timing report of design complier shown below, “slack” is -1.08. I guess that my circuit can roughly operate at the clock period of 2.08ns (1+1.08=2.08). Then, I set the clock period to 2.1ns and 2.0ns respectively. Only at clock period 2.1ns, the signature is at the same as golden signature. So the maximum operating speed of my circuit is 476MHz

Now, we use haps to realize “FPGA Design and Implementation Flow”, “FPGA Verification Flow” , “FPGA Prototyping Flow” and “improve Debug Capability”

Using HAPS complete screenshot



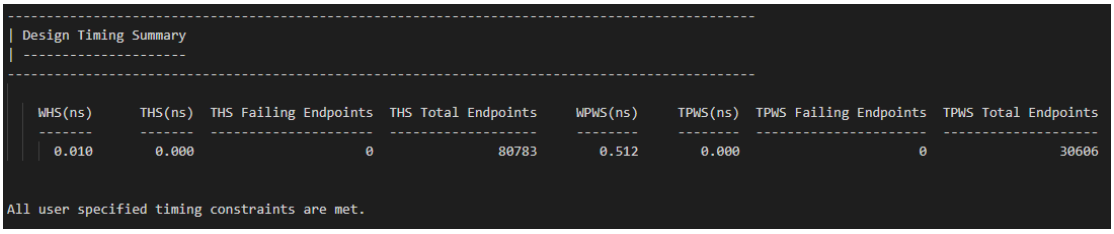
Design Timing Summary(slack meet)



Design Timing Summary

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
1.487	0.000	0	80817	0.512	0.000	0	30606

All user specified timing constraints are met.



Design Timing Summary

WHS(ns)	THS(ns)	THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
0.010	0.000	0	80783	0.512	0.000	0	30606

All user specified timing constraints are met.