| | Chisel_P1 Spec | Status/Errata |
|---|---|---|
| Instruction set | RV32IMAC | ✓ |
| Privilege levels | machine, user | ✓ |
| Memory management | No | ✓ |
| Physical memory prot | No | ✓ |
| Compliance tests | https://github.com/riscv/riscv-tests | ✓ |
| | rv32u{i,m,a,c}-p, rv32mi-p | ✓ no failures |
| Operating system | FreeRTOS | ✓ no known issues |
| Pipeline stages | 5 | ✓ |
| Default GFE clock MHz | 50 | ✓ |
| Max GFE clock MHz | 150 | ✓ |
| Superscalar | No | ✓ |
| Out-of-order | No | ✓ |
| ICache/DCache | 4 KB | ✓ |
| Multiply-Divide unit | Yes | ✓ |
| Single/double FPU unit | No | ✓ |
| RISC-V debug module | RISC-V External Debug Support v0.13<br>system bus | ✓ |
| Interrupts (PLIC) | Chapter 8, SiFive U54-MC-RVCoreIP v1p0<br>16 interrupts | ✓ no known ssues |
| Timer (CLINT) | Chapter 9, SiFive U54-MC-RVCoreIP v1p0 | ✓ no known ssues |
| System bus | 64-bit AXI4 | ✓ no known ssues |
| Implementation language | Chisel | ✓ |