Release 1 GFE Hardware Description

1 CAPABILITIES, SYSTEM AND COMPONENTS

Figure 1 shows a block diagram of the Release 1 GFE hardware. The system in the XCVU9P runs bare-metal code. A host-based gdb debugger connects to the system over the USB/JTAG connector, and a host-based console connects over the USB/UART connector. The P1 system can access 1 GB of the 4GB on-board DRAM through the Xilinx DDR controller and phy.

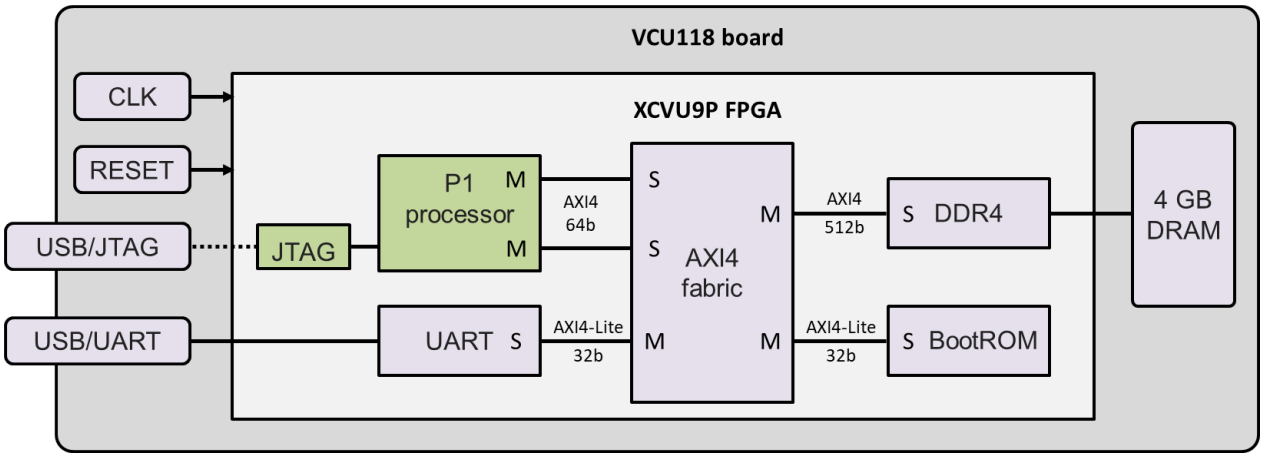

Figure 1: GFE P1 VCU118 FPGA board and device block diagram

The GFE system consists of a Rocket or Piccolo RISC-V core (see specifications below), JTAG controller, UART controller, DDR4 controller and BootROM. All components but the P1 processors and the JTAG block (green) are Xilinx IP (purple). The BootROM is a read only memory constructed from a BRAM and AXI BRAM controller. The GFE system is the same whether the processor is Rocket or Piccolo.

The P1 processors include Debug Modules (not shown) that connect to the custom JTAG block (https://gitlab-ext.galois.com/ssith/gfe/tree/master/jtag) that uses Xilinx BSCAN primitives under the hood. This enables a tap

into the FPGA's JTAG system controller to multiplex the P1 JTAG channel onto the external USB/JTAG port (dotted line connection).

The components are connected through an AXI4 fabric with 5 ports. The fabric automatically translates between protocols (AXI4-Lite and AXI4) and channel widths (32, 64, 256 bit).

See section "Xilinx UltraScale+ Implementation" for the Xilinx circuit implementation of this block diagram.

Table 1 lists the Xilinx IP cores used in the GFE system:

Component	Product	Documentation
AXI Interconnect	PG059	https://www.xilinx.com/support/documentation/ip_documentation/axi_interconnect/v2_1/pg059-axi-interconnect.pdf
DDR4 Controller	PG150	https://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/v1_4/pg150-ultrascale-memory-ip.pdf
AXI BRAM Controller	PG078	https://www.xilinx.com/support/documentation/ip_documentation/axi_bram_ctrl/v4_0/pg078-axi-bram-ctrl.pdf
AXI UART 16550	PG143	https://www.xilinx.com/support/documentation/ip_documentation/axi_uart16550/v2_0/pg143-axi-uart16550.pdf

Table 1

2 P1 PROCESSOR SPECIFICATIONS

	Rocket	Piccolo
Instruction set	RV32IMAC	RV32IMAC
Privilege levels	Machine, User	Machine, User
Memory management	No	No
Pipeline depth	5	3
Default GFE clock MHz	83	83
Max GFE clock MHz	150	83
Superscalar	No	No
Out-of-order	No	No
ICache/DCache	4 KB	4 KB
Multiply-Divide unit	Yes	Yes
Single/double FPU unit	No	No
RISC-V debug module	Yes	Yes
Interrupts	1	1
Time (CLINT)	Yes	Yes
System bus	64-bit AXI4	64-bit AXI4
Operating system	FreeRTOS	FreeRTOS
Implementation language	Chisel	BSV

"Default GFE clock MHz" is the current frequency setting for the ACLK signal (see Figures 2 and 3) that clocks all GFE components except the DDR4 controller. ACLK is generated by the clock generator inside the DDR4 controller (for convenience, not necessity). The ACLK frequency can be modified by adjusting the advanced clocking settings of the DDR controller.

"Max GFE clock MHz" is the maximum clock frequency at which the GFE has been tested with Rocket and Piccolo.

For Rocket, it may be possible to run faster than 150 MHz if the rest of the system can keep up (this hasn't been tried). For Piccolo, the GFE clock frequency is currently limited by Piccolo, not the rest of the system.

3 XILINX ULTRASCALE+ DESIGN IMPLEMENTATION

The block diagram in Figure 1 is implemented using Vivado's IP Integrator design flow:
https://www.xilinx.com/content/dam/xilinx/support/documentation/sw_manuals/xilinx2018_3/ug995-vivado-ip-subsystems-tutorial.pdf

The IP Integrator enables quick and easy graphical connections of Xilinx IP that is instantiated and configured within an IP Integrator project session. In addition, the P1 processors are imported into IP Integrator as 3rd party reusable IP blocks that can be connected as easily as Xilinx IP.

The top-level GFE system is a Vivado *block design*. It consists of three instances (Figure 2): a Xilinx JTAG module (*xilinx_jtag_0*) and a P1 processor (*mkP1_Core_0*) that correspond to blocks in Figure 1; and a subsystem module (*gfe_subsystem*) that instantiates all the other Xilinx modules.

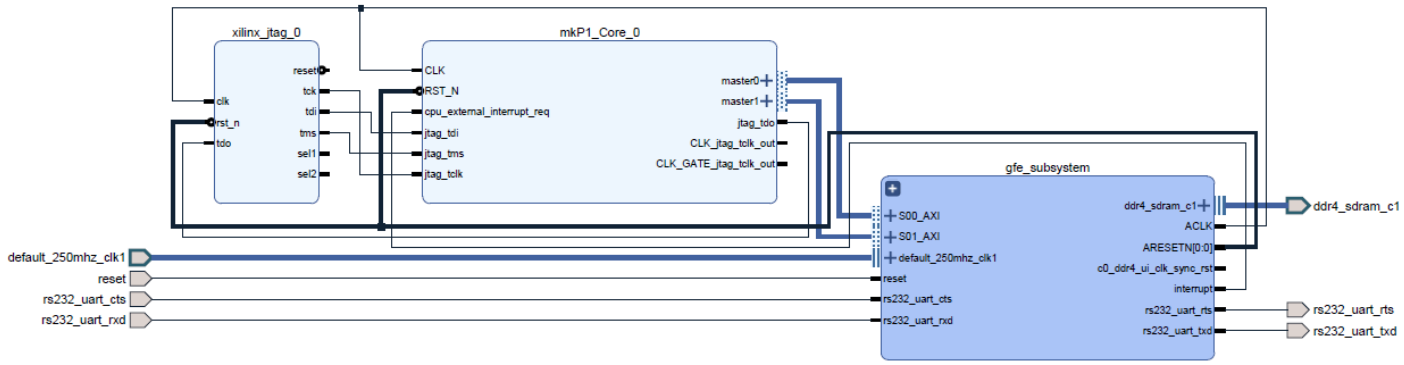

Figure 2: Top-level Vivado block design for GFE P1

The *gfe_subsystem* module is shown in Figure 3. It instantiates all the Xilinx cores that are necessary to implement the fabric, UART, DDR4 controller and BootROM in Figure 1. In addition, it instantiates two blocks to implement reset.

The memory map for the BootROM, UART and DDR4 can be viewed in the "Address Editor" tab next to the "Diagram" tab in the Vivado GFE project window:

Cell	Slave Interface	Base Name	Offset Address	Range	High Address
mkP1_Core_0					
master0 (64 address bits : 16E)					
gfe_subsystem/axi_bram_ctrl_0	S_AXI	Mem0	0x0000_0000_7000_0000	4K	0x0000_0000_7000_0FFF
gfe_subsystem/axi_uart16550_0	S_AXI	Reg	0x0000_0000_6230_0000	4K	0x0000_0000_6230_0FFF
gfe_subsystem/ddr4_0	C0_DDR4_S_AXI	C0_DDR4_ADDRESS_BLOCK	0x0000_0000_8000_0000	1G	0x0000_0000_BFFF_FFFF
master1 (64 address bits : 16E)					
gfe_subsystem/axi_bram_ctrl_0	S_AXI	Mem0	0x0000_0000_7000_0000	4K	0x0000_0000_7000_0FFF
gfe_subsystem/axi_uart16550_0	S_AXI	Reg	0x0000_0000_6230_0000	4K	0x0000_0000_6230_0FFF
gfe_subsystem/ddr4_0	C0_DDR4_S_AXI	C0_DDR4_ADDRESS_BLOCK	0x0000_0000_8000_0000	1G	0x0000_0000_BFFF_FFFF

Note that the first UART register is at 0x62300000, not 0x62301000 as the UART documentation would suggest. This is a result of the small address space allocated to UART in the Xilinx interconnect. The interconnect allocates 0x62300000-0x62300fff to UART, but the UART registers in the Xilinx documentation are defined at 0x6230100X. Synthesis causes the upper bits to be ignored within the UART block, so the resulting UART registers are located at 0x6230000X

Our reference code uses the proper addresses (0x6230000X). Writing to and reading from 0x6230100X causes undefined behavior (this is processor dependent).

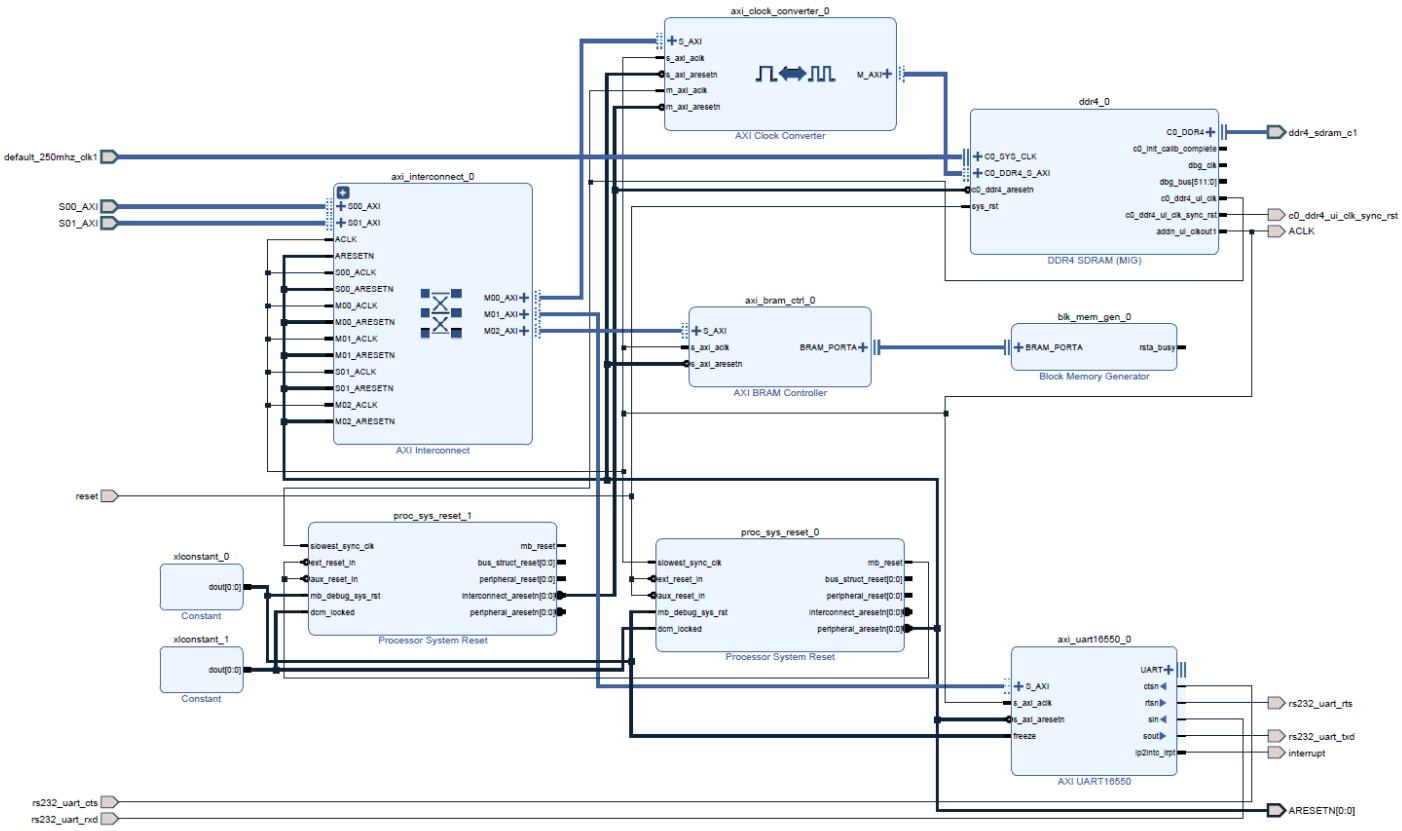

Figure 3: Xilinx block design implementation for *gfe_subsystem*