

# CHERI Documentation Roadmap

Version 1.1

This interim document is not released for public consumption

Robert N. M. Watson, Peter G. Neumann  
SRI International and the University of Cambridge\*

March 5, 2014

This document is a guide to technical reports and notes released by the CTSRD Project.

## 1 Core technical reports

### *CHERI Architecture Document*

This report describes the CHERI processor approach, core architecture, instruction-set architecture (ISA), and programming model.

### *BERI Hardware Reference*

This report describes the current implementation status of the BERI and CHERI ISAs, the BERI implementation, Bluespec-based simulation, synthesis to Altera FPGAs (including those on the Terasic DE4 board), peripherals (such as the BERI PIC, but also flash storage, etc), the BERI processor debug unit, and BERI unit-test suite.

### *BERI Software Reference*

This report describes the software development environment on BERI, with a particular focus on building and using FreeBSD/BERI.

### *CHERI User's Guide*

This report describes the CHERI software development environment – especially, differences between FreeBSD/BERI and CheriBSD, the CHERI-aware clang/LLVM/gas, and the Deimos micro-kernel. This document is intended to supplement the *BERI Software Reference*, which contains all material common to FreeBSD/BERI and CheriBSD (e.g., how to cross-build the OS and prepare disk images).

---

\*Sponsored by the Defense Advanced Research Projects Agency (DARPA) and the Air Force Research Laboratory (AFRL), under contract FA8750-10-C-0237. The views, opinions, and/or findings contained in this report are those of the authors and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

### *CHERI Formal Methods Report*

This report describes formal methods activities associated with the CHERI processor, including ISA modelling and work to import descriptions of the processor into PVS.

## **2 Supplementary developer documentation**

### *CHERI ISA Quick Reference*

This document provides a single-sheet reference to the CHERI ISA, including CHERI capability-coprocessor instructions and their encodings.

### *Using the PVS specification of the CHERI capability coprocessor*

This technical note describes how to verify CHERI ISA security proofs using SRI's PVS tool.

### *CheriCloud Architecture*

This technical note describes the CheriCloud remote access and development facility for CHERI-based prototypes.

## **3 Demonstration notes and guides**

### *CHERI DE4 Factory Install Guide*

This document describes the process of bootstrapping or recovering CHERI demonstration hardware based on the Terasic DE4 board.

### *CHERI DE4 Getting Started Guide*

This document is a guide to the CHERI DE4 tablet demonstration platform, including a tour of the demonstration and supporting maintenance activities (e.g., firmware upgrades).