CHERI ISA Quick Reference 1.1 - March 16, 2013

Capability Inspection Instructions

31–26	25–21	20–16	15–11	10–3	2–0	
0x12	0x08	cd	offset			BC2F cd, offset
0x12	0x00	rd	cb		0x0	CGetPerm rd, cb
0x12	0x00	rd	cb		0x1	CGetType rd, cb
0x12	0x00	rd	cb		0x2	CGetBase rd, cb
0x12	0x00	rd	cb		0x3	CGetLen rd, cb
0x12	0x00	rd	cb		0x5	CGetTag rd, cb
0x12	0x00	rd	cb		0x6	CGetUnsealed rd, cb
0x12	0x00	rd	cd		0x7	CGetPCC rd(cd)

Capability Modification Instructions

31–26	25–21	20–16	15–11	10–6	5–3	2–0	
0x12	0x04	cd	cb	rt		0x0	CAndPerm cd, cb, rt
0x12	0x04	cd	cb	rt		0x1	CSetType cd, cb, rt
0x12	0x04	cd	cb	rt		0x2	CIncBase cd, cb, rt
0x12	0x04	cd				0x3	CSetLen cd, cb, rt
0x12	0x04	cd	cb	rt		0x5	CClearTag cd

Permission Flag Bits

Bit	Name
0	Non Ephemeral
1	Permit Execute
2	Permit Load
3	Permit Store
4	Permit Load Capability
5	Permit Store Capability
6	Permit Store Ephemeral
7	Permit Seal
8	Permit Set Type
9	Reserved
10	Access EPCC
11	Access KDC
12	Access KCC
13	Access KR1C
14	Access KR2C
15	Reserved

Register Usage

Register	Alias	Use
C0		Base for MIPS operations
C1		First argument, return value
C2-C4		Next three arguments
C5-C15		Caller-save registers
C16-C24		Callee-save registers
C25		Not preserved across exceptions
C26	IDC	Invoked data capability
C27	KR1C	Reserved for kernel use
C28	KR2C	Reserved for kernel use
C29	KCC	Kernel code capability
C30	KDC	Kernel data capability
C31	EPCC	PCC in trap handlers

Memory Access Instructions

31–26	25–21	20–16	15–11	10–3	2	1–0	
0x3e	cs	cb	rt	offset			CSC cs, rt, offset(cb)
0x36	cs	cb	rt	offset			CLC cd, rt, offset(cb)
0x32	rd	cb	rt	offset	s	t	CL*x* rd, rt, offset(cb)
0x32	rd	cb	rt	offset	1	0	CLB rd, rt, offset(cb)
0x32	rd	cb	rt	offset	1	1	CLH rd, rt, offset(cb)
0x32	rd	cb	rt	offset	1	2	CLW rd, rt, offset(cb)
0x32	rd	cb	rt	offset	1	3	CLLD rd, rt, offset(cb)
0x32	rd	cb	rt	offset	0	0	CLBU rd, rt, offset(cb)
0x32	rd	cb	rt	offset	0	1	CLHU rd, rt, offset(cb)
0x32	rd	cb	rt	offset	0	2	CLWU rd, rt, offset(cb)
0x32	rd	cb	rt	offset	0	3	CLD rd, rt, offset(cb)
0x3a	rs	cb	rt	offset	e	t	CS*x* rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	0	0	CSB rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	0	1	CSH rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	0	2	CSW rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	0	3	CSD rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	1	0	CSBH rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	1	1	CSHH rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	1	2	CSWH rs, rt, offset(cb)
0x3a	rs	cb	rt	offset	1	3	CSCD rs, rt, offset(cb)

Control Flow Instructions

31–26	25–21	20–16	15–11	10–6	5–0	
0x12	0x08		cb	rt		CJR rt(cb)
0x12	0x07		cb	rt		CJALR rt(cb)
0x12	0x02	cd	cs	ct		CSealData cd, cs, ct
0x12	0x03	cd	cs	ct		CUnseal cd, cs, ct
0x12	0x01	cd	cs			CSealCode cd, cs
0x12	0x05	cs	cb			CCall cs, cb
0x12	0x06					CReturn