field effect transistor
impendance amplifiers, microwave
desirably higher input impedance than bipolar transistors which allows the input of a FET to be
easily matched to the standard microwave system. The FET has a negative temperature at high
current lives; that is the current decreases as temperature increases. This characteristic leads to a
more uniform temperature distribution over the device area and prevents the FET from thermal runway
second breakdown which occurs in the bipolar transistor. The device is thermally stable, even
when the active area is large or when many devices are connected in parallel.

Because FETs are unipolar devices, they do not suffer from minority carrier storage effects and consequently have higher switching speeds and higher cut-off frequencies. In addition the devices are basically square-law or linear devices; inter-modulation and cross-modulation products are much smaller.

16.2. Types of Field-effect Transistor

Broadly speaking there are two main types of field effect transistors :

1. Junction field-effect transistor (JFET).
2. Metal oxide semiconductor field-effect transistor (MOSFET) or insulated gate field-effect transistor (IGFET).

Both of these types of FET's can be further sub-divided as shown in Fig. 16.2.

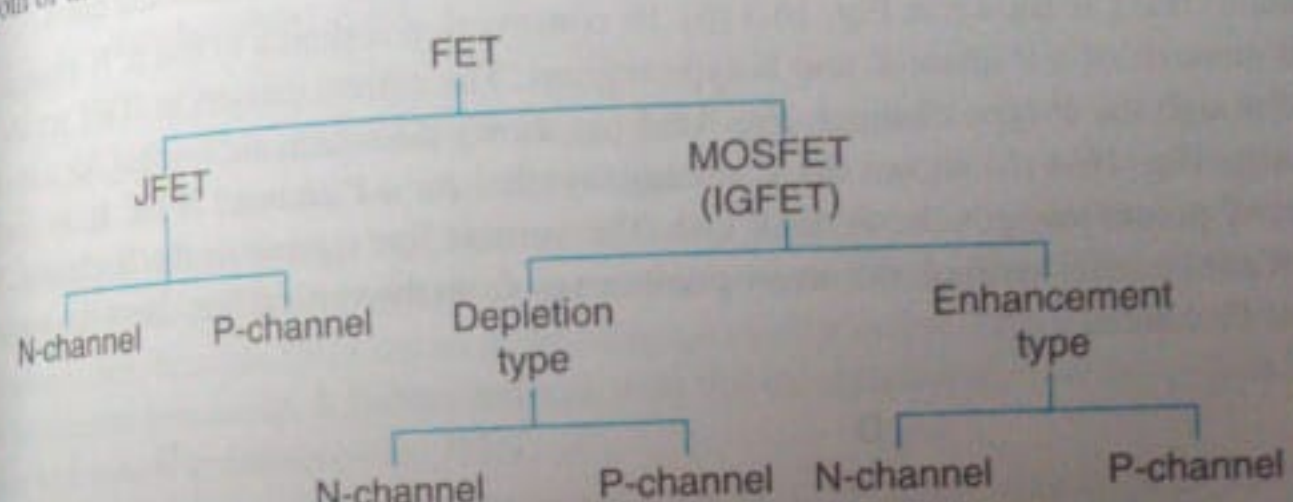


Fig. 16.2.

Now we shall discuss the construction, operation and characteristic of all the above mentioned field-effect transistors in the following pages.

16.3. Junction Field-Effect Transistor

The junction field-effect transistors (JFET's) can be divided depending upon their structure into the following two categories:

1. N-channel JFET and
2. P-channel JFET.

The basic construction of an N-channel JFET is as shown in Fig. 16.3 (*a*). It consists of an N-type semiconductor bar with two P-type heavily doped regions diffused on opposite sides of its middle

part. The P-type regions form two PN junctions. The space between the junctions (*i.e.*, N-type region) is called a channel. Both the P-type regions are connected internally and a single wire is taken out in the form of a terminal called the gate (*G*). The electrical connections (called ohmic contacts) are made to both ends of the N-type semiconductor and are taken out in the form of two terminals called drain (*D*) and source (*S*). The drain (*D*) is a terminal through which electrons leave the semiconductor bar and source (*S*) is a terminal through which the electrons enter the semiconductor.

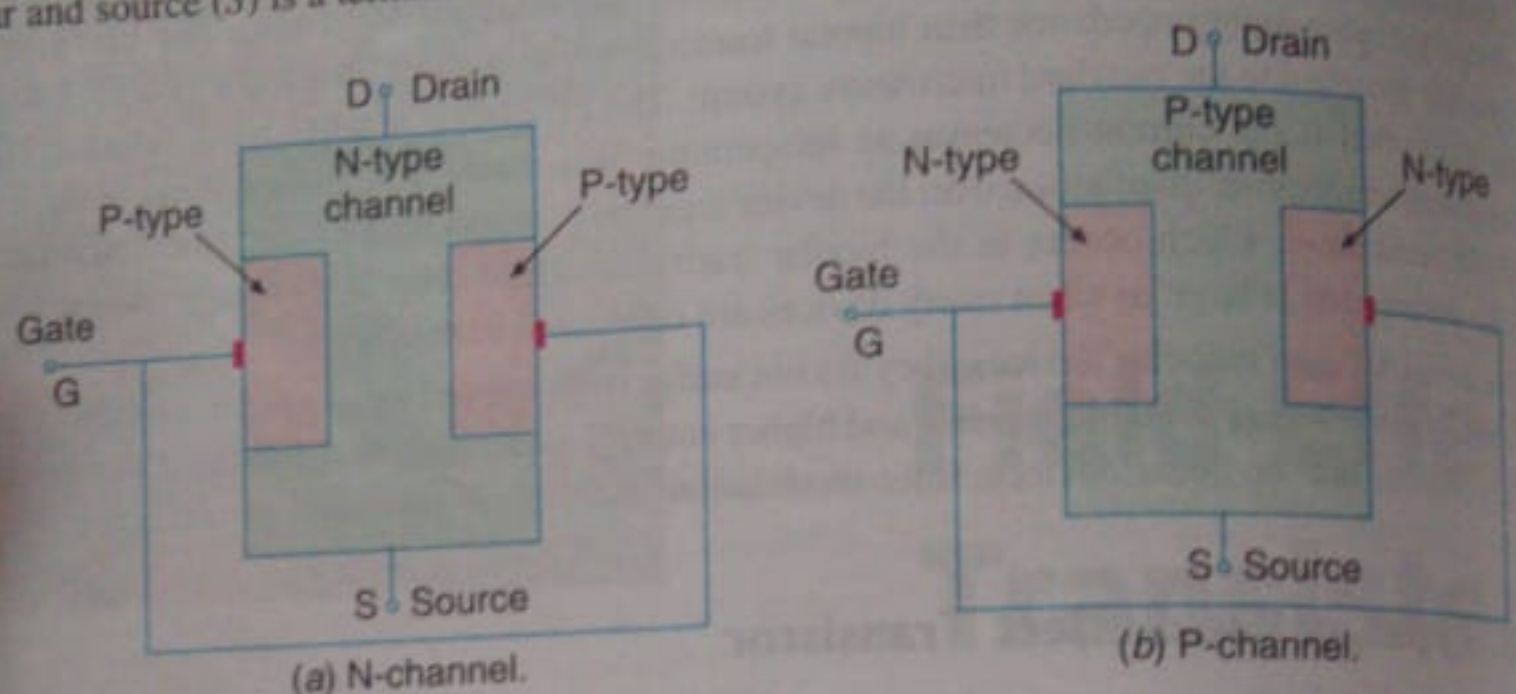


Fig. 16.3. JFET's.

Whenever a voltage is applied across the drain and source terminals, a current flows through the N-channel. The current consists of only one type of carriers (*i.e.*, electrons) Therefore the field-effect transistor (FET) is called a unipolar device. This distinguishes an FET from a BJT (*i.e.*, a bipolar junction transistor) where the current consists of the flow of both the electrons and holes.

A P-channel JFET is shown in Fig. 16.3 (*b*). Its construction is similar to that of N-channel JFET except that it consists of a P-channel and N-type regions. The current carriers in JFET are the holes which flow through the P-type channel. Fig. 16.4 (*a*) shows the schematic symbol for a N-channel JFET. Similarly, Fig. 16.4 (*b*) shows the schematic symbol for a P-channel JFET. In an N-channel JFET, the arrow points towards the vertical line. The vertical line represents the N-channel. On the other hand, in a P-channel symbol, the arrow points away from the vertical line. Here the vertical line represents the P-channel.

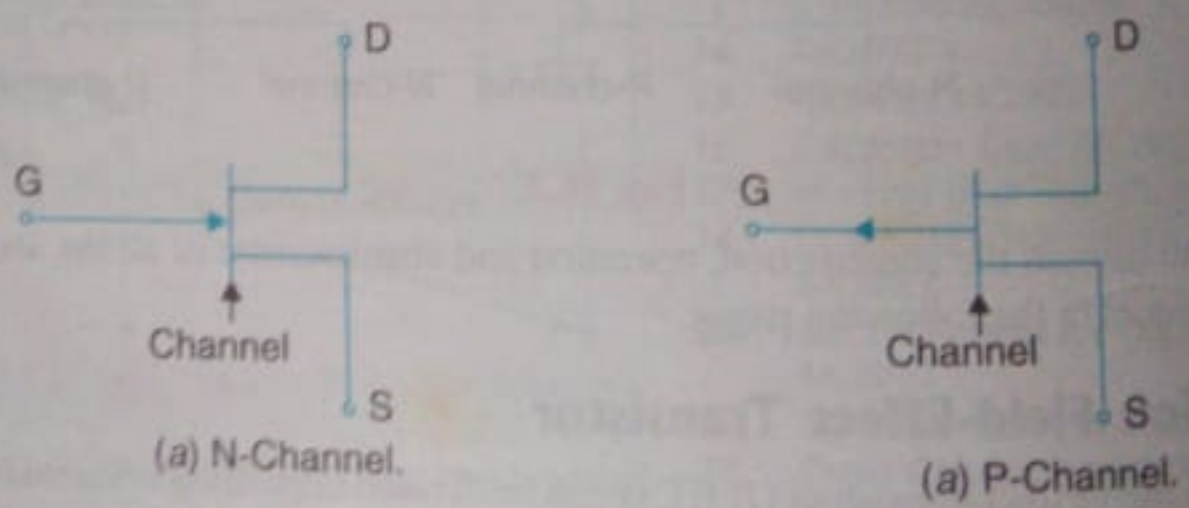


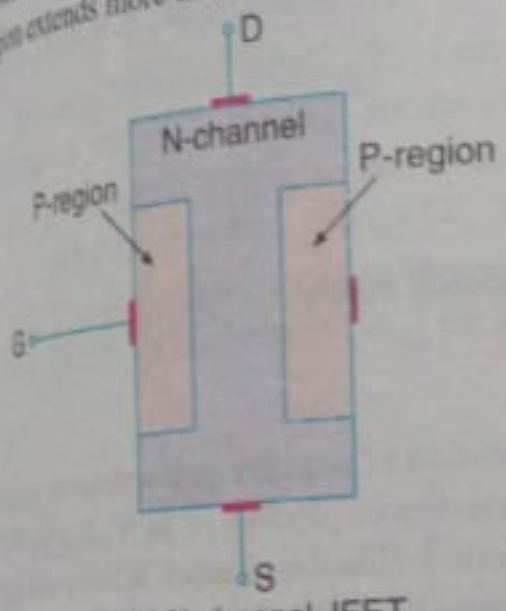
Fig. 16.4. Symbols for JFET's.

Now we shall discuss the operation and characteristics of JFET's with reference to N-channel JFET. The operation of a P-channel JFET is similar to N-channel except that all voltages and currents are reversed.

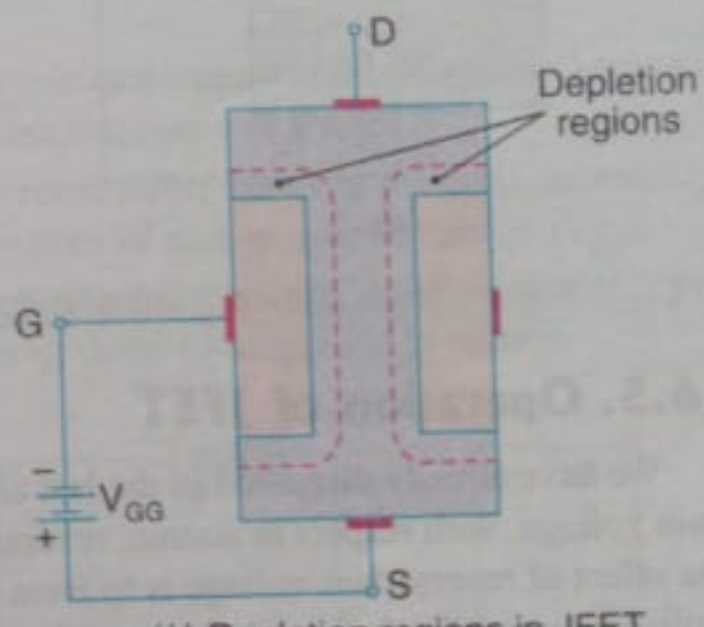
16.4. Formation of Depletion Region in JFET

Consider an N-channel JFET as shown in Fig. 16.5 (*a*). Here the P-type gate and N-type channel constitute PN junction. This PN junction is always reverse biased in JFET operation. The reverse bias is applied by a voltage V_{GG} connected between the gate and source terminals as shown in Fig. 16.5 (*a*). It may be noted that positive terminal of the voltage (V_{GG}) is connected to source (S) and negative terminal to gate (G).

We know that whenever a PN junction is reverse biased, the electrons and holes diffuse across the junction and leave behind the positive ions on N-side and negative ions on P-side. The region, containing these immobile ions, is known as depletion region. As the reverse bias voltage across the junction is increased, thickness of the depletion region is also increased. If both the P-side and N-side of the junctions are equally doped, the depletion region will extend equally in both the regions. However, if one side of the junction is heavily doped, as compared to the other side, the depletion region extends more into the region of lower doping.



(*a*) N-channel JFET.



(*b*) Depletion regions in JFET.

Fig. 16.5.

A similar action takes place in JFET. Since the *P-region of a N-channel JFET is heavily doped, as compared to the N-channel, the depletion region extends less into the P-region and deeper into the N-channel* as shown in Fig. 16.4 (*b*). Incidentally, when there is no applied voltage between the gate and source, the depletion region is symmetrical around the junction. The conductivity of depletion region is zero because there are no mobile charge carries in this region. Hence the effective width of the N-channel is reduced. It further reduces with the increased reverse-bias voltage applied across the gate and source terminals of the JFET.

The reverse-bias across the gate source junction of a JFET may also be achieved by applying a voltage across the drain and source terminals as shown in Fig. 16.5 (*a*). It may be noted that drain (D) is connected to the position terminal of the dc supply (V_{DD}) and source (S) is connected to the negative terminal.

Now we shall discuss as to how the drain-to-source voltage produces a reverse-bias across the gate-source junction in the same way as the gate-to-source voltage. In order to do so, we represent the channel resistances r_a and r_b as shown in the Fig. 16.6 (*a*). These resistances are shown variable, as their values depends upon the magnitude of the drain-to-source voltage (V_{DS}) and gate-to-source voltage (V_{GS}). In the presence of positive supply voltage V_{DD} (with gate open), the electrons flow from source to drain through the N-channel and constitutes a current known as drain current (I_D). The conventional direction of drain current is indicated from drain-to-source through the device. The drain current causes a voltage drop across the resistance r_b, which has the effect of reverse biasing the gate-to-source junction. Thus even if the gate is open, the gate-to-source junction is reverse biased by

the drain-to-source voltage. It creates depletion regions within the channel as shown in Fig. 16.6 (*a*). It may be noted from Fig. 16.6 (*b*) that depletion region is not symmetrical around the gate-source junction. As a matter of fact, it is extended more deeper into the channel near the drain terminal and less on the source terminal. It is because of the fact, *that voltage drop across* r_a *is greater than that across* r_b. *Due to this, reverse bias voltage is higher near the drain end of the channel as compared to the source end.*

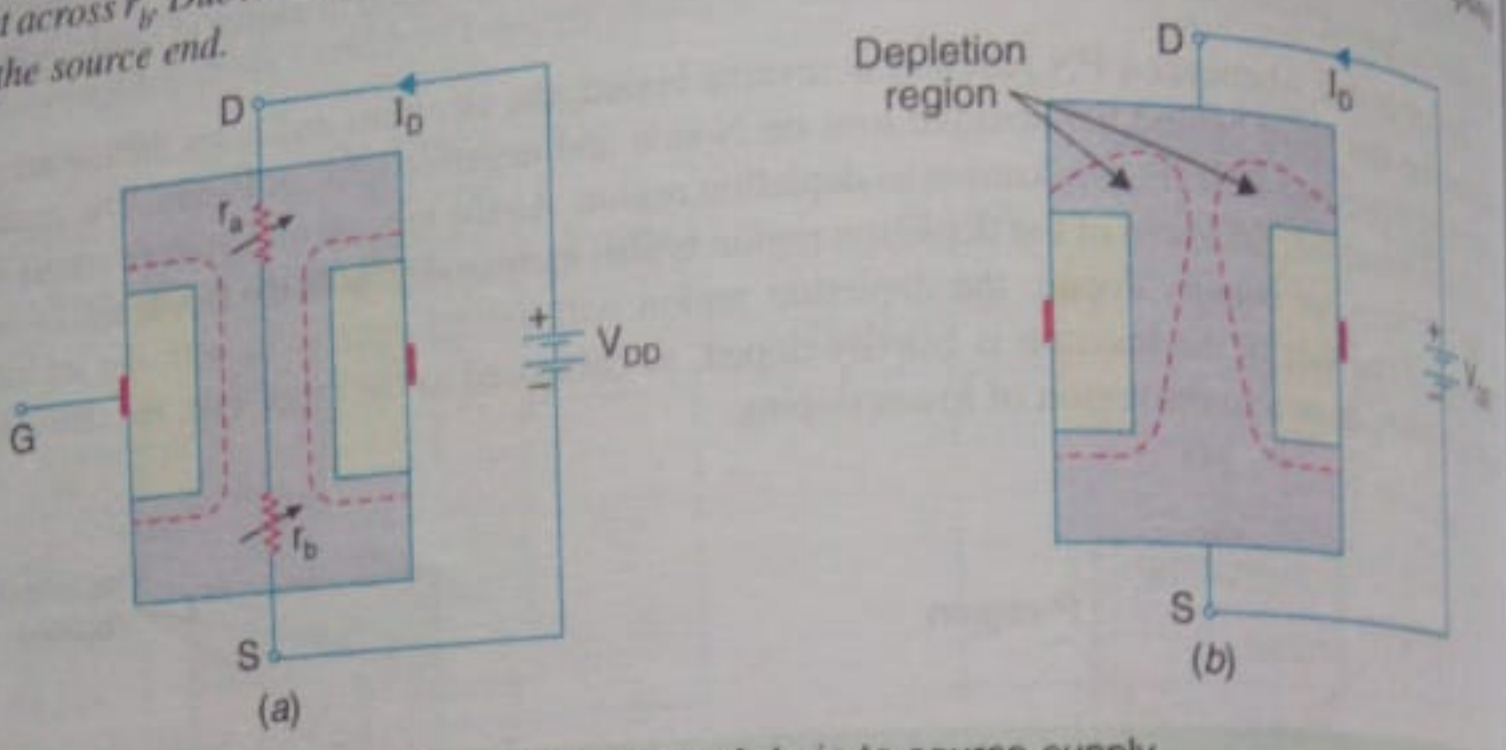


Fig. 16.6. Effect of drain-to-source supply.

16.5. Operation of JFET

We have already discussed in the last article the application of negative gate voltage or positive drain voltage, with respect to source, reverse biases the gate-source junction of an N-channel JFET. The effect of reverse bias voltage is to form depletion regions within the channel. When a voltage is applied between the drain and source with a dc supply voltage (V_{DD}), the electrons flows from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current (I_D) and its conventional direction is indicated from drain-to-source. The value of drain current is maximum, when no external voltage is applied between the gate and source and is designated by the symbol I_{DSS}.

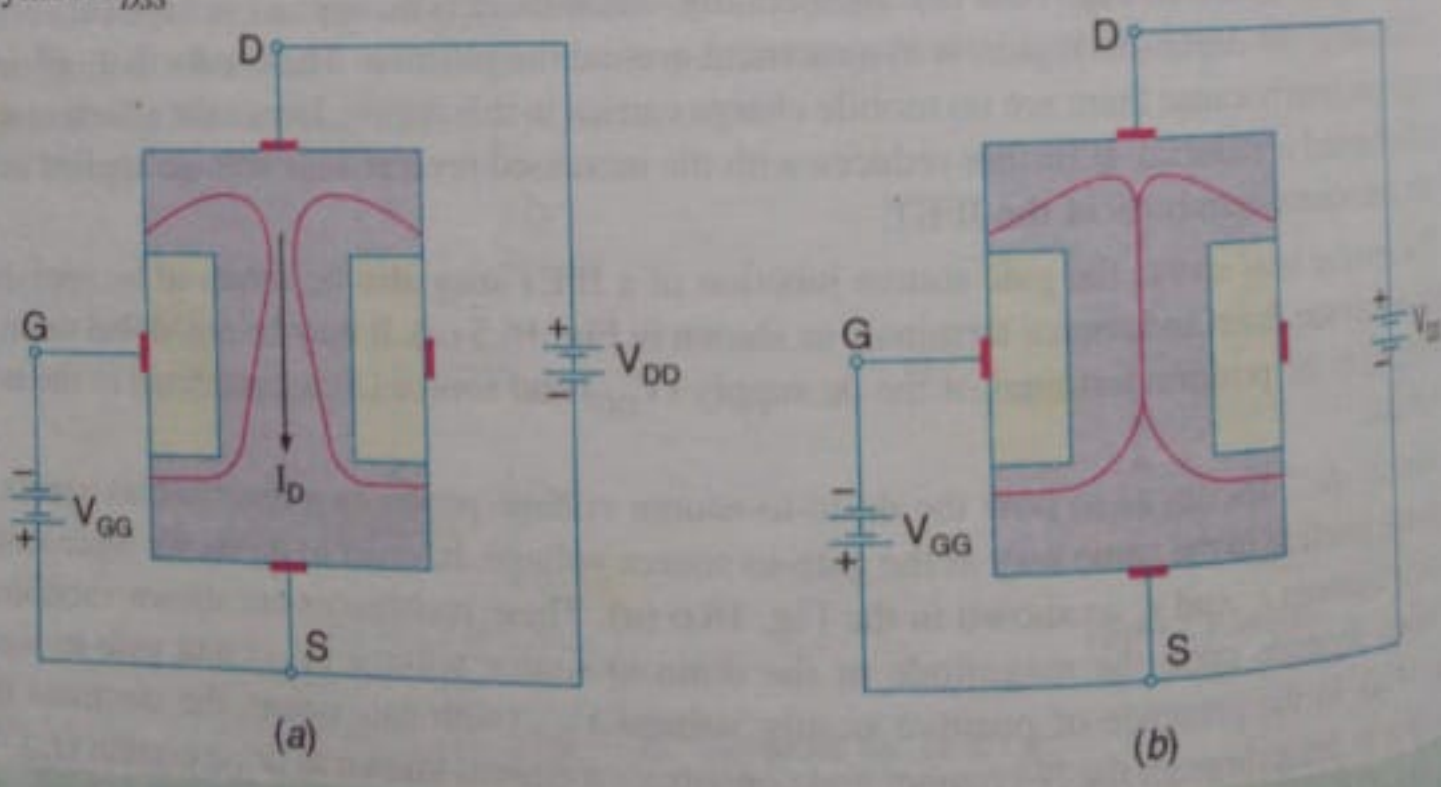


Fig. 16.7. Operation of JFET.

When the gate-to-source voltage (V_{GS}), if applied by a dc supply, (V_{GG}) and increased above zero

as shown in Fig. 16.7 (*a*), the reverse-bias voltage across the gate-source junction is increased. As a result of this, the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel. When the gate-to-source voltage (V_{GS}) is increased further, a stage is reached at which two depletion regions touch each other as shown in Fig. 16.7 (*b*). At this gate-to-source voltage, the channel is completely blocked or pinched off and drain current is reduced to zero. The gate-to-source voltage (V_{GS}) at which the drain current is zero (or completely cut-off) is called pinch off voltage. It is designated by the symbol V_p or V_{GS} (off). The value of pinch off voltage V_p is negative for N-channel JFET's. It depends on (*i*) doping of the N and P regions of the device and (*ii*) width of the original channel structure.

The operation of P-channel JFET is exactly similar to N-channel JFET, except that current carriers are holes and polarities of the dc supply, voltage V_{GG} and V_{DD} are reversed.

16.6. Characteristics of JFET

We know that a family (or a set) of curves which relate device current and voltages are known as characteristic curves. Followings are the two important characteristics of a JFET:

1. ***V-I or drain characteristics.*** These curves give relationship between the drain current (I_D) and drain-to-source voltage (V_{DS}) for different values of gate-to-source voltage (V_{GS}).
2. ***Transfer characteristics.*** These curves give relationship between drain current (I_D) and gate-to-source voltage (V_{GS}) for different values of drain-to-source (V_{DS}) voltage.

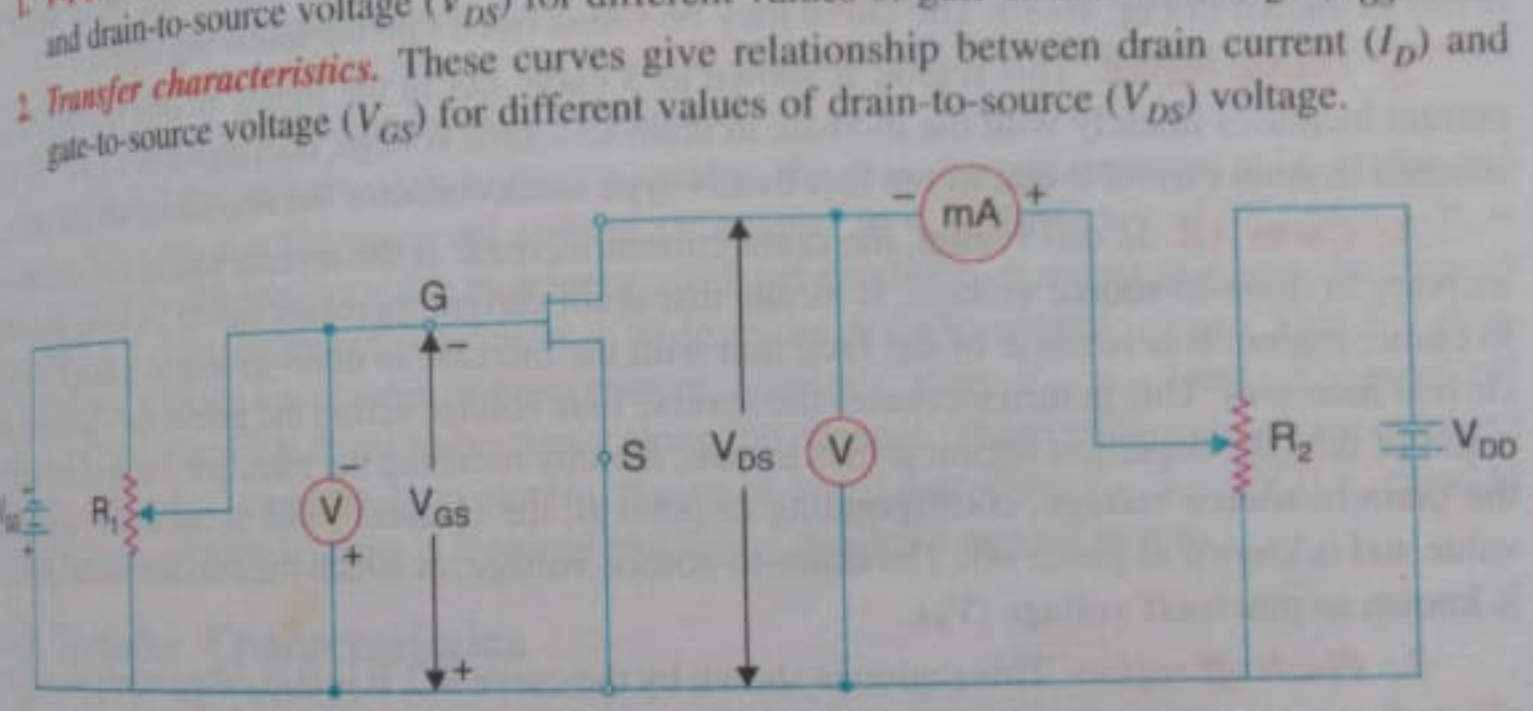


Fig. 16.8. Circuit arrangement for plotting JFET characteristics.

The drain and transfer characteristics of JFET may be obtained by using an N-channel JFET connected in the common source mode as shown in Fig. 16.8. Here the potentiometers R_1 and R_2 are used to vary the voltages V_{GS} and V_{DS} respectively. The voltages V_{DS} and V_{GS} may be measured by the voltmeters connected across the JFET terminals. The drain current (I_D) can be measured by the milliammeter connected in series with the JFET and the supply voltage V_{DD}.

16.7. Drain Characteristics

These curves may be obtained by using the circuit arrangement shown in Fig. 16.8. First of all, we adjust the gate-to-source voltage (V_{GS}) to zero volt. Then increase the drain-to-source voltage (V_{DS}) in small suitable steps and record the corresponding values of drain current (I_D) at each step. Now if we plot a graph with drain-to-source voltage along the horizontal axis and drain current along the vertical axis, we shall obtain a curve marked $V_{GS} = 0$ as shown in Fig. 16.9. A similar procedure may be used to obtain curves for different values of gate-to-source voltage *i.e.*, V_{GS} = 1, 2, 3 and 4 V.

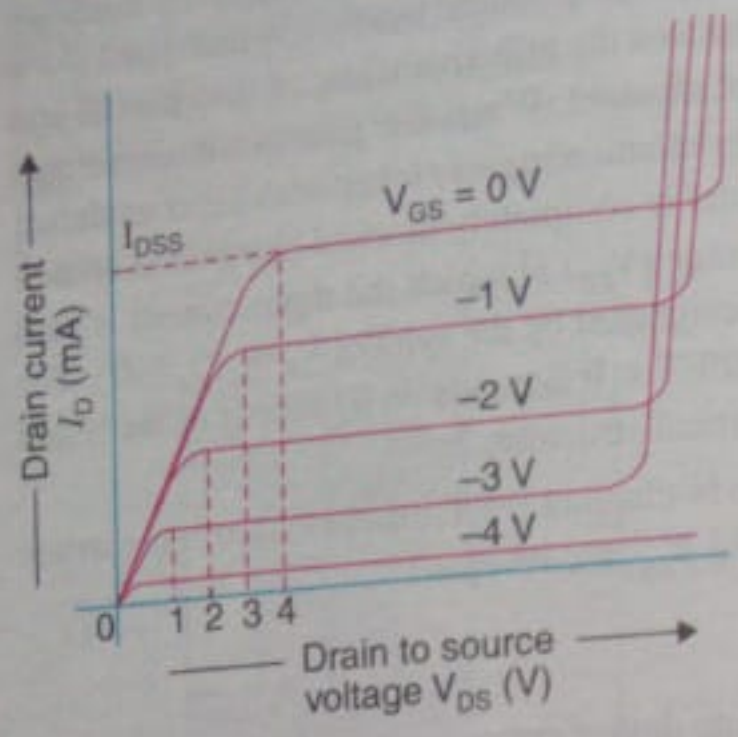


Fig. 16.9. Drain characteristics of JFET.

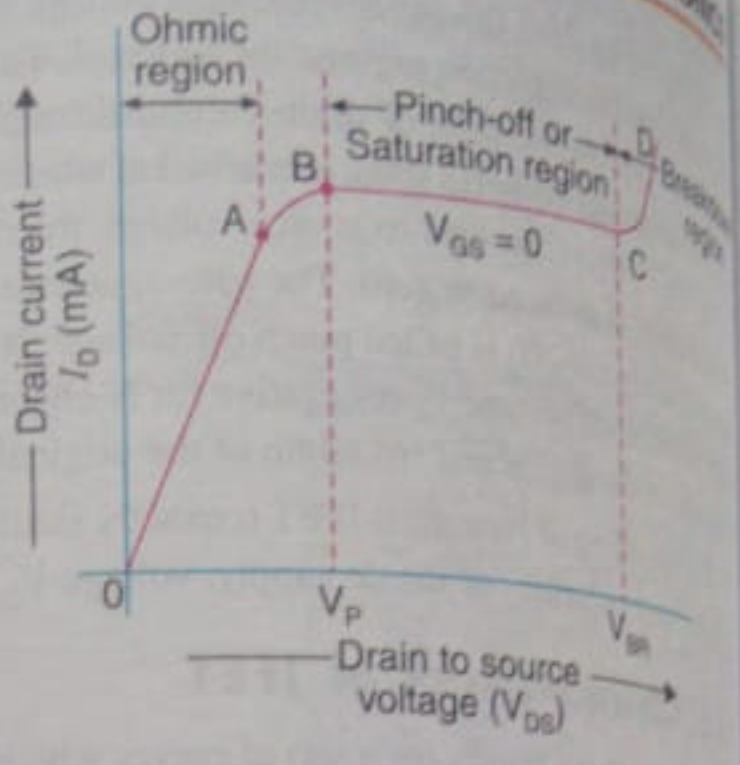


Fig. 16.10. Drain characteristics with $V_{GS} = 0$ V

In order to explain, the typical shape of drain characteristics, let us select the curve with V_{GS} = 0 volt as shown in Fig. 16.10. The curve may be sub-divided into the following regions:

1. ***Ohmic region.*** This region is shown as a curve *OA* in the figure. In this region, the drain current increases linearly with the increase in drain-to-source voltage, obeying Ohm's Law. The linear increase in drain current is due to the fact that N-type semiconductor bar acts like a simple resistor.

2. ***Curve AB.*** In this region, the drain current increase at the reverse square law rate with the increase in drain-to-source voltage. It means that drain current increases slowly as compared to that in ohmic region. It is because of the fact, that with the increase in drain-to-source voltage, the drain current increases. This in turn increases the reverse bias voltage across the gate-source junction. As a result of this, the depletion region grows in size, thereby reducing the effective width of channel. At the drain-to-source voltage, corresponding to point *B*, the channel width is reduced to a minimum value and is known as pinch off. The drain-to-source voltage, at which the channel pinch-off occurs is known as pinch-off voltage (V_p).

3. ***Pinch off region.*** This region is shown by the curve *BC*. It is also called saturation region or constant current region. In this region, the drain current remains constant at its maximum value (I_{DSS}). The drain, current in the pinch off region, depends upon the gate-to-source voltage and is given by the relation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The above relation is known as *Shockly's equation*. The pinch off region is the normal operating region of JFET, when used as an amplifier.

4. ***Breakdown region.*** This region is shown by the curve *CD*. In this region, the drain current increases rapidly as the drain-to-source voltage is also increased. It happens because of the breakdown of gate-to-source junction due to avalanche effect. The drain-to-source voltage corresponding to point *C* is called breakdown voltage.

16.8. Effect of Gate-to-Source Voltage on Drain Characteristics

We have already discussed in the last article about the drain characteristics of JFET. The effect of increasing gate-to-source voltage on the drain characteristics may be noted from Fig. 16.9. As

gate-to-source voltage (V_{GS}) is increased above zero to the 1, 2, 3 and 4 volts, following two effects take place:

1. The value of pinch off voltage is reached at a smaller value of drain current as compared to that when $V_{GS} = 0$, and
2. The value of drain-to-source voltage (V_{DS}) is decreased as compared to that when $V_{GS} = 0$.

The first effect may be understood from the fact that reverse bias voltage across the gate-source junction of JFET is the sum of gate-to-source voltage (V_{GS}) and drain-to-source voltage (V_{DS}). Thus for fixed V_{DS}, the increased value of V_{GS} will increase the reverse bias across the junction. For example, if V_{GS} of – 1 V is applied between the gate and source of JFE, then the gate-to-source junction becomes reverse biased, even when the drain current is zero. This causes the depletion regions to be formed within the channel. As the voltage V_{DS} is increased above zero, the drain current increases. This produces voltage drop across channel resistance, which in turn produces reverse bias voltage across the gate-source junction. The amount of reverse bias voltage required to be produced by drain current would obviously be decreased by one volt. In other words, a smaller voltage drop along the channel (*i.e.*, smaller than that when $V_{GS} = 0$) will increase the depletion regions to the point where they will pinch off the drain current. As a result of this, the pinch-off voltage (V_P) is reached at a lower value of drain current than that when $V_{GS} = 0$.

The second effect is caused due to the fact that the increased value of gate-to-source voltage (V_{GS}) keeps adding to the reverse bias at the junction produced by the drain current. Therefore its lower value is required to reach the breakdown voltage.

It may be noted that with zero gate-to-source voltage, the drain current saturates at I_{DSS} value and the characteristic indicates the pinch off voltage (V_P) equal to 4 V. However, if V_{GS} of – 1 V, is applied, the channel still requires – 4 V to achieve pinch off condition. It means that now the channel requires only 3 V drop (instead of previously 4 V) from the drain-to-source voltage. This 3 V drop may be achieved with the lower value of drain current. Similarly, when V_{GS} is – 2 and –3 V, pinch off is achieved with 2 V and 1 V drops respectively along the channel. These voltage drops are obtained with further reduced values of the drain current. It may be noted that when V_{GS} is – 4 V (*i.e.*, equal to pinch off voltage), no channel drop is required and hence the drain current is zero.

16.9. Transfer Characteristics

These are also called transconductance curves, which give us the relationship between drain current (I_D) and gate-to-source voltage (V_{GS}) for a constant value of drain-to-source voltage (V_{DS}). The transfer characteristics may be obtained by using the circuit arrangement shown in Fig. 16.8. First of all, we adjust the drain-to-source voltage to some suitable value and increase the gate-to-source voltage in small suitable steps. Now record the corresponding values of drain current at each step. If we plot a graph with gate-to-source voltage (V_{GS}) along the horizontal axis and the drain current (I_D) along the vertical axis, we shall obtain a curve as shown in Fig. 16.11. A similar procedure may be used to obtain curves at different values of gate-to-source voltage (V_{GS}).

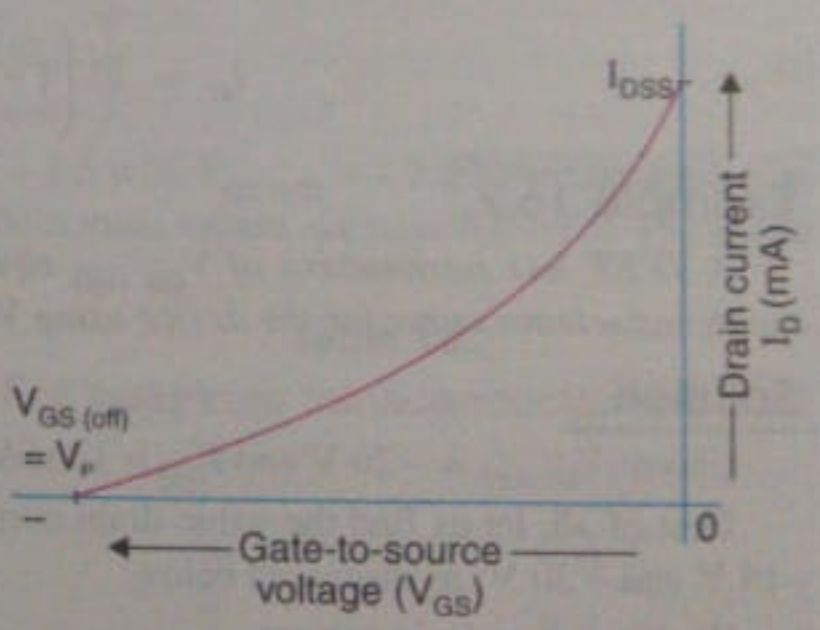


Fig. 16.11. Transfer characteristics of *N*-channel.

The upper end of the curve is shown by the drain current value equal to I_{DSS}, while the lower end is indicated by a voltage equal to $V_{GS(off)}$ or V_p. It may be noted that the curve is part of a parabola and therefore may be expressed by the equation,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2 = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

There is one important point which must be mentioned. Most JFET specifications sheet give more than one value of $V_{GS(off)}$ and I_{DSS}. For example, the specifications sheet for the JFET 2N5457 lists the following:

$V_{GS(off)\,(minimum)} = -0.5$ V and $I_{DSS(min)} = 1$ mA

$V_{GS(off)\,(maximum)} = -6$ V and $I_{DSS(max)} = 5$ mA

In such a situation, we must use the two minimum values to plot one curve and the two maximum values to plot another curve on the same graph.

Example 16.1.

The data sheet of a certain JFET indicates that I_{DSS} equal to 15 mA and V_{GS} (off) equal to –5 V. Determine the drain current for V_{GS} equal to 0 V, – 1 V and – 4 V.

Solution.

Given: $I_{DSS} = 15$ mA and $V_{GS\,(off)} = -5$ V

We know that drain current,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

∴ Drain current when ($V_{GS} = 0$,)

$$I_D = 15\left(1-\frac{0}{-5}\right)^2 = 15 \text{ mA}$$ **Ans.**

Similarly, drain current when $V_{GS} = -1$ V,

$$I_D = 15\left(1-\frac{-1}{-5}\right)^2 = 9.6 \text{ mA}$$ **Ans.**

and drain current when $V_{GS} = -4$ V,

$$I_D = 15\left(1-\frac{-4}{-5}\right)^2 = 0.6 \text{ mA}$$ **Ans.**

Example 16.2.

A JFET has parameters of $V_{GS\,(off)}$ equal to – 20 V and I_{DSS} equal to 12 mA. Plot its transconductance curve for the device using V_{GS} values of 0 V, – 5 V, –10 V, – 15 V and – 20 V.

Solution.

Given: $V_{GS\,(off)} = -20$ V and $I_{DSS} = 12$ mA

First of all, let us find the value drain currents for the given values of V_{GS} (0 V, – 5 V, – 10 V, – 15 V and – 20 V) as discussed below:

We know that drain current,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS\,(off)}}\right)^2$$

∴ Drain current when $V_{GS} = -5$ V,

$$I_D = 12\left(1-\frac{-5}{-20}\right)^2 = 6.75 \text{ mA}$$

Similarly, using the maximum values of $V_{GS(off)} = -6$ V and $I_{DSS} = 20$ mA, we can use equation (i) again for $V_{GS} = -4$ V and -2 V to obtain the values of I_D in between the end points. The end points of the transconductance curve are (–6 V, 0 mA) and (0 V, 20 mA). The values of I_D for in between points are 2.2 mA and 8.9 mA. The values obtained are shown in Table 16.3.

Now if we plot the values corresponding to the sets shown in Tables 16.2 and 16.3 and joining them, we get the minimum and maximum trans conductance curve as shown in Fig. 16.13.

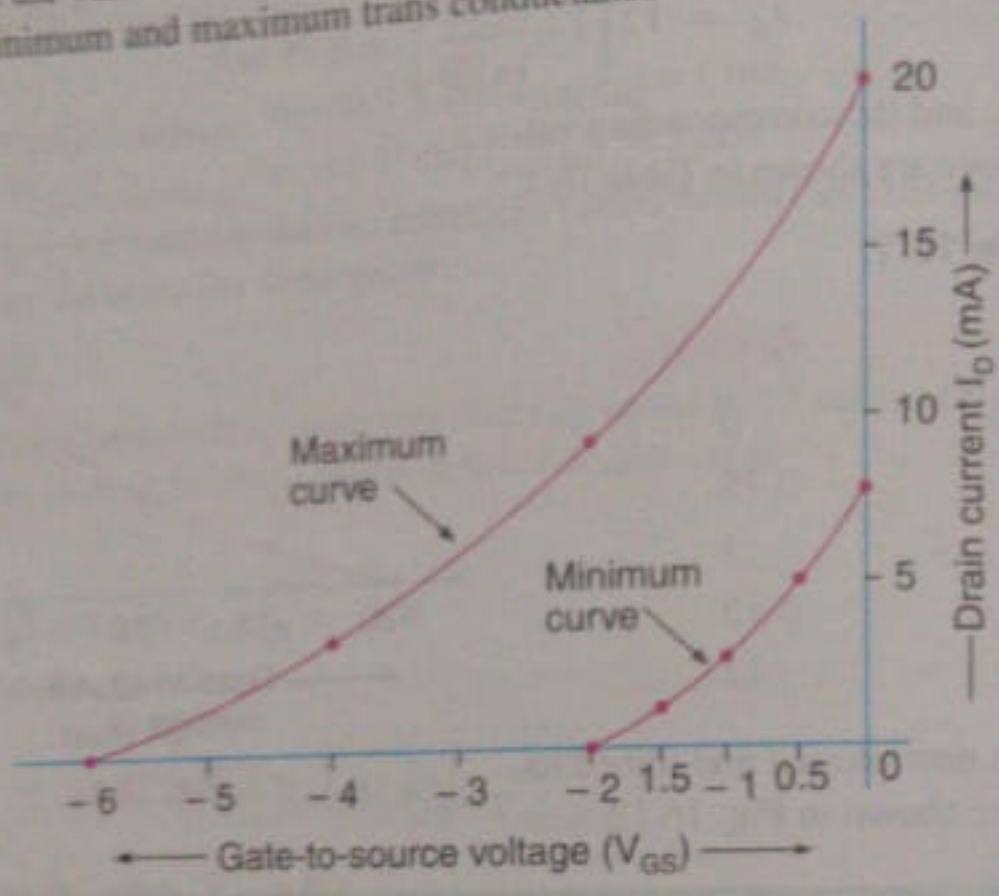


Fig. 16.13.

16.10. Specifications Sheet of JFET

Although the genral content of specification sheets may very from the absolute minimum to an extensive display of graph and charts, there are a few fundamental parameters that will be provided by all manufactures. The specifications sheet for 2N5484 through 2N5486 JFETs as provided by the Motorola is as shown in Fig. 16.14.

Maximum Ratings: Most of the maximum ratings for these devices are self-explanatory at this point. In out discussion for the BJT specifications sheet, we covered all the commonly used maximum voltage, current and power ratings. The JFET maximum ratings are no different. As seen form the table for maximum ratings, we find that for 2N5484, the maximum ratings for V_{DG} and V_{GSR} is 25 V.

The next maximum ratings in the list is for the drain current which is indicated as 30 mA dc. Then it is the maximum value of forward gate current. This rating is indicated as 10 mAdc. This rating may produce a through in your mind that the FET could be operated in the forward region. But the answer to such a thought is NO. Recall that the contorl of drain current in FET depends upon the amount of *reverse* bias on the JFET. The maximum drain current (I_{DSS}) is reached when the reverse bias reaches 0 V. any increase in V_{GS} above 0 V will not cause any increase in drain current. However, should the gate accidentally becomes forward biassed; I_G must be greater than 10 mAdc, for the device to be destroyed. As long as I_G is below 10 mAdc, the device will be safe.

The maximum power dissipation which the device under consideration can safely handle at 25°C is 310 mW. As the temperature exceeds 25°C temperature, the maximum power dissipation reduces at the rate of 2.82 mW for each 1°C increase in temperature above 25°C.

Off Characteristics : In this list three values are indicated:

(*i*) gate-source brakdown voltage, $V_{(BR)GSS}$

(*ii*) gate reverse current, I_{GSS}, and

(*iii*) gate-source cut-off voltage, $V_{GS(off)}$. The gate-source brakdown voltage defines the limit on V_{GS}. If V_{GS} is allowed to exceed this value (–25 V for 2N5484), the JFET will have to be replaced.

The gate reverse current rating indicates the maximum value of gate current that will occur when the gate-source junction is reverse biased. For the 2N5484 JFET, this rating is 1 nAdc when the ambient temperature (T_A) is 25 °C. note that the negative current value is used to indicate the direction of the gate current. I_{GSS} is a temperature dependent rating. Notice that the value of I_{GSS} increases form 1 nAdc to 1 mAdc as theambient temperature increases from 25 ° C to 100°C

Since we have already disscussed $V_{GS(off)}$ and I_{DSS} (listed under "**ON Characteristics**") in detail, we will not discuss them further here. It may be carefully noted that there are wide ranges of $V_{GS(off)}$ and I_{DSS} values within the 2N 5484-5486 series. For example, for 2N5484, the values of $V_{GS(off)}$ vary from – 0.3 to – 3 V and I_{DSS} from 1 mA to 5 mA. Similarly for 2N5485, the values of $V_{GS(off)}$ vary from -0.5 to –4 V and I_{DSS} from 4 mA to 10 mA. And for 2N5486 the value of $V_{GS(off)}$ vary from –2 V to -6 V and I_{DSS} from 8 mA to 20 m..

Small signal characteristics: These will be discussed later.

Case Construction and Terminal Identification: The 2N5484-6 JFETs have the appearance as shown of right top corner of the specification sheet. The terminal identification is also provided there. The JFETs are available in top-hat containers as shown in Fig. 16.14.

16.11. JFET Parameters

The electrical behaviour of JFET may be described in terms of certain parameters called JFET parameters. Such parameters may be obtained from the characteristic curves. The important parameters of JFET are as discussed below:

1. ***D.C drain resistance*** (R_{DS}). It is also called the static or ohmic resistance of the channel and is given by the ratio of voltage (V_{DS}) to the drain current (I_D). Mathematically d.c. drain resistance,

$$R_{DS} = \frac{V_{DS}}{I_D}$$

2. ***A.C. drain resistance*** (r_d). It is also called dynamic drain resistance and is the a.c. resistance between the drain and source terminal when the JFET is operating in the pinch-off or saturation region. It is given by the ratio of small change in drain-to-source voltage (ΔV_{DS}) to the corresponding change in drain current (ΔI_D) for a constant gate-to-source voltage (V_{GS}). Mathematically, the a.c. drain resistance,

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$$

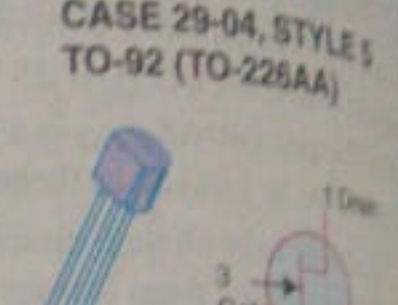
It is sometimes written as r_{ds}, which indicates that it is the resistance from drain-to-source terminals. Since r_d is the output resistance of JFET, it may also be expressed as an output admittance Y_{os} (*i.e.*, equal to $1/r_d$).

3. ***Transconductance*** (g_m). It is also called forward transconductance or forward transmittance. It is given by the ratio of small change in drain current (ΔI_D) to the corresponding change in gate-to-source voltage (ΔV_{GS}) for a constant drain-to-source voltage (V_{DS}). Mathematically, the transconductance,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

2N5484 thru 2N5486

CASE 29-04, STYLE 5
TO-92 (TO-226AA)



JFET VHF/UHF AMPLIFIERS

N-CHANNEL– DEPLETION

Refer to 2N4416 for graphs.

MAXIMUM RATINGS

Rating	Sympol	Value	Unit
Drain-Gate Voltage	V_{DG}	25	Vdc
Reverse Gate-Source Voltage	V_{GSR}	25	Vdc
Drain Current	I_D	30	mAdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ $T_C = 25°C$	P_D	310	mW
Derate above 25°C		2.82	mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	– 65 to + 150	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate-Source Breakdown Voltage ($I_G = -1.0$ μAdc, $V_{DS} = 0$)		$V_{(BR)GSS}$	– 25	—	—	Vdc
Gate Reverse Current ($V_{GS} = -20$ Vdc, $V_{DS} = 0$)		I_{GSS}	—	—	– 1.0	nAdc
($V_{GS} = -20$ Vdc, $V_{DS} = 0$, $T_A = 100°C$)					– 0.2	μAdc
Gate Source Cutoff Voltage ($V_{DS} = 15$ Vdc, $I_D = 10$ nAdc)	2N5484	$V_{GS(off)}$	– 0.3	—	– 3.0	Vdc
	2N5485		– 0.5	—	– 4.0	
	2N5486		– 2.0	—	– 6.0	
ON CHARACTERISTICS						
Zero-Gate-Voltage Drain Current ($V_{DS} = 15$ Vdc, $V_{GS} = 0$)	2N5484	I_{DSS}	1.0	—	5.0	mAdc
	2N5485		4.0	—	10	
	2N5486		8.0	—	20	
SMALL-SIGNAL CHARACTERISTICS						
Forward Transfer Admittance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1.0$ kHz)	2N5484	$\lvert y_{fs} \rvert$	3000	—	6000	μmhos
	2N5485		3500	—	7000	
	2N5486		4000	—	8000	
Input admittance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 100$ MHz)	2N5484	$Re(y_{is})$	—	—	100	μmhos
($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 400$ MHz)	2N5485, 2N5486		—	—	1000	
Output Admittance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 1.0$ kHz)	2N5484	$\lvert y_{os} \rvert$	—	—	50	μmhos
	2N5485		—	—	60	
	2N5486		—	—	75	
Output Conductance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 100$ MHz)	2N5484	$Re(y_{os})$	—	—	75	μmhos
($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 400$ MHz)	2N5485, 2N5486		—	—	100	
Forward Transconductance ($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 100$ MHz)	2N5484	$Re(y_{fs})$	2500	—	—	μmhos
($V_{DS} = 15$ Vdc, $V_{GS} = 0$, $f = 400$ MHz)	2N5485		3000	—	—	
	2N5486		3500	—	—	

Fig. 16.14. (Courtesy : Motorola Inc.)

(Continued)

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Fig. No.	Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Gate-Source Breakdown Voltage (I_G = 10 μAdc, V_{DS} = 0)	–	$V_{(BR)GSS}$	25	–	Vdc
Gate Leakage Current (I_{GSS} = −30 Vdc, V_{DS} = 0)	–	I_{GSS}	– –	10 100	pAdc
(I_{GSS} = −30 Vdc, V_{DS} = 0, T_A = 125°C)					nAdc
Drain-Gate Voltage Drain Current (V_{DS} = 10 Vdc, V_{GS} = 0)	–	I_{DGO}	–	10	
(V_{DS} = 10 Vdc, V_{GS} = 0, T_A = 125°C)			–	1.0	μAdc
ON CHARACTERISTICS					
Gate-Source Threshold Voltage (V_{DS} = 10 Vdc, I_D = 10 μAdc) 3N169	–	$V_{GS(th)}$	0.5	1.5	Vdc
3N170			1.0	2.0	
3N171			1.5	3.0	
ON Drain Current (V_{DS} = 10 Vdc, V_{GS} = 10 Vdc)	3	$I_{D(on)}$	10	–	mAdc
Drain-Source "ON" Voltage (I_D = 5.0 mAdc, V_{GS} = 10 Vdc)	–	$V_{DS(on)}$	–	2.0	Vdc
SMALL SIGNAL CHARACTERISTICS					
Drain-Source Resistance (V_{GS} = 10 Vdc, I_D = 0, f = 1.0 kHz)	4	$r_{ds(on)}$	–	200	Ohms
Forward Transfer Admittance (V_{DS} = 10 Vdc, I_D = 2.0 mAdc, f = 1.0 kHz)	1	$\lvert y_{fs} \rvert$	1000	–	μmhos
Reverse Transfer Capacitance (V_{DS} = 0, V_{GS} = 5.0 Vdc, f = 1.0 MHz)	2	C_{rss}	–	1.3	pF
Input Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz)	2	C_{iss}	–	5.0	pF
Drain-Substrate Capacitance (V_{DB} = 10 Vdc, f = 1.0 MHz)	–	$C_{d(sub)}$	–	5.0	pF
SWITCHING CHARACTERISTICS					
Turn-On Delay Time	(V_{DD} = 10 Vdc, $I_{D(on)}$ = 10 mAdc, $V_{GS(on)}$ = 10 Vdc, $V_{GS(off)}$ = 0, R_G = 50 Ohms)	6,10	$t_{d(on)}$	–	3.0	ns
Rise Time		7,10	t_r	–	10	ns
Turn-Off Delay Time		8,10	$t_{d(off)}$	–	3.0	ns
Fall Time		9,10	t_f	–	15	ns

Values JEDEC Registered Data

FIGURE 1 – FORWARD TRANSFER ADMITTANCE

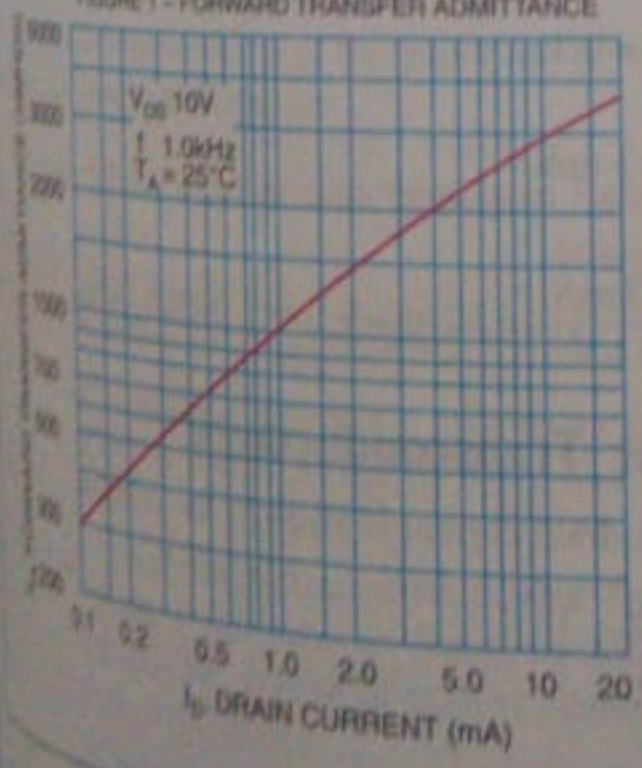


FIGURE 2 – CAPPACITANCE

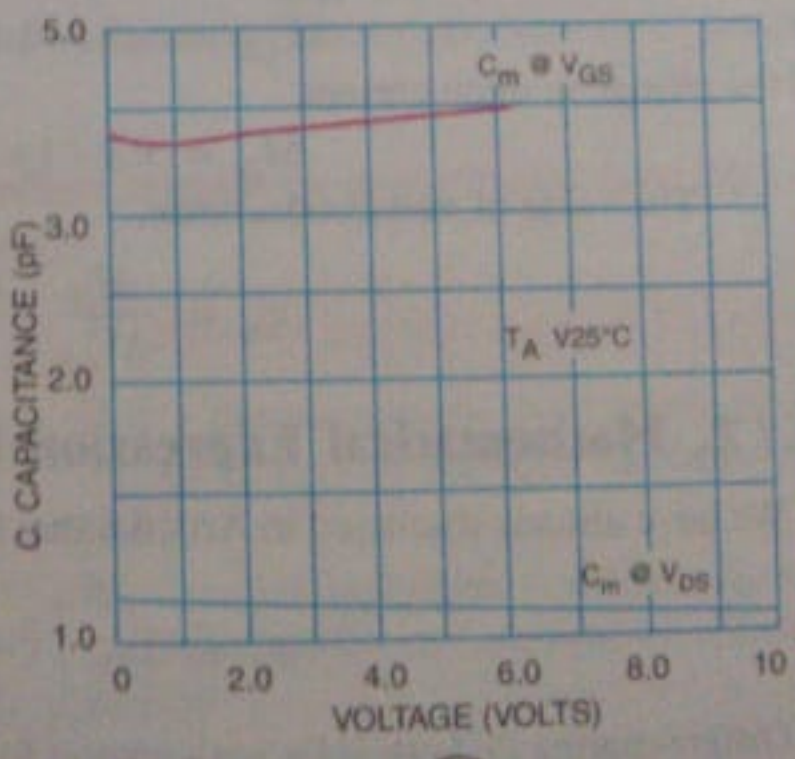


Fig. 16.14. (a) (Contd.) (Courtesy : Motorola Inc.)

The value of transconductance (g_m) is expressed in siemens (S) or mhos. We know that transfer characteristic of a JFET is a part of a parabola *i.e.*, it is non-linear. Therefore the value of g_m varies depending upon the location on the curve as set by the gate-to-source voltage (V_{GS}). It has a greater value near the top of the curve than near the bottom.

4. *Amplication factor* (μ). It is given by the ratio of small change in drain-to-source voltage (ΔV_{DS}) to the corresponding change in gate-to-source voltage (ΔV_{GS}) for a constant drain current (I_D). Mathematically, the amplification factor,

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

The amplification factor (μ) may also be expressed as a product of transconductance (g_m) and a.c. drain resistance (r_d).

Thus
$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}} = r_d \times g_m$$

5. *Input Resistance* (R_i). We know that a JFET operation with its gate-source junction reverse biased. As the reverse current of a junction is, usually, very small. Therefore gate-reverse current of a JFET is also very small. Since the gate-source junction of a JFET is used as an input, therefore its input resistance of a JFET is very high. This high input resistance is an advantage of JFET over its bipolar transistor. Mathematically, the input resistance,

$$R_i = \frac{V_{GS}}{I_{GSS}}$$

where V_{GS} = Gate-to-source voltage and
I_{GSS} = Gate reverse current. It is of the order of nano-ampere.

Example 16.4.

When V_{GS} of a FET changes from –3.1 V to –3 V, the drain current charges from 1 mA to 1.3 mA. What is the value of transconductance ?

Solution.

Given: V_{GS} of a FET changes from –3.1 V to 3 V and the drains current, 1 mA to 1.3 mA.

We know that change in V_{GS},

$$\Delta V_{GS} = -3 (-3.1) = 0.1.$$

and the change in drain current,

$$\Delta I_D = 1.3 - 1 = 0.3 \text{ mA}.$$

∴ The value of transconductance,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{0.3 \text{ mA}}{0.1 \text{ V}} = 30 \text{ mA/V} \quad \text{or} \quad 30 \text{ mS} \quad \text{Ans.}$$

16.12. Mathematical Expression for Transconductance

We have already discussed in Art 16.6 that the drain current is given by the relation,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Differentiating on both sides with respect to V_{GS},

$$\frac{dI_D}{dV_{GS}} = 2I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \times \left(\frac{0 - 1}{V_P}\right)$$

$$g_m = -\frac{2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Substituting $V_{GS} = 0$ in the above expression,

$$g_m = -\frac{2I_{DSS}}{V_P} = g_{mo}$$

The value of g_m at $V_{GS} = 0$ is the maximum and is equal to $-2I_{DSS}/V_P$. This value of g_m is designated as g_{mo}. The equation (*i*) may now be rewritten as:

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Example 16.5.

The following information is included on the data sheet for an N-channel JFE:

$$I_{DSS} = 20\ mA,\ V_P = -8\ V \text{ and } g_{mo} = 5000\ \mu S.$$

Determine the values of drain current and transconductance at $V_{GS} = -4$ volts.

Solution.

Given: $I_{DSS} = 20$ mA, $V_P = -8$ volts; $g_{mo} = 5000$ µS and $V_{GS} = -4$ volts.

Value of drain current

We know that drain current,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 20\left(1 - \frac{-4}{-8}\right)^2 = 5\ \text{mA}\ \textbf{Ans.}$$

Value of transconductance

We also know that transconductance,

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) = 5000\left(1 - \frac{-4}{-8}\right) = 2500\ \mu\text{S}\ \textbf{Ans.}$$

16.13. Comparison Between Field-Effect Transistor and Bipolar Junction Transistor

Table 16.4 shows some of the important points of comparison between the field-effect transistor and bipolar junction transistor.

Table 16.4: Comparison between field-effect transistor and bipolar junction transistor

S.No	*Field-Effect Transistor (FET)*	*Bipolar junction transistor (BJT)*
1.	It is a unipolar device. *i.e.*, current in the device is carried either by electrons or holes.	It is a bipolar device. *i.e.* current in the device is carried by both electrons and holes.
2.	It is a voltage-controlled device *i.e.*, voltage at the gate (or drain) terminal controls the amount of current flowing through the device.	It is a current-controlled device. *i.e.* the base current controls the amount of collector current.
3.	Its input resistance is very high and is of the order of several megaohms.	Its input resistance is very low as compared to FET and is of the order of few kilohms.

4.	It has a negative temperature coefficient at high current levels. It means that current decreases as the temperature increases. This characteristic prevents the FET from thermal breakdown.	It has a positive temperature coefficient at high current level. It means that collector current increases with the increase in temperature. This characteristic leads the BJT to thermal breakdown.
5.	It does not suffer from minority-carrier storage effects and therefore has higher switching speeds and cut-off frequences.	It suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies than that of FET's.
6.	It is less noisy than a BJT or vacuum tube and is thus more suitable as an input amplifier for low-level signals. It is used extensively in high fidelity frequency modulated receivers.	It is comparatively more noisy than a field-effect transistor.
7.	It is much simpler to fabricate as a integrated circuit (IC) and occupies a less space on IC chip than that of BJT.	It is comparatively difficult to fabricate as an integrated circuit and occupies more space on IC chip than that of FET.

16.14. MOSFETs

The MOSFET is an abbreviation for metal-oxide semiconductor field-effect transistor. Like JFET it has a source, gate and drain. However, unlike JFET, the gate of a MOSFET is insulated from the channel. Because of this, the MOSFET is sometimes known as an IGFET which stands for insulated gate field effect transistor.

16.15. Types of MOSFET

There are two basic types of MOSFETs; depletion-type MOSFETs and enhancement-type MOSFETs. The depletion type MOSFETs are also called D-type MOSFETs and enhancement-type MOSFETs. as E-type MOSFETs. The primary difference between the two types of MOSFETs is the difference between the constructions. Both the D-type and E-type MOSFETs are disscussed one by one in the following pages.

16.16. Depletion-Type MOSFET

Fig. 16.15 shows the basic structure of an N-channel depletion type MOSFET. It consists of a conducting bar of N-type material with an insulated gate on the left and P-region on the right. Free electrons can flow from source to drain through the N-type material. The P-region is called substrate (or body). It physically reduces the conducting path to a narrow channel. A thin layer of silicon dioxide is deposited on the left side of the channel. This layer insulates the gate from the channel. Because of this, a negligible gate current flows even when the gate voltage is positive. It will be interesting to know that a PN junction, which exists in a JFET, has been eliminated in the MOSFET.

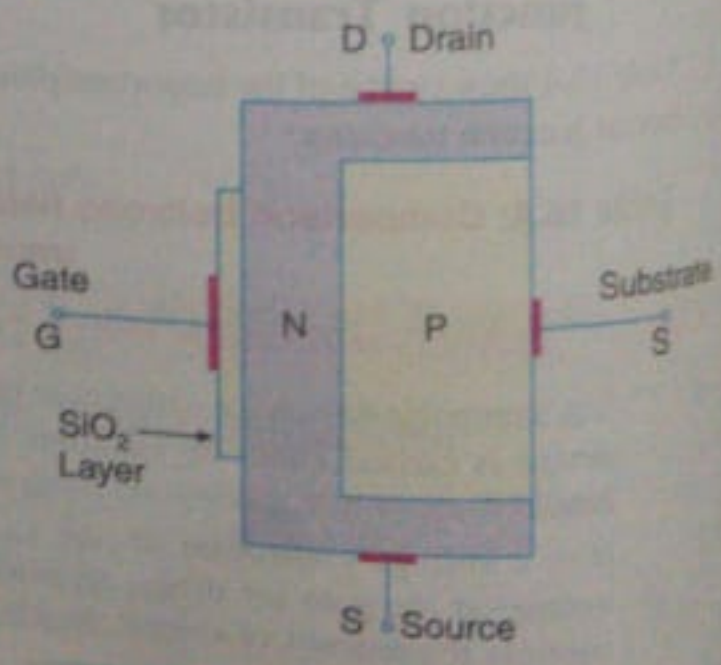


Fig. 16.15. Basic structure of an N-channel depletion-type MOSFET.

The basic construction of a depletion-type P-channel MOSFET is similar to that of N-channel except that the conducting bar is of P-type material and the substrate is of N-type material.

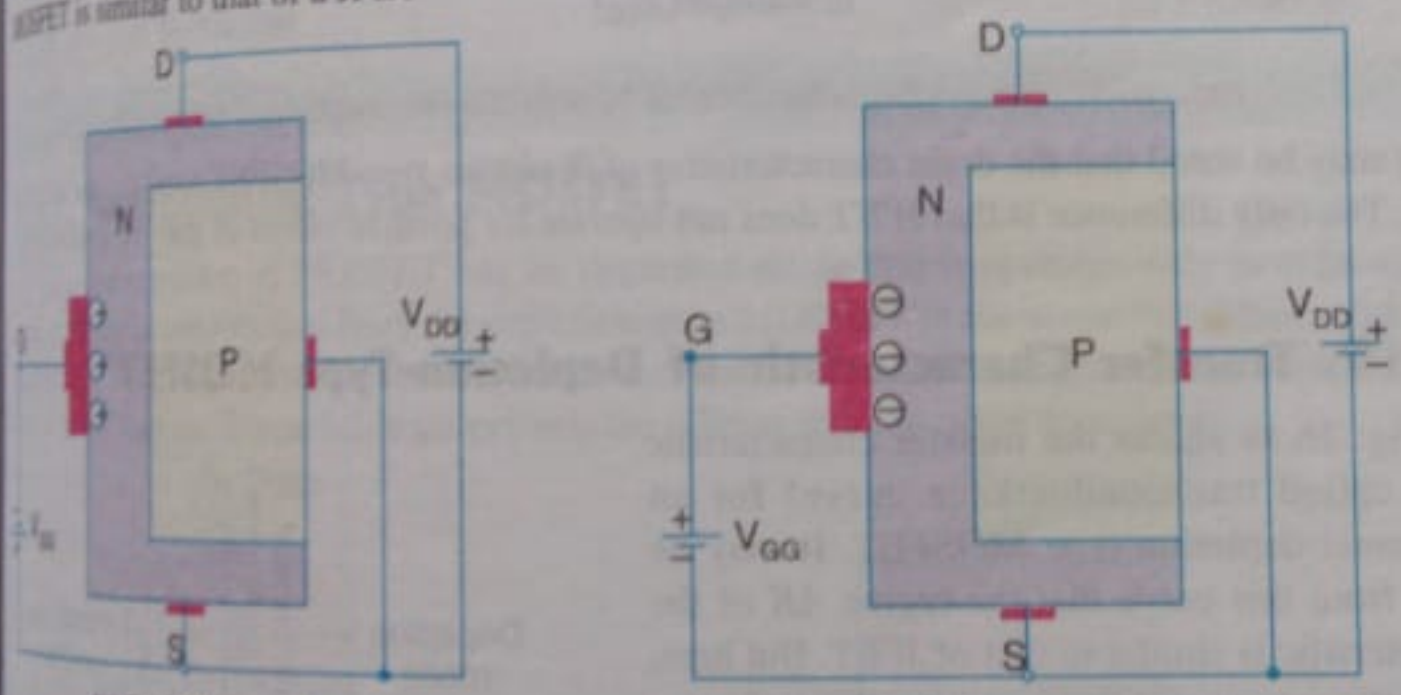
16.17. Working of a Depletion-Type MOSFET

The depletion-type MOSFET can be operated in two different modes as given below:

1. ***Depletion mode.*** The device operates in this mode, when the gate voltage in negative.
2. ***Enhancement mode.*** The device operates in this mode, when the gate voltage is positive.

Since the depletion-type MOSFET can be operated in either depletion or enhancement mode, therefore this device is commonly known as depletion-enhancement (DE) type MOSFET. The working of a MOSFET may be explained easily, if we visualize the entire structure of the device as a parallel plate capacitor. One of the plates is formed by the gate and the other by the semiconductor channel. The plates are separated by a dielectric (SiO_2 layer). We know that if one plate of a capacitor is made negative, it induces a positive charge on the opposite plate and vice versa. This principle is used below in explaining the working of MOSFET's in the depletion and enhancement modes.

1. ***Depletion mode.*** Fig. 16.16 (*a*) shows a MOSFET with a negative gate-to-source voltage. The negative voltage, on the gate, induces a positive charge in the channel. Because of this, free electrons in the vicinity of positive charge are repelled away in the channel. As a result of this, the channel is depleted of free electrons. This reduces the number of free electrons (which constitute the drain current) passing through the channel. Thus as the value of negative gate-to-source voltage is increased, the value of drain voltage, called $V_{GS(off)}$, the channel is totally depleted of free electrons and therefore the drain current reduces to zero. Thus with the negative gate voltage, the operation of MOSFET is similar to that of a JFET



(*a*) Depletion mode. (*b*) Enhancement mode.

Fig. 16.16. Working of a depletion-type MOSFET.

It is evident from the above discussion that negative gate voltage depletes the channel of free electrons. It is due to this fact that the working of a MOSFET, with a negative gate voltage, is called depletion mode.

2. ***Enhancement mode.*** Figure 16.16 (*b*) shows a MOSFET with a positive gate-to-source voltage. The positive gate voltage increases the number of free electrons passing through the channel. The greater the gate voltage, greater is the number of free electrons passing through the channel. This increases i.e., enhances the conducting of the channel. Because of this fact, positive gate operation is called enhancement mode.

It will be interesting to know that depletion-type MOSFET can conduct even if the gate-source voltage (V_{GS}) is zero. Because of this, it is commonly known as Normally-ON MOSFET.

16.18. Drain Characteristic of Depletion-Type MOSFET

Fig. 16.17 shows the drain characteristic for the N-channel depletion-type MOSFET in the common source configuration. These curves are plotted for both negative and positive values of gate-to-source voltage (V_{GS}). The curves shown above the curve for $V_{GS} = 0$ have a positive zero whereas those below it have a negative value of V_{GS}. When V_{GS} is zero and negative, the MOSFET operates in the depletion-mode. On the other hand, if VGS is zero and positive, the MOSFET operates in the enhancement-mode.

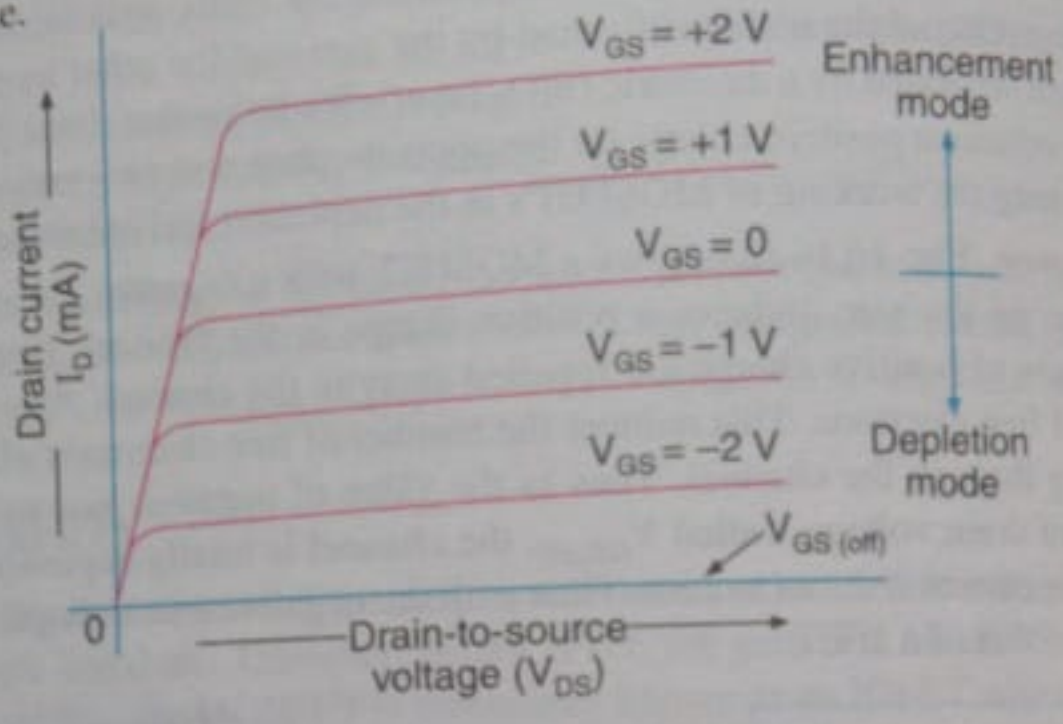


Fig. 16.17. Drain characteristics of N-channel depletion-type MOSFET.

It may be noted that the drain characteristics of depletion-type MOSFET's are similar to that of JFET. The only difference is that JFET does not operate for positive values of gate-to-source voltage (V_{GS}).

16.19. Transfer Characteristic of Depletion-Type MOSFET

Fig. 16.18 shows the transfer characteristic (also called transconductance curve) for an N-channel depletion-type MOSFET. It may be noted from this curve that the region *AB* of the characteristic is similar to that of JFET. But here, this curve extends for the positive values of gate-to-source voltage (V_{GS}) also. The value I_{DSS} represents the current from drain-to-source with $V_{GS} = 0$. The drain current at any point along the transfer characteristic (*i.e.*, the curve *ABC*) is given by the relation,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

It may be noted that even if $V_{GS} = 0$, the device has a drain current equal to I_{DSS}. Due to this fact, it is called normally-ON MOSFET.

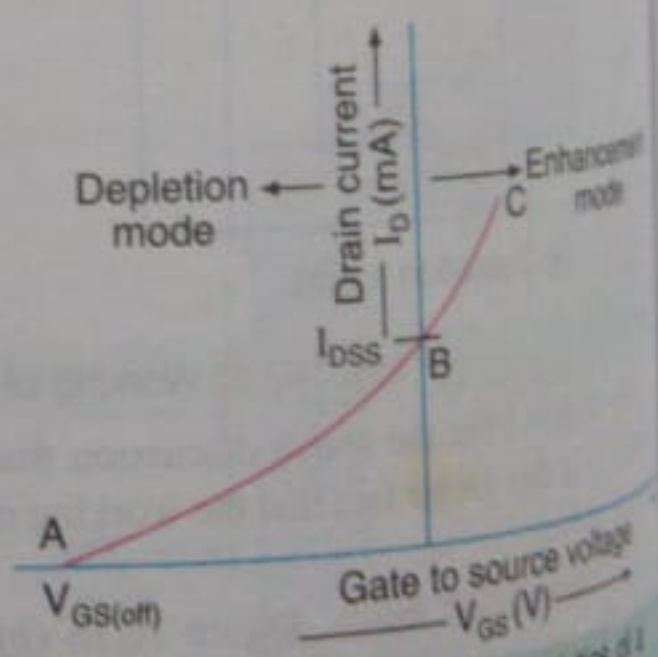


Fig. 16.18. Transfer characteristics of N- channel depletion-type MOSFET

16.20. Circuit Symbol for Depletion-Type MOSFET

Fig. 16.19 (*a*) and (*b*) shows the circuit symbols for the N-channel depletion-type MOSFET. In these figures, a thin vertical line (just right to the gate) represents the channel. The drain and source terminals are connected to the top and bottom of the channel as shown. The arrow, on the P-type substrate, points towards the channel. This indicates that the channel is N-type. In some MOSFET's, a connection from the substrate is also taken out. Such MOSFET's have 4-terminals as indicated in the Fig. 16.19 (*a*). But in most of the MOSFET's the substrate is internally connected to the source. This results in a three terminal device, whose circuit symbol is as shown in Fig. 16.19 (*b*). Fig. 16.19 (*c*) shows the circuit symbol for a P-channel depletion type MOSFET. It may be noted that the symbol is similar to that of N-channel, except the direction of the arrow on the substrate. Its direction is away from the channel, which indicates that the channel is of P-type material.

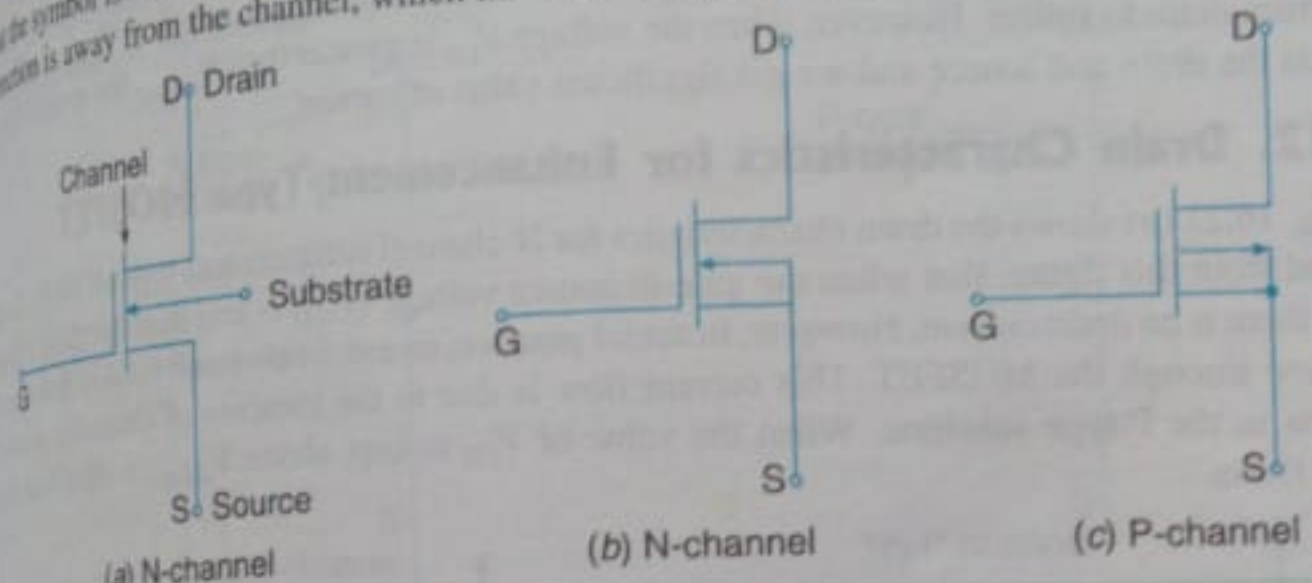


Fig. 16.19. Circuit symbols for depletion type MOSFET'S

16.21. Enhancement-Type MOSFET

The enhancement-type MOSFET has no depletion mode and it operates only in enhancement mode. It differs in construction from the depletion-type MOSFET in the sense that it has no physical channel. Fig. 16.20 (*a*) shows the basic structure of the N-channel enhancement-type MOSFET. It may be noted, that the P-type substrate extends the silicon dioxide layer completely.

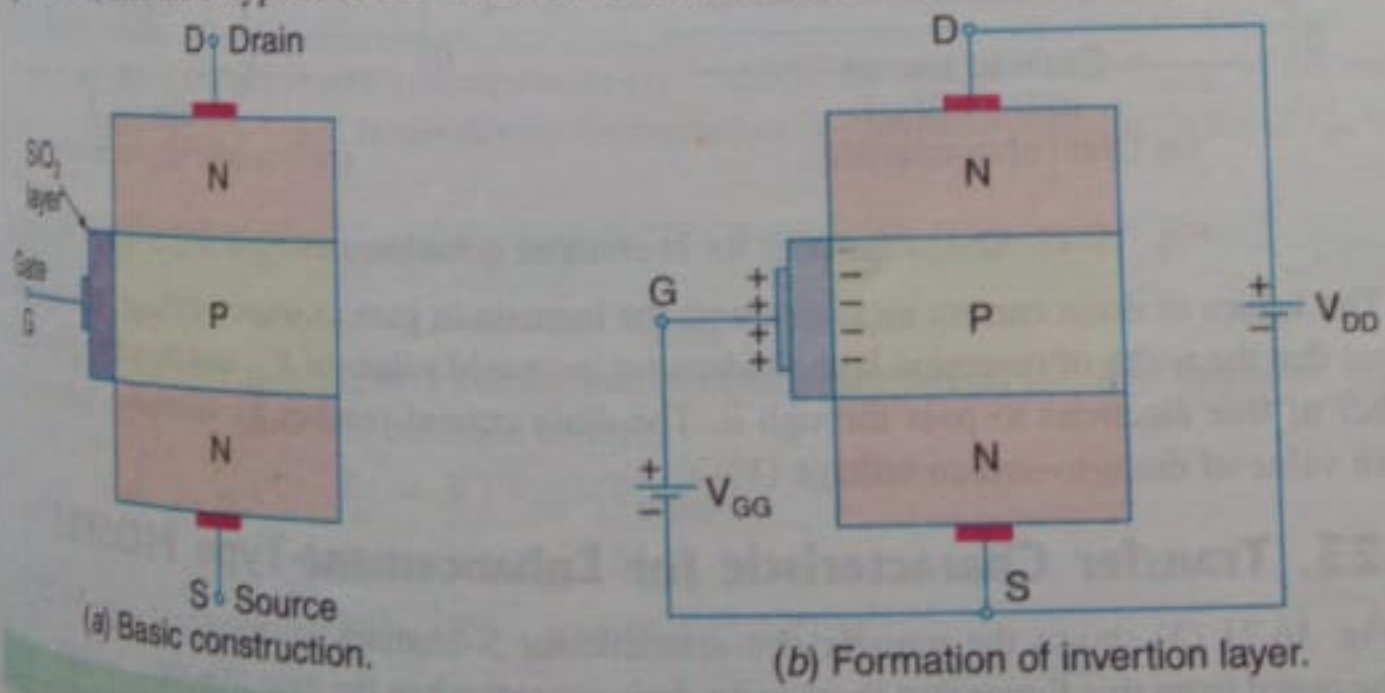


Fig. 16.20. Enhancement type MOSFET.

Fig. 16.20 (*b*) shows the normal biasing polarities for the N-channel enhancement-type MOSFET. It must be remembered that this M OSFET is always operated with the positive gate-to-source voltage V_{GS}. When the gate-to-source voltage is zero, the V_{DD} supply tries to force free electrons from

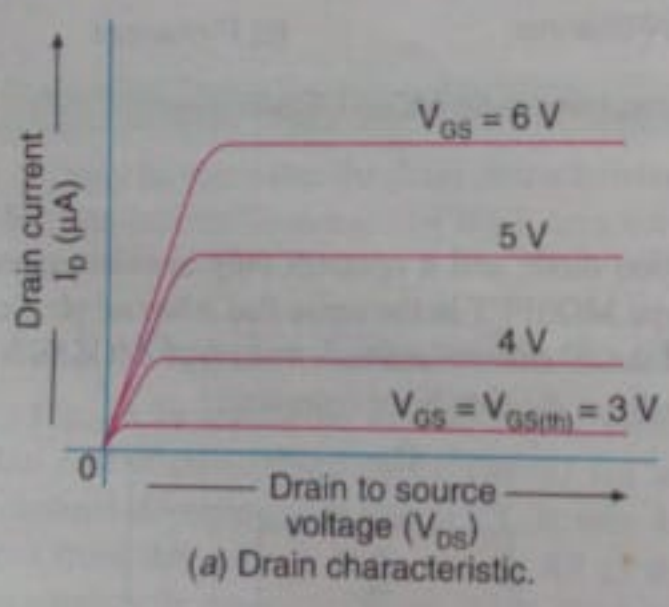
source-to-drain. But the presence of P-region does not permit the electrons to pass through it. Thus there is no drain current for $V_{GS} = 0$. Due to this fact, the enhancement type MOSFET is also called normally-OFF MOSFET.

Now, if some positive voltage is applied at the gate, it induces a negative charge in the P-type substrate just adjacent to the silicon dioxide layer. The induced negative charge is produced by attracting the free electrons from the source. When the gate is positive enough, it can attract a number of free electrons. This forms a thin layer of electrons, which stretches from source to drain. This effect is equivalent to producing a thin layer of N-type channel in the P-type substrate. This layer of free electrons is called N-type inversion layer.

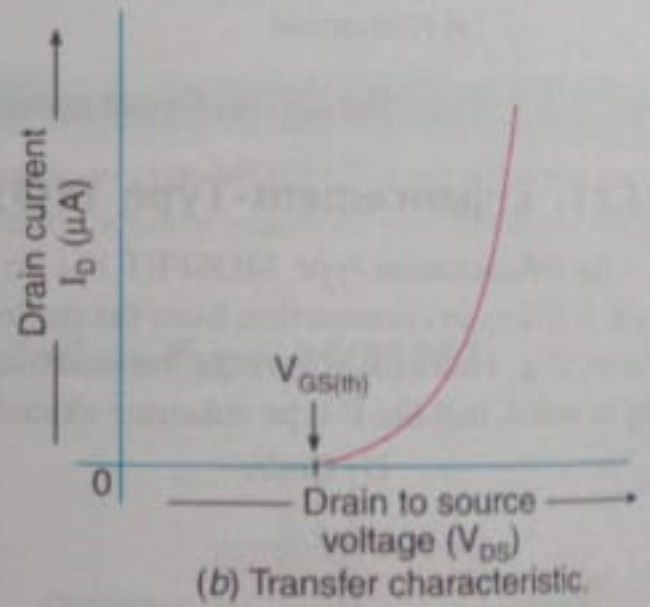
The minimum gate-to-source voltage (V_{GS}), which produces inversion layer, is called threshold voltage and is designated by the symbol $V_{GS(th)}$. When the voltage V_{GS} is less than $V_{GS(th)}$, no current flows from drain to source. However, when the voltage V_{GS} is greater than $V_{GS(th)}$, the inversion layer connects the drain and source and we get significant value of current.

16.22. Drain Characteristics for Enhancement-Type MOSFET

Fig. 16.21 (*a*) shows the drain characteristics for N-channel enhancement-type MOSFET. It may be noted from this figure, that when the gate-to-source voltage (V_{GS}) is less than threshold voltage, $V_{GS(th)}$, there is no drain current. However, in actual practice, an extremely small value of drain current does flow through the MOSFET. This current flow is due to the presence of thermally generated electrons in the P-type substrate. When the value of V_{GS} is kept above $V_{GS(th)}$, a significant drain current flows.



(*a*) Drain characteristic.



(*b*) Transfer characteristic.

Fig. 16.21. Characteristics for N-channel enhancement-type MOSFET.

The values of drain current increases with the increase in gate-to-source voltage. It is because of the fact that the width of inversion layer widens for increased values of V_{GS} and therefore allows more number of free electrons to pass through it. The drain current reaches its saturation value above a certain value of drain-to-source voltage (V_{DS}).

16.23. Transfer Characteristic for Enhancement-Type MOSFET

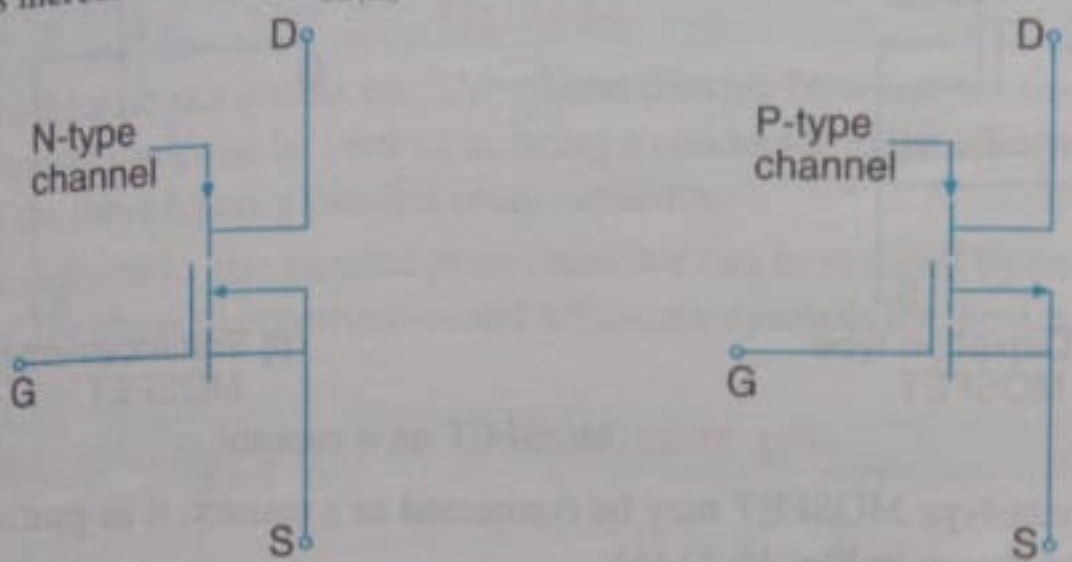
Fig. 16.21 (*b*) shows the transfer characteristic for N-channel enhancement type MOSFET. It may be noted from this figure that there is no drain current when the gate-to-source voltage, $V_{GS} = 0$. However, if V_{GS} is increased above the threshold voltage, $V_{GS(th)}$, the drain current increases rapidly as shown in figure. The drain current at any point along the curve is given by the relation,

$$I_D = K \left[V_{GS} - V_{GS(th)} \right]^2$$

where K is a constant, whose value depends on the type of MOSFET. Its value can be determined from the data sheet by taking specified value of drain current called $I_{D(ON)}$ at the given value of V_{GS} and then substituting these values in the above equation. Incidently, it may be noted that enhancement-type MOSFET does not have an I_{DSS} parameter like JFET and depletion-type MOSFET.

16.24. Circuit Symbol for Enhancement-Type MOSFET

Fig. 16.22 (*a*) shows the circuit symbol for *N*-channel enhancement-type MOSFET. In this figure, the broken line indicates that there is no conducting channel between drain and source, when $V_{GS} = 0$. Due to this fact, this device is also known as "Normally-OFF MOSFET". The drain and source terminals are shown at the top and bottom end of the broken line. The substrate is internally connected to the source as shown. The arrow points in the direction of channel (or inversion layer), which is created when V_{GS} is increased above $V_{GS(th)}$.



(*a*) N-channel. (*b*) P-channel.

Fig. 16.22. Circuit symbols for enhancement-type MOSFET.

Fig. 16.22 (*b*) shows the circuit symbol for the P-channel enhancement-type MOSFET. This symbol is similar to N-channel except that the arrow points outwards. This indicates that the channel (or invertion layer) created in the substrate is of P-type. In actual practice, the N-channel and P-channel enhancement-type MOSFET's are known as NMOS and PMOS field-effect transistors respectively.

Example 16.6.

The data sheet for a certain enhancement-type MOSFET reveals that $I_{D(on)} = 10$ mA at $V_{GS} = -12$ V and $V_{GS(th)} = -3$ V. Is this device P-channel or N-channel? Find the value of I_D when $V_{GS} = -6$ V.

Solution.

Given: $I_{D(on)} = 10$ mA; $V_{GS} = -12$ volts and $V_{GS(th)} = -3$ volts.

Since the value of V_{GS} is negative for the enhancement-type MOSFET, this indicated that the device is P-channel. We know that the drain current,

$$I_D = K [V_{GS} - V_{GS(th)}]^2 \quad ...(i)$$

or

$$I_{D(on)} = K [(V_{GS} - V_{GS(th)})]^2$$

$$\therefore \quad 10 = K [-12 - (-3)]^2 = 81\ K$$

$$K = 10/81 = 0.12 \text{ mA/V}$$

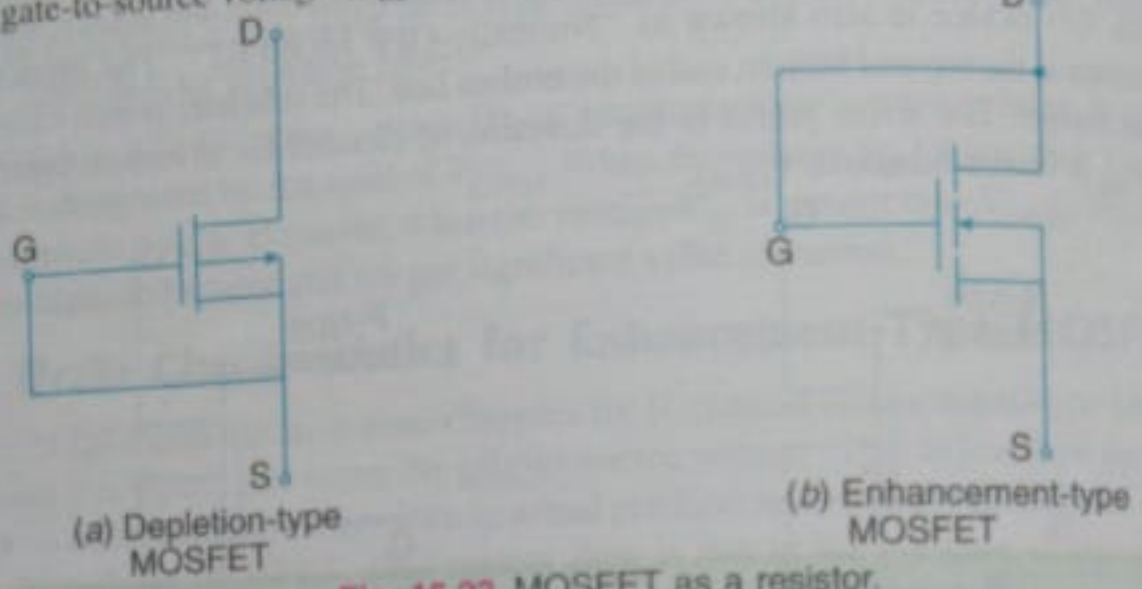
Substituting this value of K and V_{GS} (equal to -6) in the equation (*i*),

$$I_D = 0.12 [-6 - (-3)]^2 = 1.08 \text{ mA}$$ **Ans.**

16.25. The MOSFET as a Resistor

The MOSFET's have an important property that they can be used as a resistor, capacitor, amplifier and a switch. This makes the design of electronic circuits very simple, because the entire circuit consists of only MOSFETs and no other component. The examples of such circuits are microprocessors and memory circuits.

The depletion type MOSFET may be connected as a resistor, if its gate is connected to the source so that the gate-to-source voltage (V_{GS}) is zero, as shown in Fig. 16.23 (*a*).



(*a*) Depletion-type MOSFET (*b*) Enhancement-type MOSFET

Fig. 16.23. MOSFET as a resistor.

The enhancement-type MOSFET may be connected as a resistor, if its gate is connected to the drain so that $V_{GS} = V_{DS}$ as shown in Fig. 16.23 (*b*).

16.26. Advantages of N-Channel MOSFETs Over P-Channel

These days N-channel MOSFETs have become much popular than P-channel for fabricating MOS circuits and systems. The P-channel MOSFETs find their use only in complementary metal oxide semiconductor (CMOS) integrated circuits. The main advantage of N-channel MOSFET over P-channel, is due to the fact that charge carriers in N-channel devices are the electrons, which have a mobility of about 1300 cm^2/V.s. On the other hand, the charge carriers in P-channel devices are the holes which have a mobility of about 500 cm^2/V.s. Since the current, in a semiconductor, is directly proportional to the mobility, therefore the current in a N-channel MOSFET is more than two times that of P-channel for the same dimension.

The ON resistance of the N-channel MOSFET is one-third of that for P-channel. It means that in order to achieve the same value of current and ON resistance, the P-channel MOSFET requires three times the area of an equivalent N-channel MOSFET. Thus electronic currents using N-channel MOSFETs are much smaller in size than those of P-channel. This results in higher packing density.

16.27. Complementary MOSFETS (CMOS)

MOSFETs are used extensively in the field of digital electronics to manufacture logic gates and many other synchronous and asynchronous circuits. The logic gates include AND, OR, NOT gates and their various combinations. The synchronous circuits include flip-flops, counters, memories, A/D and D/A converters. The asynchronous circuits include combination of logic gates such as decoders, encoders, multiplexers and demultiplexers.

A CMOS logic gate consists of a combination of NMOS and PMOS devices. The detailed discussion of CMOS devices is beyond the scope of this book.

16.28. Daul-gate MOSFETs

As a matter of fact, the operation of MOSFETs is limited at high frequencies because of their high gate to-channel capacitance. The cause of this high capacitance can be seen in Fig. 16.24. The metal

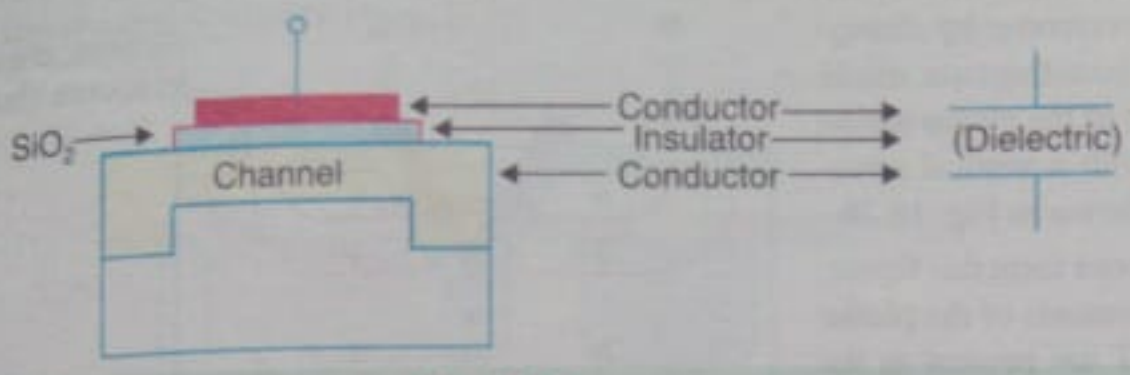


Fig. 16.24.

plate that is used for the gate is a conductor. The silicon dioxide between the gate and the channel in an insulator. The channel itself can be viewed as being a conductor to the silicon dioxide layer. Thus the combination of the three forms a parallel-plate capacitor.

The capacitance offered by this parallel plate capacitor can be reduced by employing a dual gate MOSFET structure. The physical construction and schematic symbols for the dual-gate MOSFET are shown in Fig. 16.25.

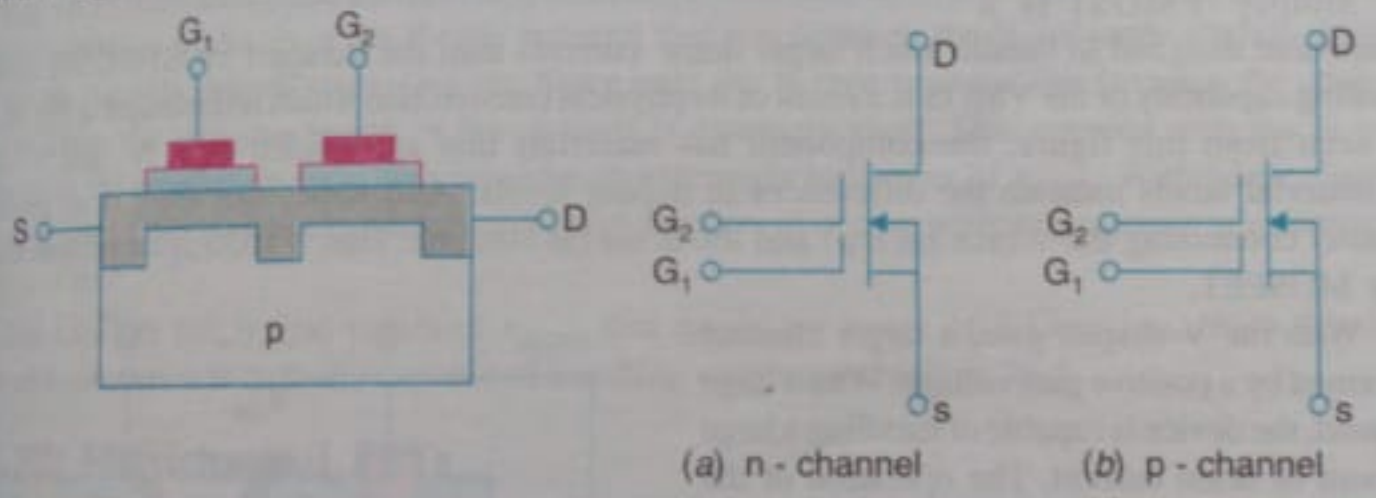


Fig. 16.25.

The reduced capacitance of the dual-gate MOSFET is the result of the way in which the component is used. Normally the component is used in such a way as toact as two series-connected MOSFETs. When the dual gate MOSFET is used as series MOSFETs, the effect is similar to connecting two capacitors in series Recall that the total capacitance in a sries connection is lower than either individual component value. Thus by connecting the two gates in a series configuration, the overall capacitance is reduced. This allows the dual-gate MOSFET to have a better high-frequency response as compared to a normal MOSFET.

16.29. Power MOSFETs

With the advancement of technology, the engineers have produced a wide variety of MOSFETs that are designed specifically for high current, high voltage and high power applications. Some applications for these components are found in cascode amplifiers, RF amplifier, power MOSFET derivers. The detail of these applications is beyond the scope of this book.

Following are some of the power MOSFETs which are important from the subject point of view.

1. Vertival MOSFET (VMOS)
2. Lateral Double-Diffused MOSFET(LDMOS)

Both there power MOSFETs are discussed below one by one in the following pages.

Similarly, drain current when $V_{GS} = -10$ V,

$$I_D = 12\left(1 - \frac{-10}{-20}\right)^2 = 3 \text{ mA}$$

and drain current when $V_{GS} = -15$ V,

$$I_D = 12\left(1 - \frac{-15}{-20}\right)^2 = 0.75 \text{ mA}$$

The value of V_{GS} and the corresponding values of I_D obtained above are shown in Table 16.1.

Table 16.1:

V_{GS} (V)	I_D (mA)
-20	0
-15	0.75
-10	3
-5	6.75
-0	12

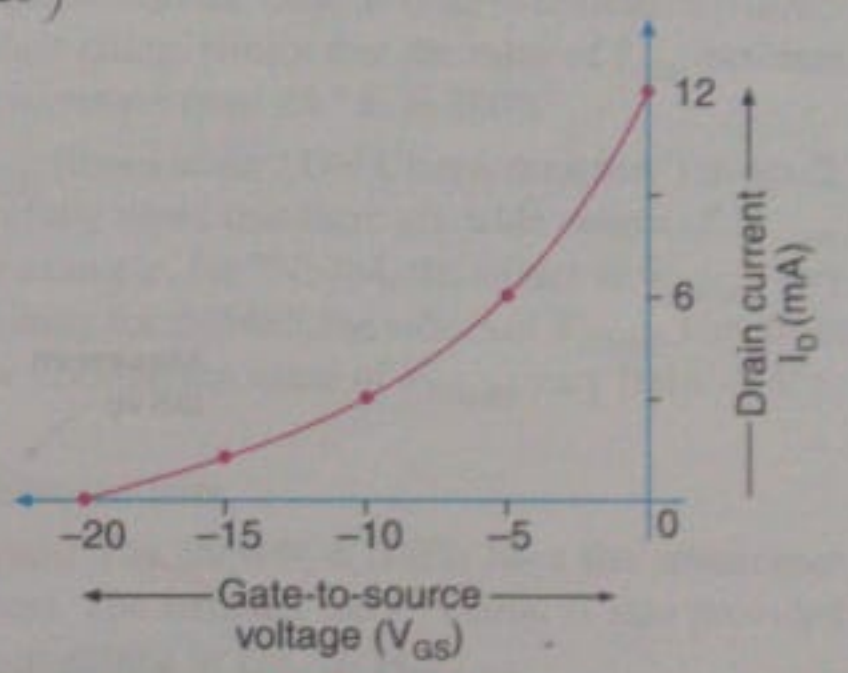


Fig. 16.12.

These points are now plotted and joined together to form a curve shown in Fig. 16.12.

Example 16.3.

A 2N5486 JFET has values of $V_{GS(off)}$ equal to – 2 V to – 6 V and I_{DSS} equal to 8 mA to 20 mA. Plot the minimum and maximum transconductance curves for the device.

Solution:

Given: $V_{GS\,(OFF)} = -2$ V to – 6 V and $I_{DSS} = 8$ mA to 20 mA.

First of all, let us find the values of drain currents for the given values of V_{GS}.

We know that drain current,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad ...(i)$$

Substituting the values of $V_{GS} = -0.5, -1.0$ and -1.5 with $V_{GS\,(off)} = -2.0$ V, we get the corresponding values of $I_D = 4.5$ mA, 2 mA and 0.5 mA. With these values, we have the set of V_{GS} versus I_D value, shown in Table 16.2

Table 16.2:

For minimum transconductance curve

V_{GS}(V)	I_D (mA)
-2.0	0
-1.5	0.5
-1.0	2.0
-0.5	4.5
0	8

Table 16.3:

For maximum transconductance curve

V_{GS}(V)	I_D (mA)
-6	0
-4	2.2
-2	8.9
0	20