DRV8301 Current Limiting Mode Layout Considerations

戴观祖 Garrick Dai South China OEM

ABSTRACT

The DRV8301 is a highly integrated gate driver IC with dual current shunt amplifiers and buck regulator dedicated for three phase motor drive applications. One critical feature of DRV8301 is a current limit mode which can save a lot of external components to realize motor phase current detection and current limit function. The function can be realized by configuring DRV8301 internal registers through SPI interface. However, in practical application, unexpected abnormal reset problem of DRV8301 internal registers can occur with poor PCB layout. This application report explains the DRV8301 current limit function, the unexpected register reset problem, and a detailed analysis with countermeasures to solve the problem.

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1 DRV8301 Brief Introduction

The DRV8301 is three phase motor pre-driver with dual current shunt amplifiers and a buck regulator for three phase motor drive applications. It provides three half bridge drivers, each capable of driving two N-type MOSFETs, one for the high-side and one for the low side. It supports up to 2.3A sink and 1.7A source peak current capability and only needs a single power supply with a wide range from 8 to 60V. The DRV8301 uses bootstrap gate drivers with trickle charge circuitry to support 100% duty cycle. The gate driver uses automatic hand shaking when high side FET or low side FET is switching to prevent current shoot through. Vds of FETs is sensed to protect external power stage during overcurrent conditions.

The DRV8301 includes two current shunt amplifiers for accurate current measurement. The current amplifiers support bi-directional current sensing and provide an adjustable output offset of up to 3V.

The DRV8301 also has an integrated switching mode buck converter with adjustable output and switching frequency to support MCU or additional system power needs. The buck is capable to drive up to 1.5A load.

The SPI interface provides detailed fault reporting and flexible parameter settings such as gain options for current shunt amplifier, slew rate control of gate driver, etc.

1.1 Function Block Diagram

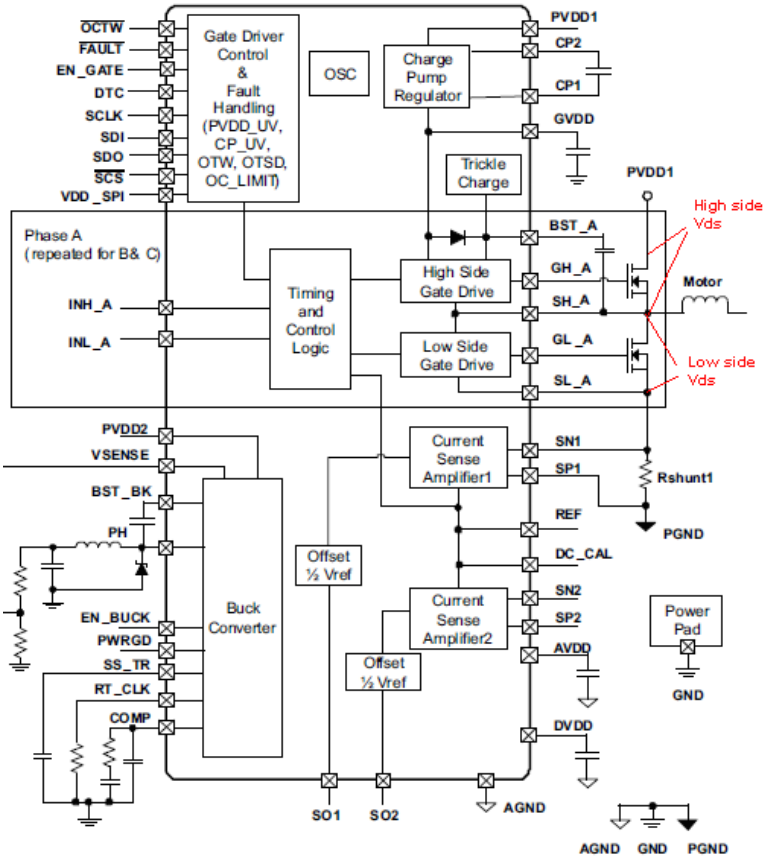

Figure 1. Function Block Diagram

1.2 Over-Current Protection (OCP) and Reporting

The DRV8301 provides over-current and under-voltage protection for the MOSFET power stage. During fault shutdown conditions, all gate driver outputs will be kept low to ensure external FETs are at high impedance state.

To protect the power stage from damage due to high currents, a VDS sensing circuitry is implemented in the DRV8301. Based on the RDS(on) of the external power MOSFETs and the maximum allowed drain-to-source current, a voltage threshold can be calculated which, when exceeded, triggers the OC protection feature. This voltage threshold level is programmable through a SPI command to internal registers.

Additionally, there are a total of 4 OC_MODE settings in SPI that determine how the IC responds to an over-current event.

1.2.1 Current Limit Mode

When current limit mode is enabled, the device operates in a current limiting mode instead of shutting down after detecting an OC event. The over-current event is reported through the OCTW pin. OCTW reporting should hold low during same PWM cycle or for a max 64µs period (internal timer), so external controller has enough time to sample the warning signal. If in the middle of reporting, other FET(s) get OC, then OCTW reporting will hold low and recount another 64µS unless PWM cycles on both FETs have ended.

1.2.2 OC Latched Shutdown Mode

When OC occurs, device will turn off both high side and low side FETs in the same phase if any of the FETs in that phase has an OC event.

1.2.3 Report Only Mode

No protection action will be performed in this mode. OC detection will be reported through OCTW pin and SPI status register. External MCU should take actions based on its own control algorithm. A pulse stretching of 64µS will be implemented on the OCTW pin so the controller can have enough time to sense the OC signal.

1.2.4 OC Disable Mode

Device will ignore all the OC detections and will not report them either.

1.3 SPI Communication

SPI interface is used to set device configuration, operating parameters and read out diagnostic information. The DRV8301 SPI Interface operates in the slave only mode.

The SPI input data (SDI) word consists of 16bit word, with 11 bit data and 5 bit (MSB) command. The SPI output data (SDO) word consists of 16bit word, with 11 bit register data and 4 bit MSB address data and 1 frame fault bit (active 1). When a frame is not valid, frame fault bit will set to 1, and rest of SDO bit will shift out zeros.

1.3.1 SPI Format

SPI input data control word is 16-bit long, consisting of:
- 1 read or write bit W [15]
- 4 address bits A [14:11]
- 11 data bits D [10:0]

SPI output data response word is 16-bit long, and its content depends on the given SPI command (SPI Control Word) in the previous cycle. When a SPI Control Word is shifted in, the SPI Response Word (that is shifted out during the same transition time) is the response to the previous SPI Command (shift in SPI Control Word "N" and shift out SPI Response Word "N-1").

Table 1. SPI Input Data Control Word Format

	R/W	Address				Data										
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	W0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Table 2. SPI Output Data Response Word Format

	R/W	Data														
Word Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Command	F0	A3	A2	A1	A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

1.3.2 SPI Control Register

The MSB bit of SDI word (W0) is read/write bit. When W0 = 0, input data is a write command; when W0 = 1, input data is a read command, and the register value will send out on the same word cycle from SDO from D10 to D0.

Table 3. Register Address

Register Type	Address [A3..A0]				Register Name	Description	Read and Write Access
Status Register	0	0	0	0	Status Register 1	Report occurred faults after previous reading	R (auto reset to default values after read)
	0	0	0	1	Status Register 2	Device ID and report occurred faults after previous reading	Device ID: R Fault report: R (auto reset to default values after read)
Control Register	0	0	1	0	Control Register 1		R/W
	0	0	1	1	Control Register 2		R/W

Control Registers

Table 4. Control Register 1 for Gate Driver Control (Address: 0x02)

Address	Name	Description	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0x02	GATE_CURRENT	Gate driver peak current 1.7A (for slew rate control)										0	0
		Gate driver peak current 0.7A										0	1
		Gate driver peak current 0.25A										1	0
		Reserved										1	1
	GATE_RESET	Normal mode									**0**		
		Reset all latched faults related to gate driver, reset gate driver back to normal operation, reset status register values to default GATE_RESET value will automatically reset to zero after gate driver completes reset									1		
	PWM_MODE	PWM with six independent inputs								**0**			
		PWM with three independent inputs. PWM control high side gates only. Low side is complementary to high side gates with minimum internal dead time.								1			
	OC_MODE (gate driver only)	Current limiting when OC detected						**0**	**0**				
		Latched shut down when OC detected						0	1				
		Report only (no current limiting or shut down) when OC detected						1	0				
		OC protection disabled (no OC sensing and reporting)						1	1				
	OC_ADJ_SET	See OC_ADJ_SET table	X	X	X	X	X						

Over Current Adjustment

When external MOSFET is turned on, the output current flows through the MOSFET, which creates a voltage drop across the drain-to-source (VDS) junction. The overcurrent protection event will be enabled when the VDS exceeds a pre-set value as specified in the register. The VDS trip point can be programmed through SPI command. Assuming the on resistance of MOSFET is RDS(on), the Vds can be calculated as follows:

$$VDS = Ioc \times RDS(on)$$

VDS is measured across the SL_x and SH_x pins for the low-side MOSFET. For the high-side MOSFET, VDS is measured across PVDD1 (internally) and SH_x. Therefore, it is important to limit the ripple on the PVDD1 supply for accurate high-side current sensing. It is also important to note that there can be up to a 20% tolerance across channels for the OC trip point. The VDS sensing scheme is meant for protection and not to be used for regulating current in a motor phase.

Table 5. OC_ADJ_SET Table

Control Bit (D6–D10) (0xH)	0	1	2	3	4	5	6	7
Vds (V)	0.060	0.068	0.076	0.086	0.097	0.109	0.123	0.138
Control Bit (D6–D10) (0xH)	8	9	10	11	12	13	14	15
Vds (V)	0.155	0.175	0.197	0.222	0.250	0.282	0.317	0.358
Control Bit (D6–D10) (0xH)	16	17	18	19	20	21	22	23
Vds (V)	0.403	0.454	0.511	0.576	0.648	0.730	0.822	0.926
Code Number (0xH)	24	25	26	27	28	29	30	31
Vds (V)	1.043	1.175	1.324	1.491	1.679	1.892	2.131	2.400

2 DRV8301 Application On Current Limit Mode(OC)

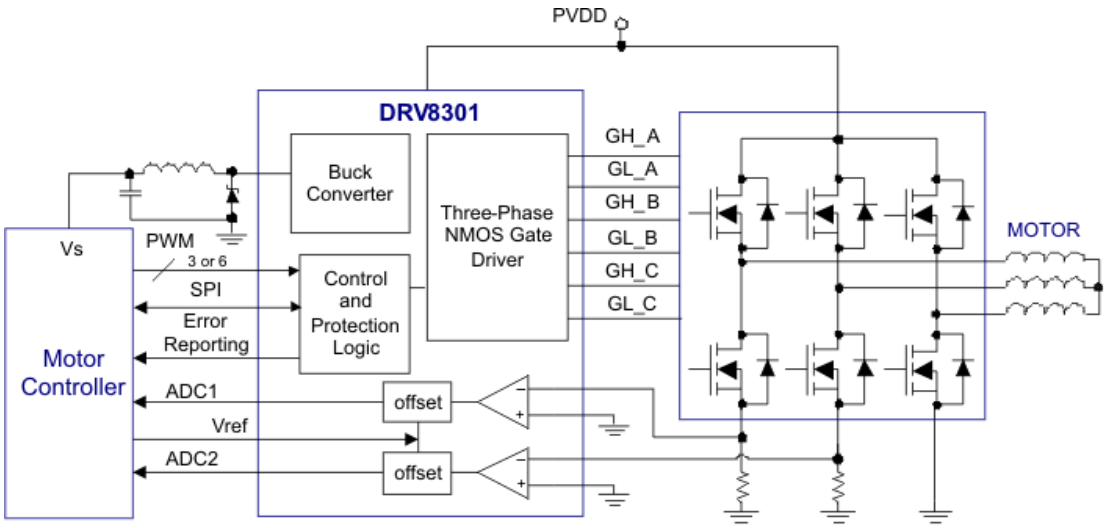

Figure 2. DRV8301 Simplified Application Schematic

Example given conditions for this simplified application solution is as follows:

- Motor : Sensored 3-phase BLDC motor, 24V, 10A(typ.), 20A(peak).

- External Mosfet: Rdson=0.044 ohm.

- Solution use “Current Limit Mode” when OC event occur.

- Set Over Current Limit Point 14.7A.

2.1 Set DRV8301 Control Registers

MCU write DRV8301 SPI to set Control Register 1=0x1500 and Control Register 2 = 0x1840. Control Register 1=0x1500, means binary (0001 0101 0000 0000), from Table 3 and Table 4 —

W0=[0]	// Write command ;
Address [A3:A0] = [0010]	// Control Register1;
Data [D1:D0] = [00]	// Gate driver peak current 1.7A;
Data D2=[0]	// Normal mode;
Data D3=[0]	// PWM with six independent inputs;
Data [D5:D4]=[00]	// Current limiting when OC detected;
Data [D10:D6]=[10100]	// OC_ADJ_SET = 20;

From Tab 5, we know Vds=0.648V(@20) , so from VDS = IOC × RDS(on), calculate IOC = 0.648/0.044 =14.72 A.

2.2 Motor Control Test Routine

Motor Control Test Routine by MCU software is like , 1st Startup motor → Speed up and last 6 seconds → Brake Motor → 2nd Startup motor again → Brake Motor → repeat …

The purpose of routine is to check motor start, brake performance and to check gate driver DRV8301 current limit function performance.

2.2.1 Motor Phase Current Waveform at Normal Situation

The Figure 3. shows motor startup and spin normally and when speed goes higher, the motor phase current goes higher as well and finally is limited near to pre-set value 14.7A. Figure 4 shows the details of motor phase current when scope time is 1ms/Div.

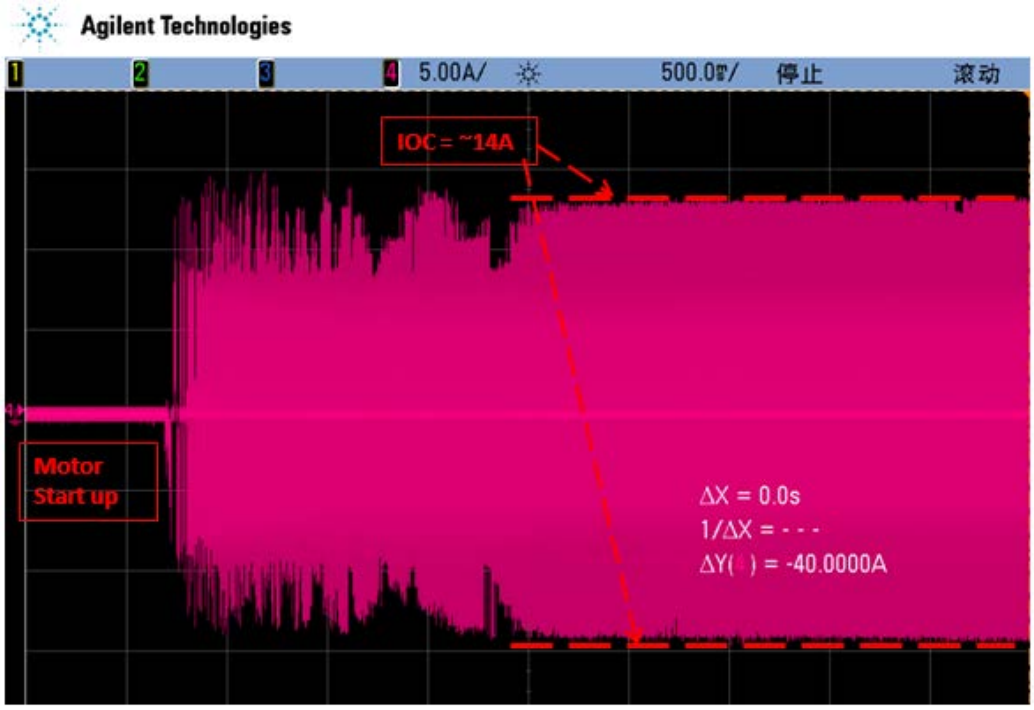

Figure 3. Motor Phase Current (normal situation)

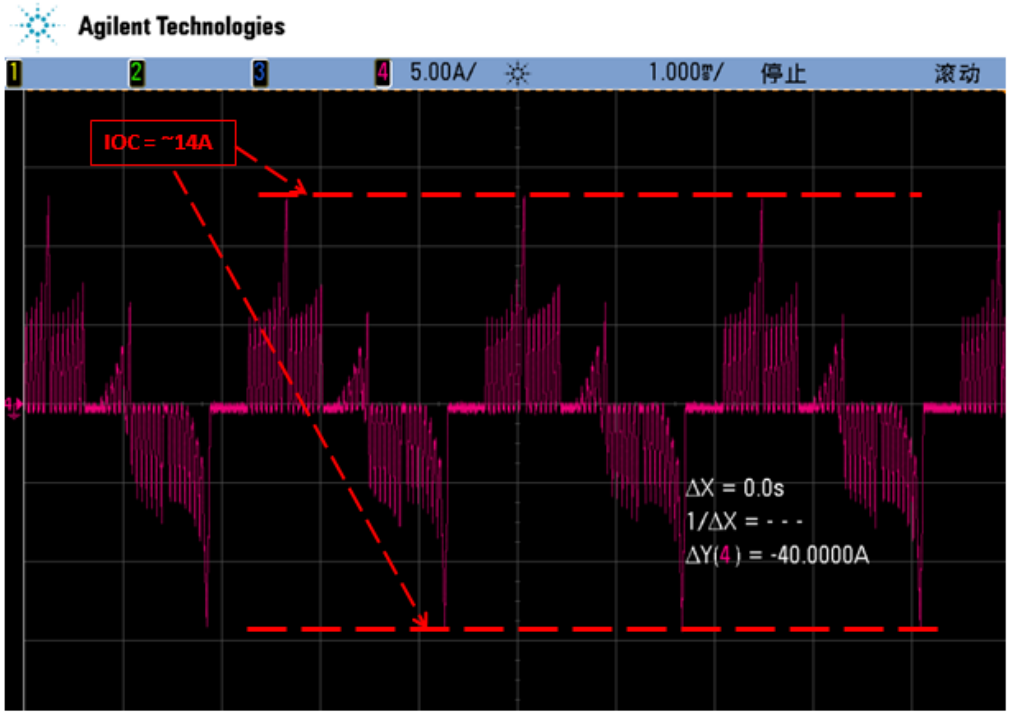

Figure 4. Detail of Motor Phase Current (normal situation)

From above, the DRV8301 current limit function works well and motor works normally as expected.

2.2.2 Motor Phase Current Waveform at Unexpexted Abnormal Situation

However, in some cases when we repeated the test again and again, the unexpected abnormal situation might occur as below. Figure 5 shows, at this time, the motor can startup and run normally for about 5 seconds, but suddenly the current limit change to about 10A unexpectedly.

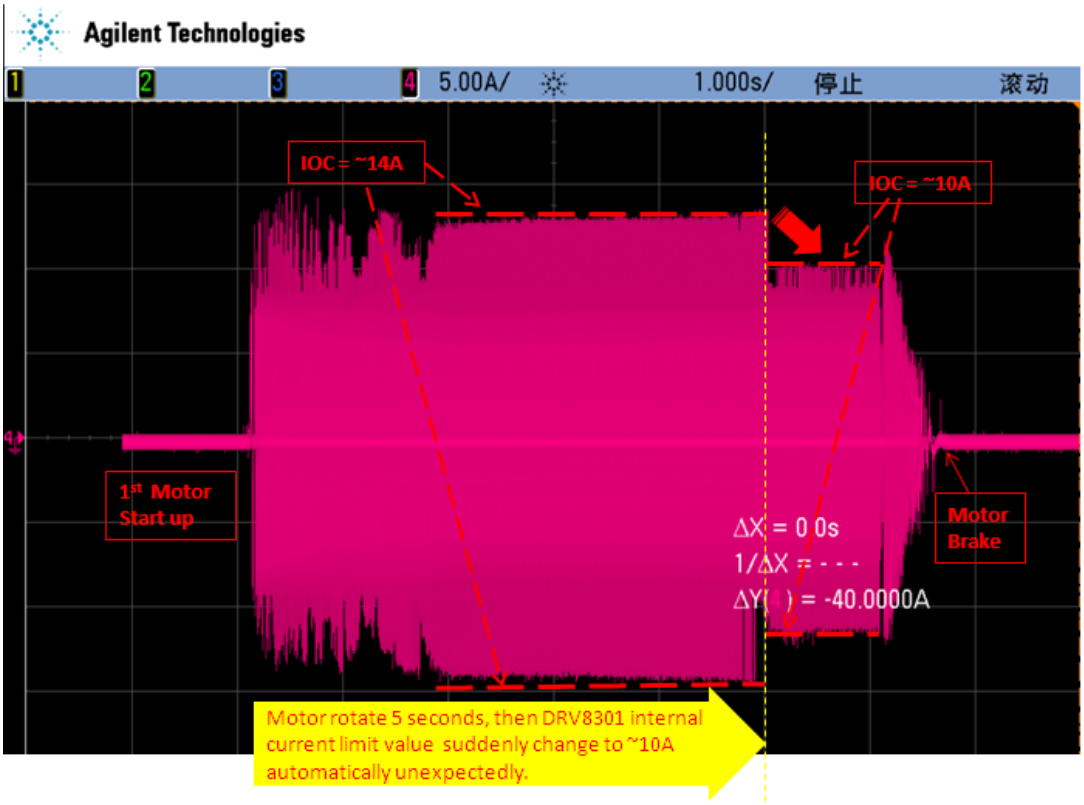

Figure 5. Motor Phase Current of 1st Startup (abnormal situation)

Figure 6 shows the next start-up after the brake shown in Figure 5. The current limit is held at about 10A. The DRV8301 internal Control Register 1 has been re-set to 10A current limit. Figure 7 shows the details of motor phase current when scope time is 1ms/Div.

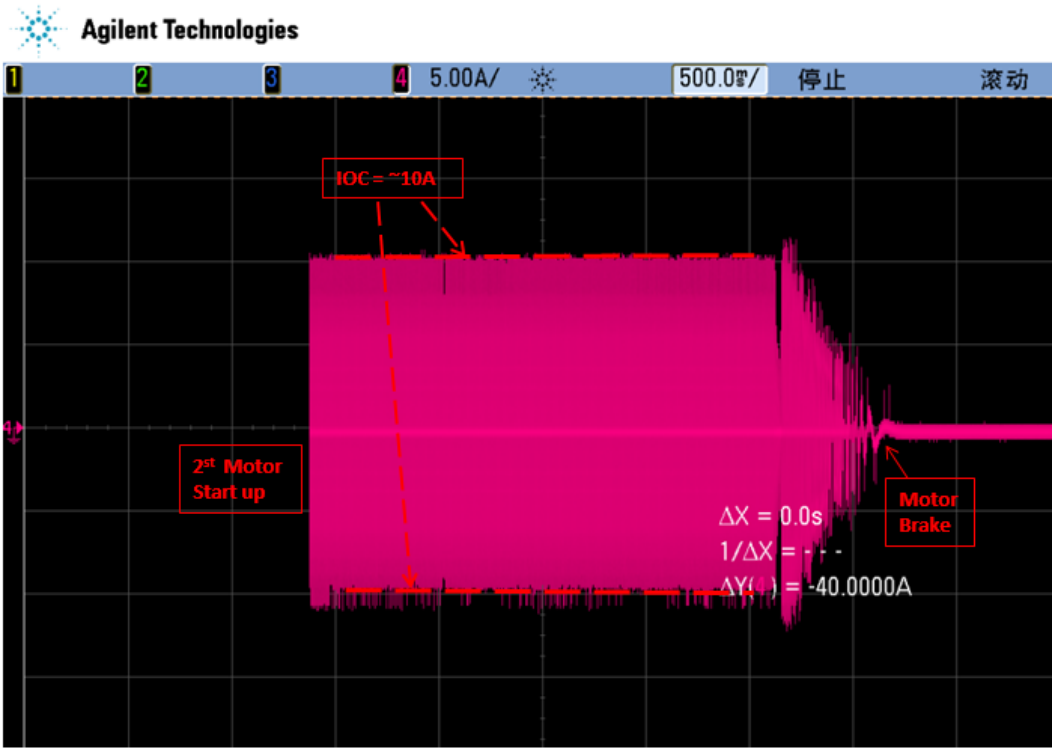

Figure 6. Motor Phase Current of 2nd Startup(abnormal situation)

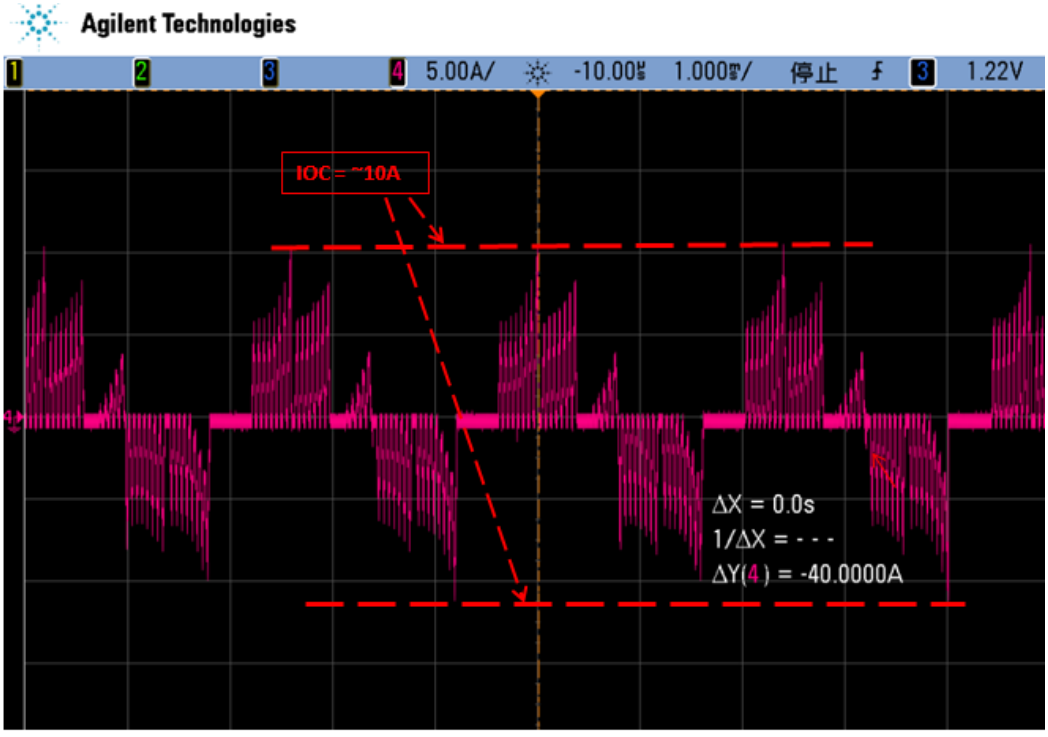

Figure 7. Detail Motor Phase Current (abnormal situation)

2.2.3 Unexpected Abnormal Situation Analysis

From Figure 6&7, it seems DRV8301 internal Control Registers have been reset to default. To prove it, let MCU to read SPI data , then get Control Register 1=0x1400, Control Register 2 = 0x1800, which both are reset to defaut value automatically unexpectedly from pre-set value 0x1500 & 0x1840 respectively. Furthermore, Control Register 1=0x1400(default), means binary (0001 0100 0000 0000), then

Data [D10:D6]=[10000] // OC_ADJ_SET = 16;

From Tab 5, we know Vds=0.403V(@16) , so from VDS = IOC × RDS(on), then IOC = 0.403/0.044 =9.15 A. Considering tolerance, so IOC = ~10A in Figure 7 can meet the analysis, which prove the DRV8301 internal Control Registers have been reset unexpectedly.

The possible reason for this is the DRV8301 DVDD voltage is collapsing suddenly, or big motor phase current circling generates large EMI, and then causing a RESET for DRV8301 internal registers in very short time. If the decoupling for DVDD, AVDD, GVDD, and PVDD is not done properly, then the device may be reset when the supplies drop during heavy load conditions… like high current or braking.

NOTE: DVDD is Internal 3.3V supply voltage. DVDD cap should connect to AGND. AVDD is Internal 6V supply voltage, AVDD cap should connect to AGND. GVDD is internal gate driver voltage regulator. GVDD cap should connect to GND. PVDD is Power supply pin for gate driver, current shunt amplifier, and SPI communication.

2.2.4 Countermeasure for Unexpected Abnormal Situation

To solve the problem, it must need to check circuit and PCB layout. The Figure 8. Is the part of circuit schematic on DRV8301 xVDD decoupling. The Figure 9. is that part's PCB layout.

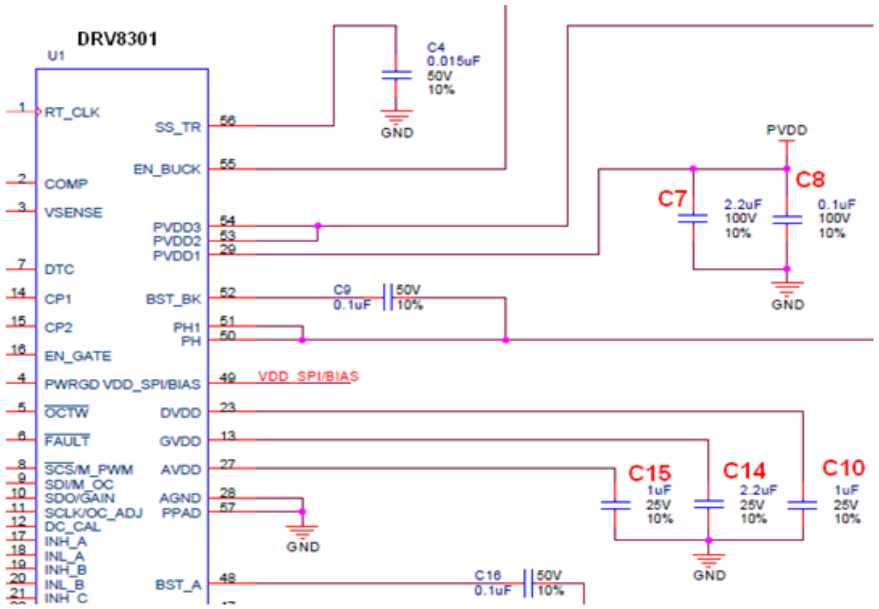

Figure 8. Circuit Schematic(xVDD part)

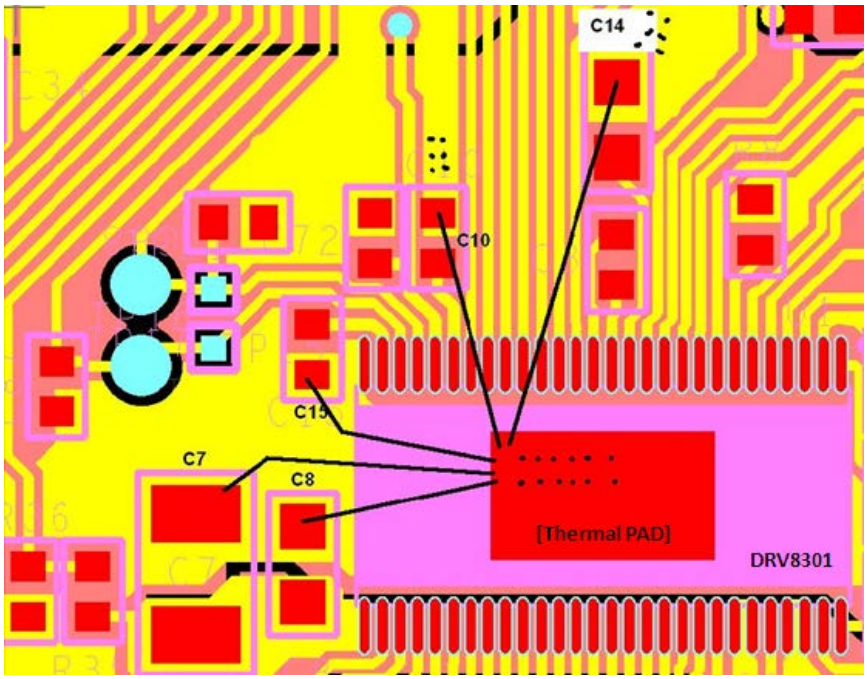

Figure 9. Recommended PCB Layout (part)

The critical components are shown with BLACK silkscreen. C7 and C8 are decoupling for PVDD1. C15 is decoupling for AVDD regulator. C10 is decoupling for DVDD regulator and C14 is decoupling for GVDD regulator. Each of these capacitors needs to have a short path to GND with a “star” connection to the PowerPAD. The exposed PowerPAD on the bottom of the device MUST be soldered to the GND plane in the PCB. BLACK lines showing the current path for

GND current. Vias that connect to the bottom layer of the 2-layer PCB are shown with BLACK dots.

After modifying PCB, the problem has been solved successfully with same software routine and test procedure. It finally proves the root cause of the problem and proper layout addresses the problem.

3 Conclusion

This application report explain details how to setup the DRV8301 current limit function for the motor driver system and demonstrates the problem of the DRV8301 internal registers automatically reset unexpectedly when applying inappropriate PCB layout. The report also explains through detailed analysis how to work out the countermeasure to solve the problem. From it, the user can understand how to use DRV8301 current limit mode, and how to solve and avoid this internal register automatic reset problem.

4 Reference

1. Three Phase Pre-Driver with Dual Current Shunt Amplifiers and Buck Regulator (SLOS719)
2. *InstaSPIN™ BLDC Lab* (*SPRABN7*)

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