Dymin_FPGA_Main.vi
Q:\GitHub\DyminSTED4all\LabviewCode\Dymin_FPGA_Main.vi
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Step before step with tn=0 is the last Dymin Step, threshold is ignored on last step, just count APD counts in selected time
These times are in units of the 80 MHz clock cycle for the SCTLs
16=200ns
32=400ns

Reminder:These "Volts" are actually in bits. Use the RT_Main vi to run this code by inputting actual Volts. Floats aren't possible in an FPGA program.

AOM Volts

nominal 12 bit ADC volts
.1=82
.2=164
.3=246

	AOM Volts	Threshold (counts)	Time (#80MHz periods)
0	0	0	32
1	82	0	32
2	164	0	32
3	246	0	32
4		0	0
5		0	0
6		0	0
7		0	0

16=200ns
32=400ns

PIX CLK (bits)
0

Dymin On?

stop 1
STOP

stop 2
STOP

stop 3
STOP

stop 4
STOP