



Dymin_RT_Main.vi

Q:\GitHub\DyminSTED4all\LabviewCode\Dymin_RT_Main.vi

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Calibrate_enum.ctl

Requirements:

Labview 2016 (32 bit)

Labview Real-Time Module

Labview FPGA Module

Compile Cloud access (Sign up at <https://www.ni.com/en-us/support/documentation/supplemental/14/compile-faster-with-the-labview-fpga-compile-cloud-service.html>)

OR Xilinx Compilation Tools to compile the code on your FPGA.

Instructions:

1. Check the myRIO target IP address in the project and make sure the target IP address is correct.
2. Run this VI.

AOM Voltages:

IN0=A/AO0

IN1=C/AO1

IN2=C/AO0

IN3=A/AO0

Voltage conversion (raw voltages from FPGA):

MSP Connectors:

Voltage=RawDataValue*4.883 mV

MXP Connectors:

Voltage=RawDataValue*1.221 mV

Measured with 50Ohm

Voltage=RawDataValue*2.1mV

I have calibrated the program to the voltage output into
50 Ohms, you will need to calibrate it to your system.

SET YOUR PIXEL CLOCK TO THIS VALUE

PIX CLK period (us)

0

PIX CLK period (bits)

0

PIX CLK Measured (us)

0

PIX CLK Measured (bits)

0

AOM Units

Voltage (Volts) ☐ Power (mW) ☐

AOM P or V

0 0 0.08 0 0 0

Threshold (counts)

0 0 0 0 0

DyMIN Step Time (us)

0 0 0 0 0

Size of time bits
1 bit=12.5 ns

AOM Voltage

0 0 0.08 0 0

Stop

Dymin On?

Laser Wait (us)

0

Wait time for laser power to change

Calibrate?

Use Voltage Only

error in

status ☒ code 0

source

error out

status ☒ code 0

source

Steps including dummy steps

All Step Times (us)

0

0 0 0 0 0 0 0 0 0 0 0 0

Time (#80MHz periods)

0

0 0 0 0 0 0 0 0 0 0 0 0