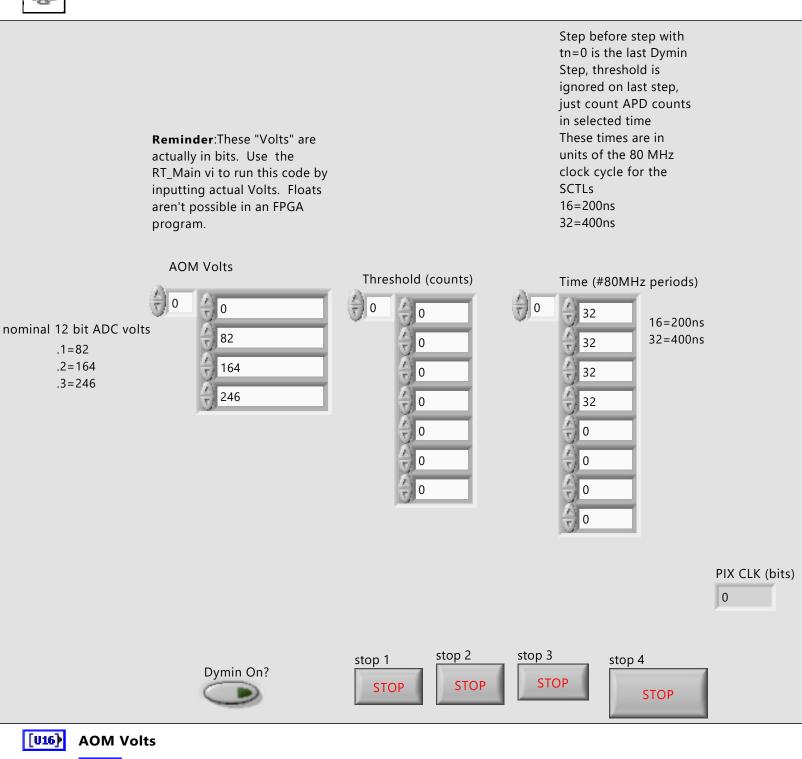
Dymin_FPGA_Main.vi





U16 AOM Volts

U16 Max AOM Voltage

[132] Threshold (counts)

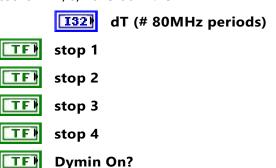
[132] Theshold (counts)

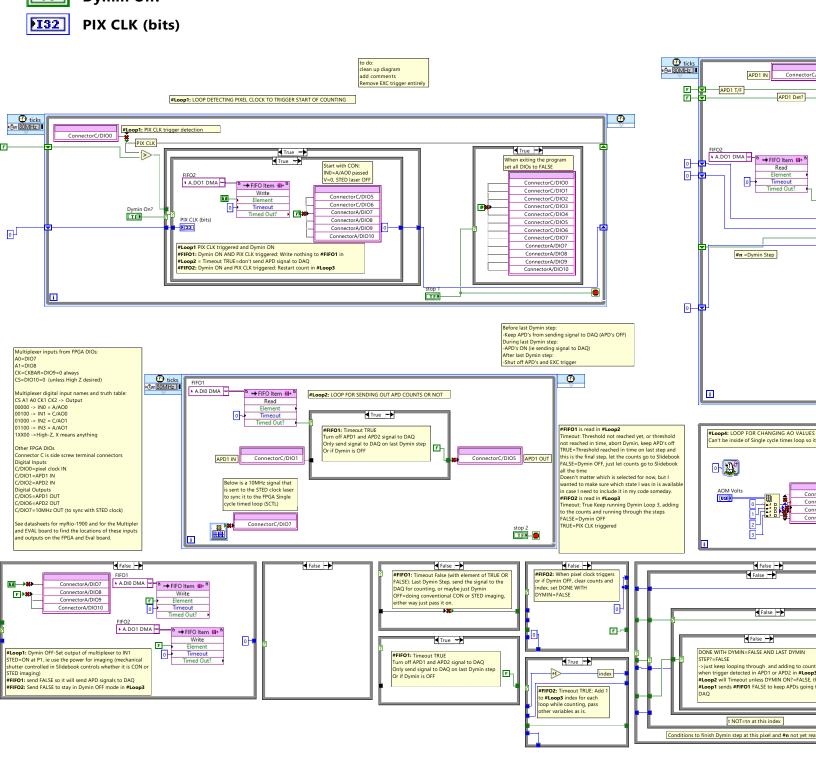
[132] Time (#80MHz periods)

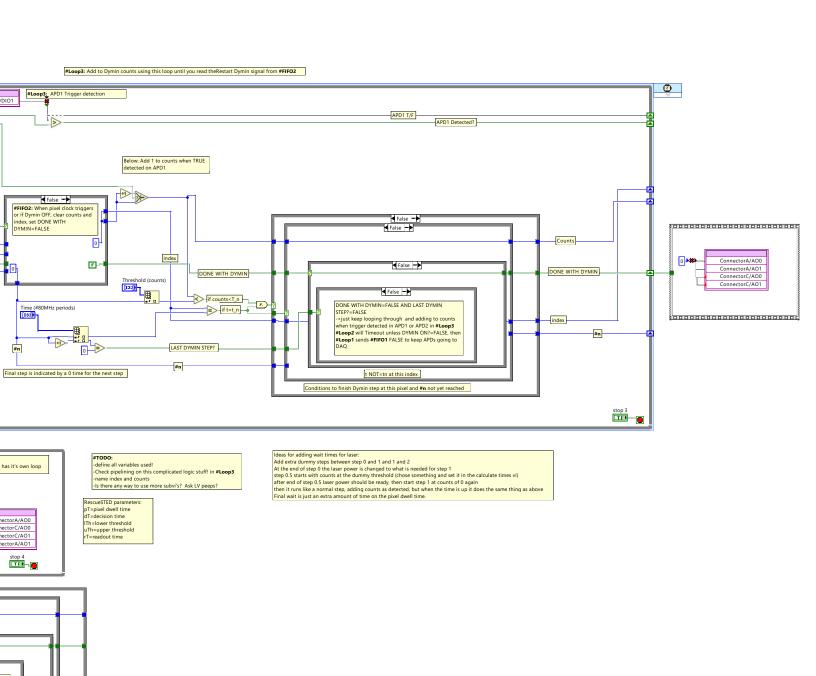
Q:\GitHub\DyminSTED4all\LabviewCode\Dymin_FPGA_Main.vi

Last modified on 7/24/2023 at 12:39 PM

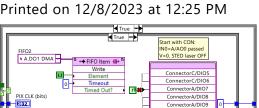
Printed on 12/8/2023 at 12:25 PM



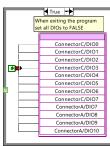


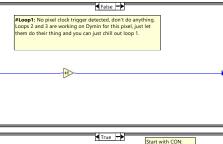


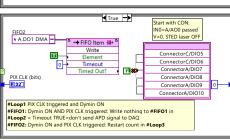
Dymin_FPGA_Main.vi Q:\GitHub\DyminSTED4all\LabviewCode\Dymin_FPGA_Main.vi Last modified on 7/24/2023 at 12:39 PM

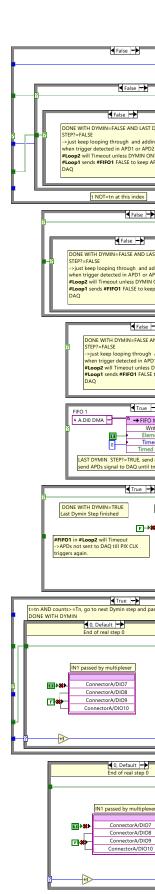


#Loop1 PIX CLK triggered and Dymin ON
#FIFO1: Dymin ON AND PIX CLK triggered: Write nothing to #FIFO1 in
#Loop2 = Timeout TRUE =don't send APD signal to DAQ
#FIFO2: Dymin ON and PIX CLK triggered: Restart count in #Loop3

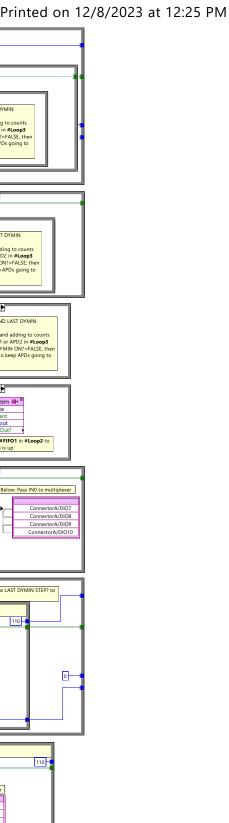




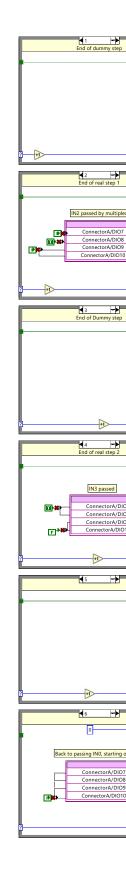




Dymin_FPGA_Main.vi Q:\GitHub\DyminSTED4all\LabviewCode\Dymin_FPGA_Main.vi Last modified on 7/24/2023 at 12:39 PM









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