AVLSI

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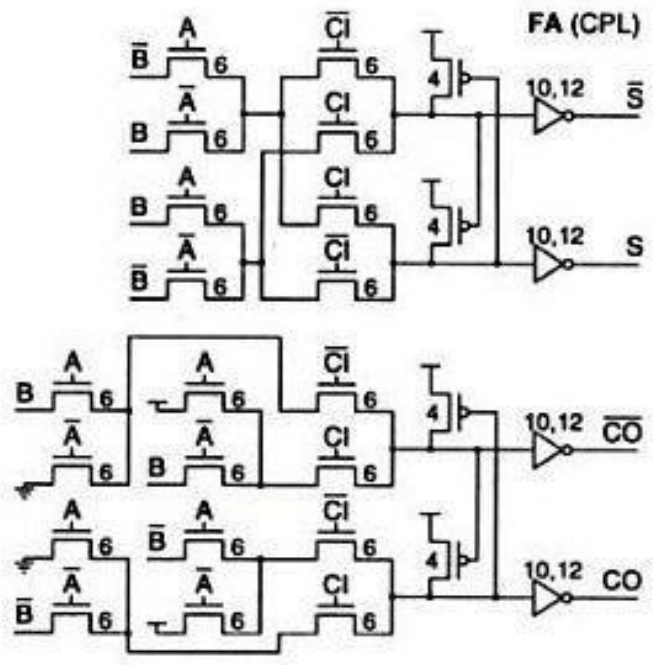
Complementary Pass Transistor Logic full adder:

The Complementary Pass Transistor Logic style is a well-known low power logic style. The CPL style uses NMOS pass transistors to implement logic and eliminates the PMOS transistors completely. The use positive feedback and NMOS transistors only makes the circuit naturally fast.

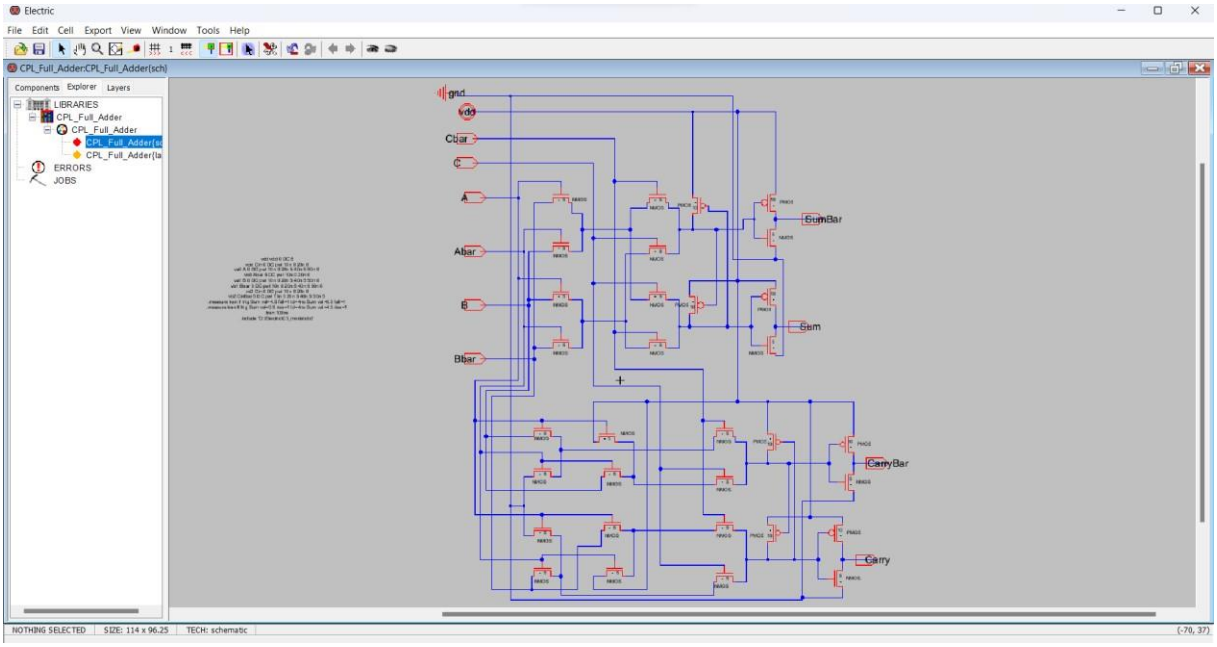
CPL Full Adder Circuit Diagram:



Truth Table:

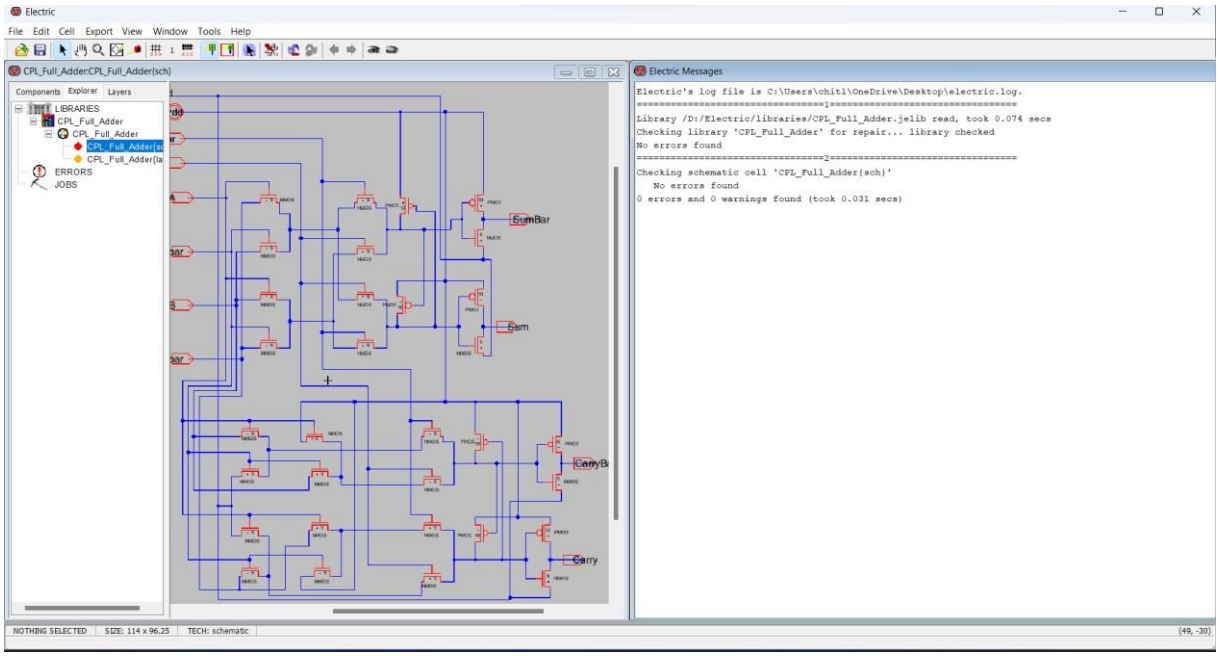
Inputs			Outputs	
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Schematic Design:

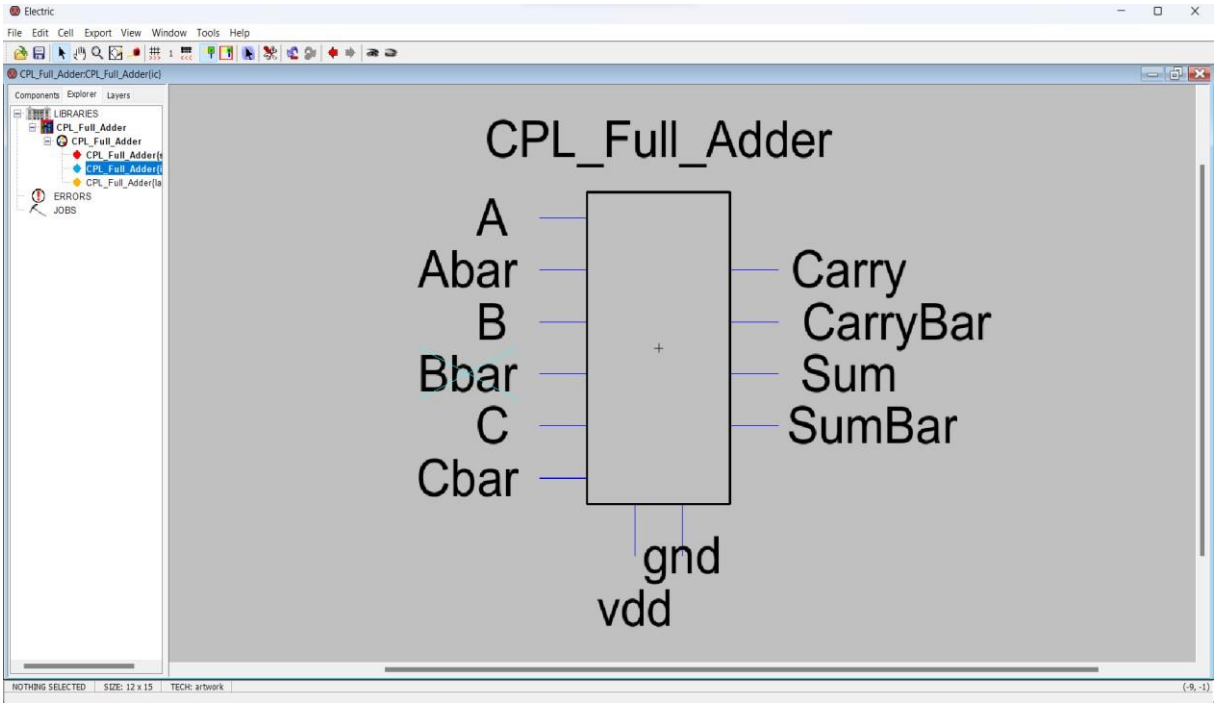


Design Rule Checking (DRC) verifies as to whether a specific design meets the constraints imposed by the process technology to be used for its manufacturing. DRC checking is an essential part of the physical design flow and ensures the design meets manufacturing requirements and will not result in a chip failure.

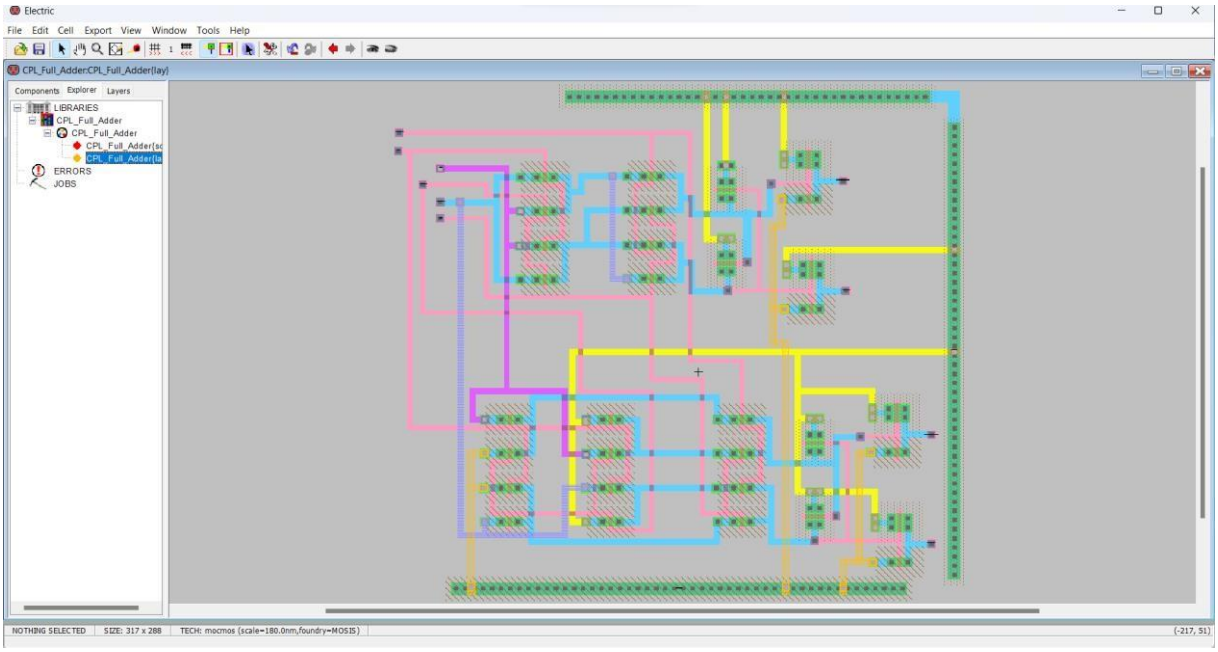
DRC Check:



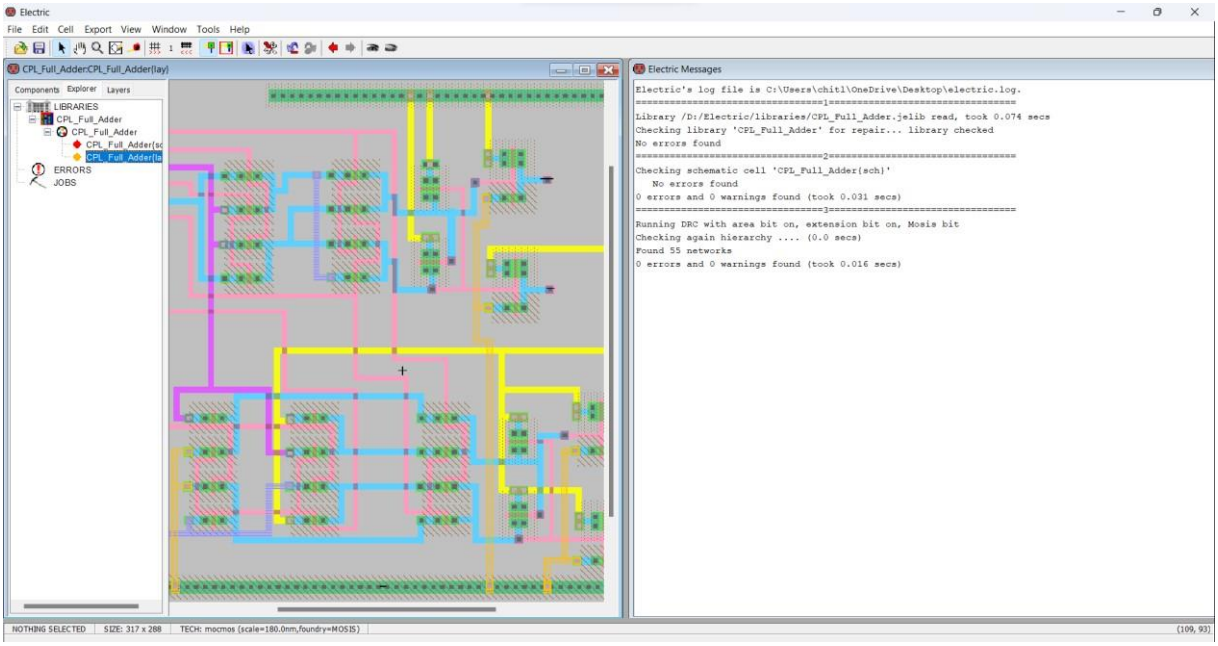
Icon:



Layout Design:

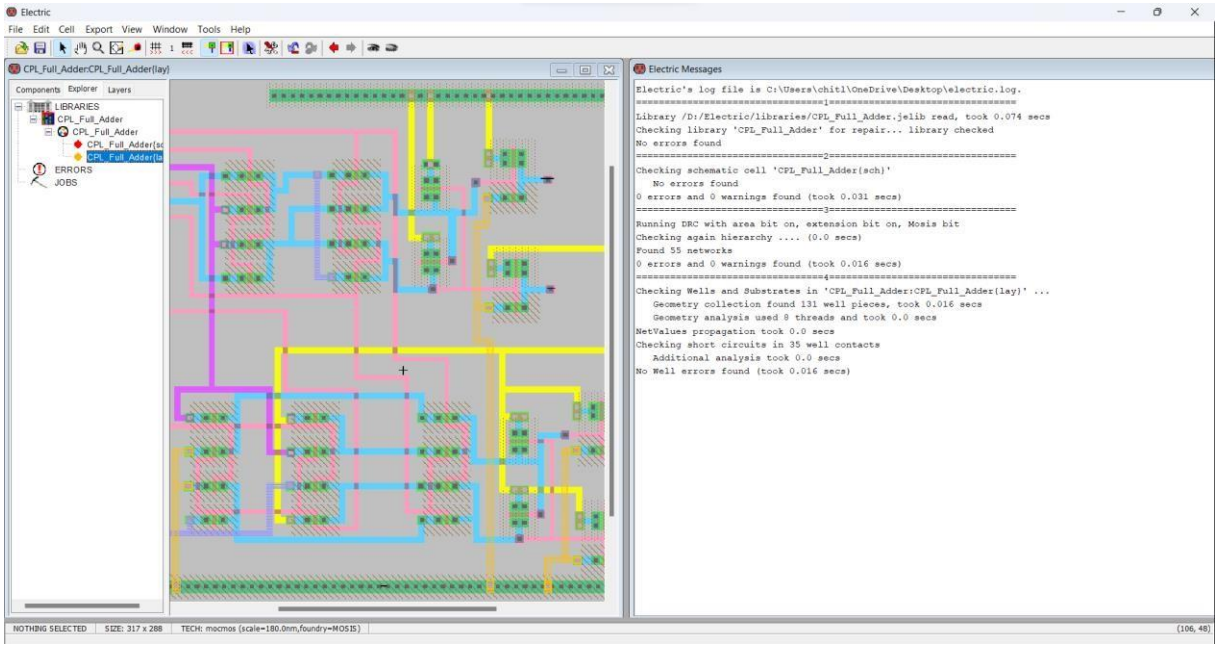


DRC Check:

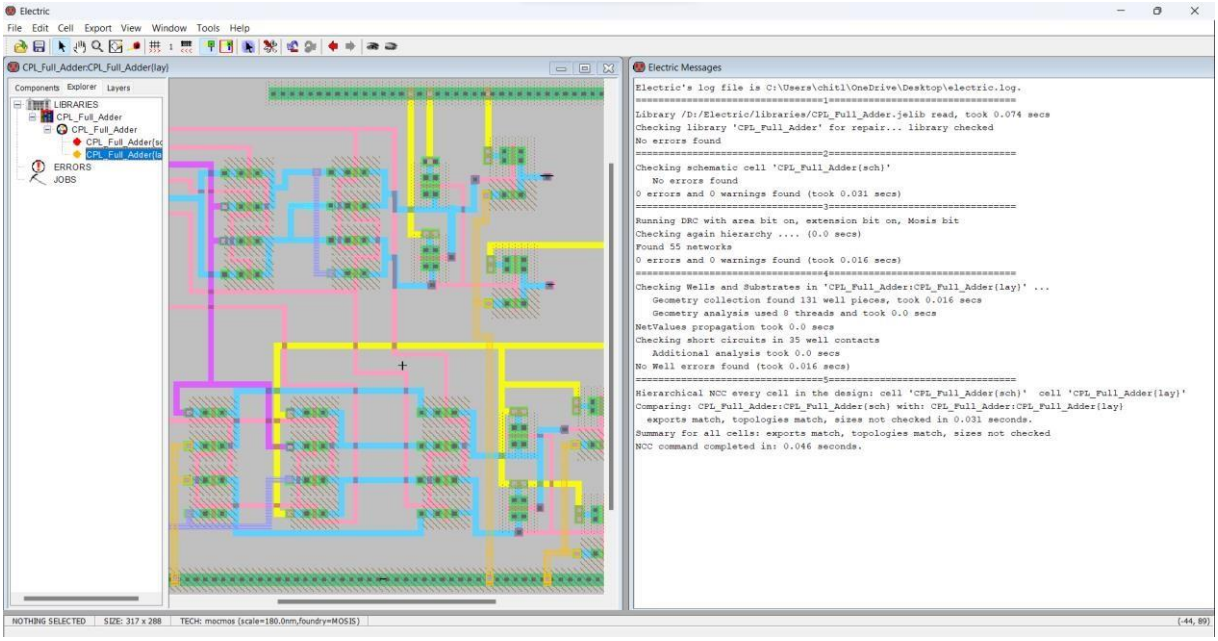


Electrical rule checking (ERC) is a methodology used to check the robustness of a design both at schematic and layout levels against various “electronic design rules”. These design rules are often project-specific and developed based on knowledge from previous tapeouts or in anticipation of potential new failures.

ERC Check:



NCC Check:



VERILOG CODE :

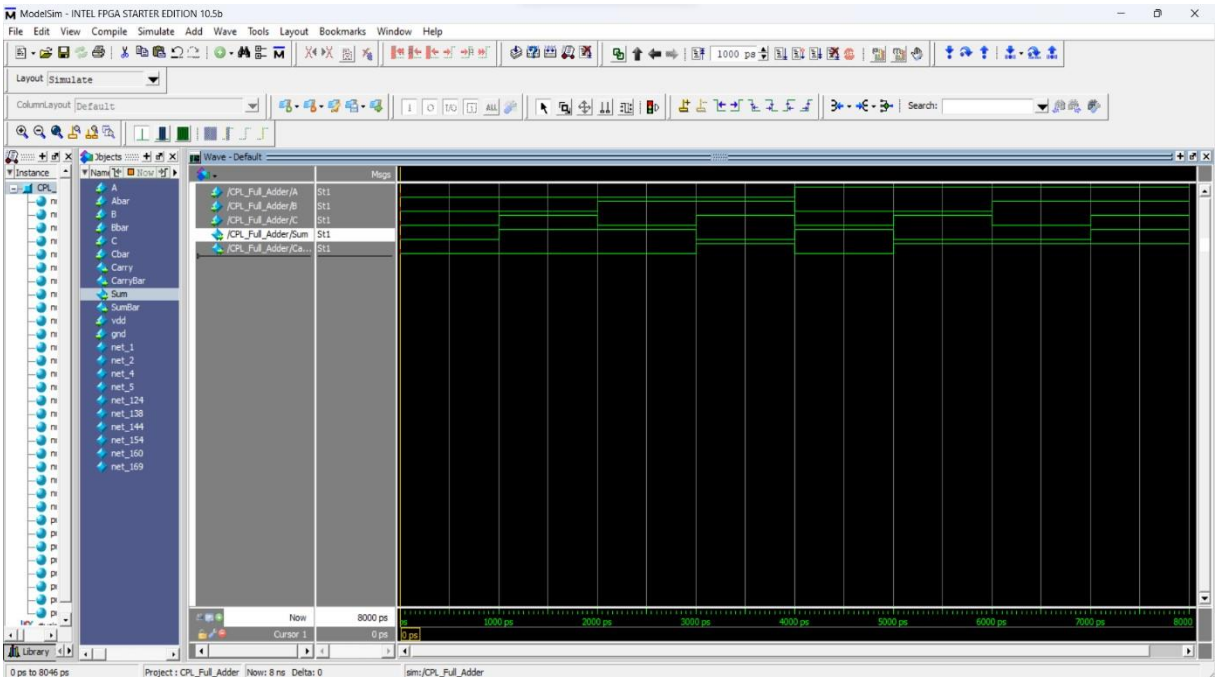
```
/* Verilog for cell 'CPL_Full_Adder:CPL_Full_Adder{lay}' from library 'CPL_Full_Adder' */
/* Created on Fri Mar 24, 2023 15:10:26 */
/* Last revised on Sat Mar 25, 2023 09:58:15 */
/* Written on Sat Mar 25, 2023 09:59:40 by Electric VLSI Design System, version 9.07 */

module CPL_Full_Adder(A, Abar, B, Bbar, C, Cbar, Carry, CarryBar, Sum, SumBar,
vdd, gnd);  input A;  input Abar;  input B;  input Bbar;  input C;  input Cbar;
output Carry;  output CarryBar;  output Sum;  output SumBar;  input vdd;
input gnd;

 supply1 vdd;  supply0 gnd;  wire net_1, net_2, net_4, net_5, net_124,
net_138, net_144, net_154, net_160;  wire net_169;

 tranif1 nmos_0(net_1, Bbar, A);
tranif1 nmos_1(net_1, B, Abar);
tranif1 nmos_2(net_2, B, A);  tranif1
nmos_3(net_2, Bbar, Abar);  tranif1
nmos_4(net_5, net_1, Cbar);  tranif1
nmos_5(net_5, net_2, C);  tranif1
nmos_6(net_4, net_1, C);  tranif1
nmos_7(net_4, net_2, Cbar);  tranif1
nmos_8(SumBar, gnd, net_5);  tranif1
nmos_9(Sum, gnd, net_4);  tranif1
nmos_10(net_124, B, A);  tranif1
nmos_11(net_124, gnd, Abar);
tranif1 nmos_12(net_138, gnd, A);
tranif1 nmos_13(net_138, Bbar,
Abar);  tranif1 nmos_14(net_144,
vdd, A);  tranif1 nmos_15(net_144, B,
Abar);  tranif1 nmos_16(net_154,
Bbar, A);  tranif1 nmos_17(net_154,
vdd, Abar);  tranif1
nmos_18(net_160, net_124, Cbar);
tranif1 nmos_19(net_160, net_144,
C);  tranif1 nmos_20(net_169,
net_154, Cbar);  tranif1
nmos_21(net_169, net_138, C);
tranif1 nmos_22(CarryBar, gnd,
net_160);  tranif1 nmos_23(Carry,
```

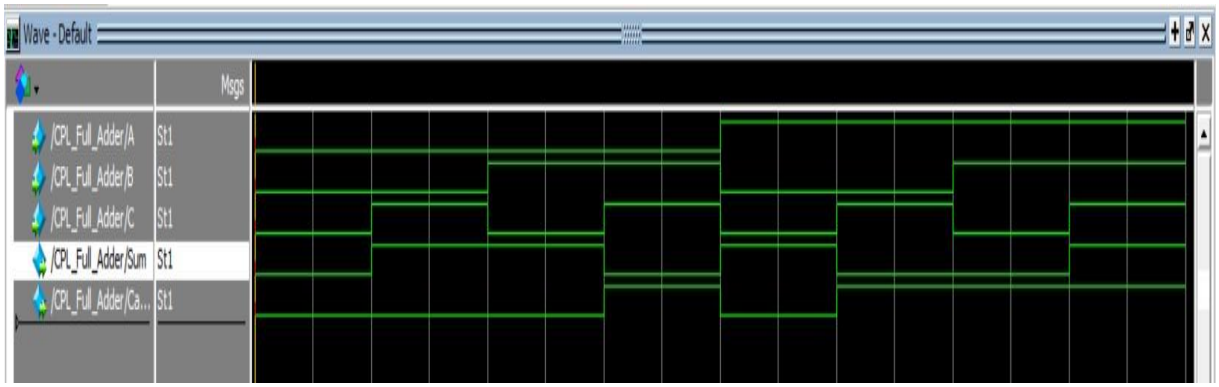
```
gnd, net_169);   tranif0
pmos_0(SumBar, vdd, net_5);   tranif0
pmos_1(net_4, vdd, net_5);   tranif0
pmos_2(net_5, vdd, net_4);   tranif0
pmos_3(Sum, vdd, net_4);   tranif0
pmos_4(CarryBar, vdd, net_160);
tranif0 pmos_5(net_169, vdd,
net_160);   tranif0 pmos_6(net_160,
vdd, net_169);   tranif0 pmos_7(Carry,
vdd, net_169); endmodule   /*
CPL_Full_Adder */
```

Results:

Simulations in ModelSim – INTEL FPGA starter edition Software

1) Compiled the Verilog code in ModelSim and simulated to get waveforms.
2) Waveforms for A, B, C, Sum and Carry respectively for all possible 3bit (8) inputs.





Conclusions:

- W/L of NMOS = 5/2.
- W/L of PMOS = 10/2.
- W/L ratio of PMOS to NMOS = 2.
- Minimum spacing between actives and polysilicon 3micrometers.
- Zero DRC errors.
- Zero ERC errors.
- No NCC errors.
- Used PMOS and NMOS to build not gate.
- Total Number of Transistors: 24 NMOS + 8 PMOS = 32.
- Got familiar with Electric Tool and ModelSim Software.

Contribution:

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- Layout design with DRC, ERC, NCC check.
- Compilation of Verilog code.
- Simulation of design in ModelSim Software.
- Waveforms.