GAP NOTE 2003-021

THE HIGH VOLTAGE TEST BENCH CHARACTERIZATION OF PRE-PRODUCTION MODULES

M. Aglietta[1], W. Fulgione[1], F. Gomez[1], C. Morello[1], G. Navarra[2] and C.Vigorito[2]

[1]Istituto di Fisica dello Spazio Interplanetario and INFN Torino, ITALY
[2]Dipartimento di Fisica Generale - Università di Torino and INFN Torino, ITALY

ABSTRACT

A test bench facility has been designed to characterize the HV modules selected for the Auger Surface Detector. This document reports on the implemented test bench, the used testing procedures, and the analysis of test results, concerning the measurement of the requested specifications for the pre-production HV power supplies (dc-dc converters).

1. DC-DC CONVERTER REQUIREMENTS

Table 1 shows the main specifications required for dc-dc converters (see left side of table 1) to be mounted on the photomultiplier bases of the AUGER Surface Detector. The given characteristics are measured in the assumed operational range [1] and within the requested accuracy (see right side of table 1) by means of the test bench and related procedures described in the following.

Required Module Specifications	*Range & Accuracy*
Main Voltage Supply	**Vcc=12 V ± 5%**
Temperature Range	**-10 < T < 70 ^{o}C**
Output Voltage Vout	**Vmin=0 < Vout < Vmax=2100 V**
Input Command Vcin	**Analog 0 < Vcin < 2.5 V (Vcin=2.5 V @ Vmax)**
Output Voltage Monitor Vmon	**Analog 0 < Vmon < 5 V (Vmon=5 V @ Vmax)**
Allowed Vout Fluctuation vs Vcc: ΔVout/Vout	**<1 $^{0}/_{00}$ @ Vout > 500 V**
Power Absorption	**Pabs < 500 mW @ Vmax for Imax=100 μA**
Ripple	$<2\cdot10^{-5}$ **@ Max Load (20 MΩ)**
Termal Stability $\frac{\Delta Vout}{Vout\cdot T}$	$<10^{-4}/^{0}C$
Integral Non Linearity for Vout vs Vcin relation	$<2\cdot10^{-3}$ **@ Vout > 500 V**
Uniformity of output voltage Vout for a constant Vcin command	$<10^{-3}$
Electromagnetic Compatibility	**Very low EMI/RFI emission, compatible with the required sensitivity, one piece packageing with several ground points.**
Features Uniformity	**<1 %**
Integral Non Linearity for Vmon vs Vout relation	$<2\cdot10^{-3}$ **@ Vout > 500 V**

Table 1 Main specifications and expected accuracy for the AUGER-SD dc-dc converters.

2. THE TEST BENCH

The test facility is a multi-channel configuration including different instruments, designed to perform a standard automatic sequence of operations to characterize the dc-dc converter behaviour. The instrumentation desk is shown in figure 1.
The bench has been realized for:

1. Helping in the choice of the module during the HV tender [2];

2. Testing the required specs of pre-production and production modules;

3. Defining the tests to be performed during production;

4. Performing sample tests on dc-dc converters to check reliability of manufacturer's data sheets during the production phase.

The test bench diagram, allowing the parallel test of 8 modules, is presented in figure 2. A block diagram of a single channel circuit is also shown.

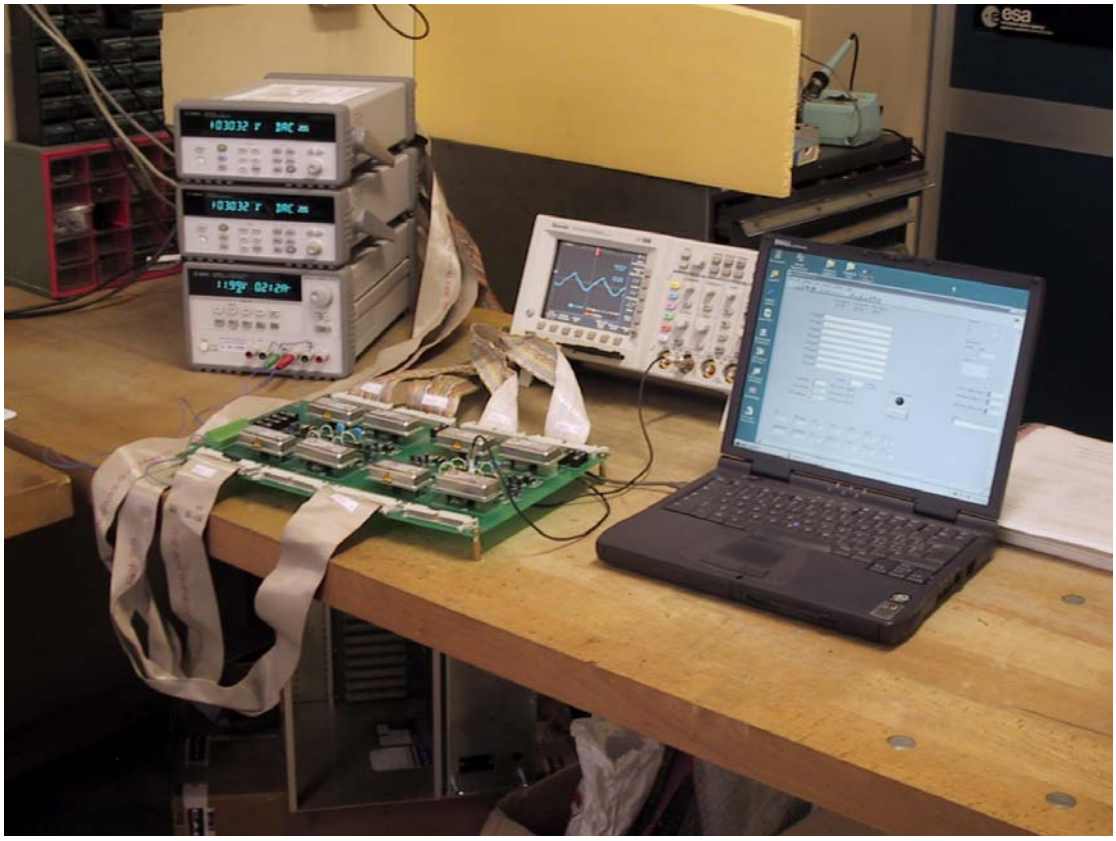

Figure 1: View of the instrumentation desk.

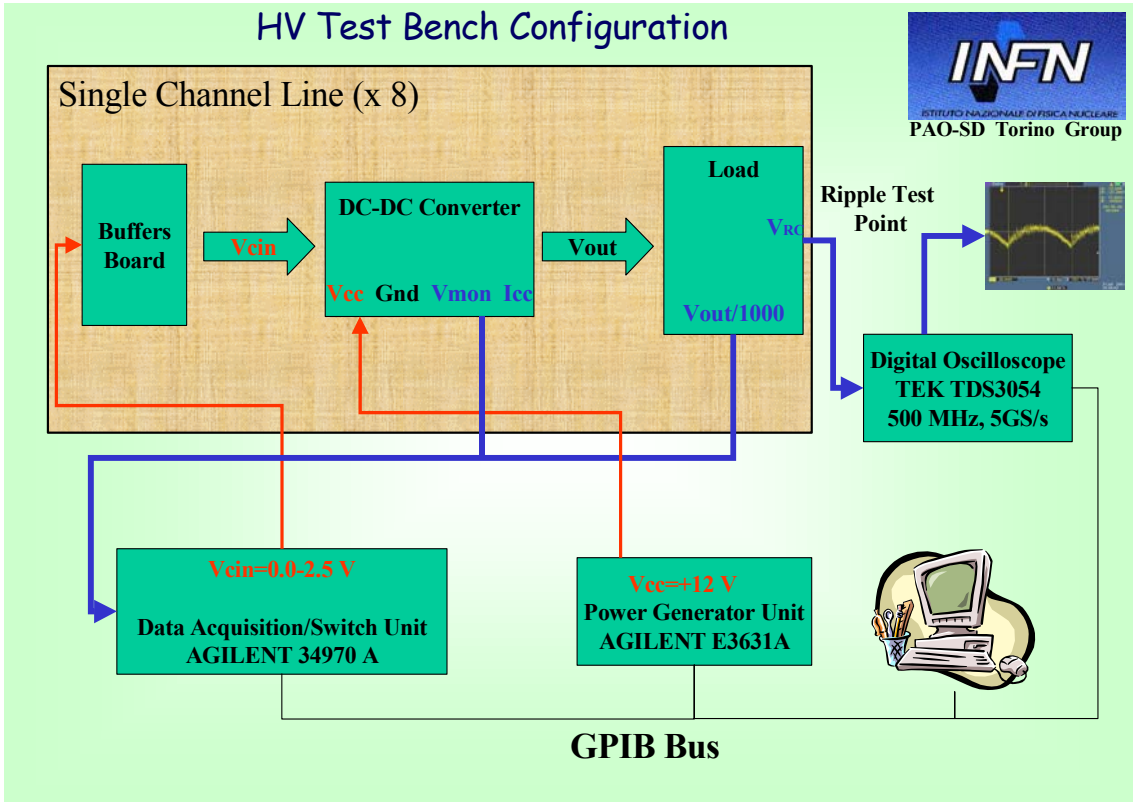

Figure 2: Diagram of the Test Bench..

The instruments and electronic components included in the test bench are:

- 1 portable computer (DELL Latitude), equipped with the LABIEW software package and a GPIB interface;
- 1 four channels Portable Digital Oscilloscope (TEK TDS3054 500 MHz,5 GS/s) for ripple measurements;
- 1 Power Generator Unit (AGILENT E3631 A) which provides low voltage supply (Vcc=12 V) to the DC-DC converters;
- 2 Data Acquisition & Switch Units (AGILENT 34970 A) used either as DAC to generate the command input Vcin to the HV modules or as multiplexed read-out system. The Power Generator and Data Acquisition devices are connected to the PC via the GBIP bus and remotely controlled;
- 1 main board which provides each modules with the load (20 MΩ) simulating the photomultiplier passive divider and with two test points for the output voltage and ripple measurement (see figure 3). Via the GPIB bus and through the switching multi-meter unit the values of the command (Vcin), the monitor (Vmon) and the output (Vout) voltages of each module as well as the absorbed power (Pabs) are recorded. The ripple is checked with the scope at Vout~2000 V. The pulse shape can be recorded.

The system is managed by a LABVIEW software which performs the parallel monitoring of 8 DC-DC converters (see figure 2).

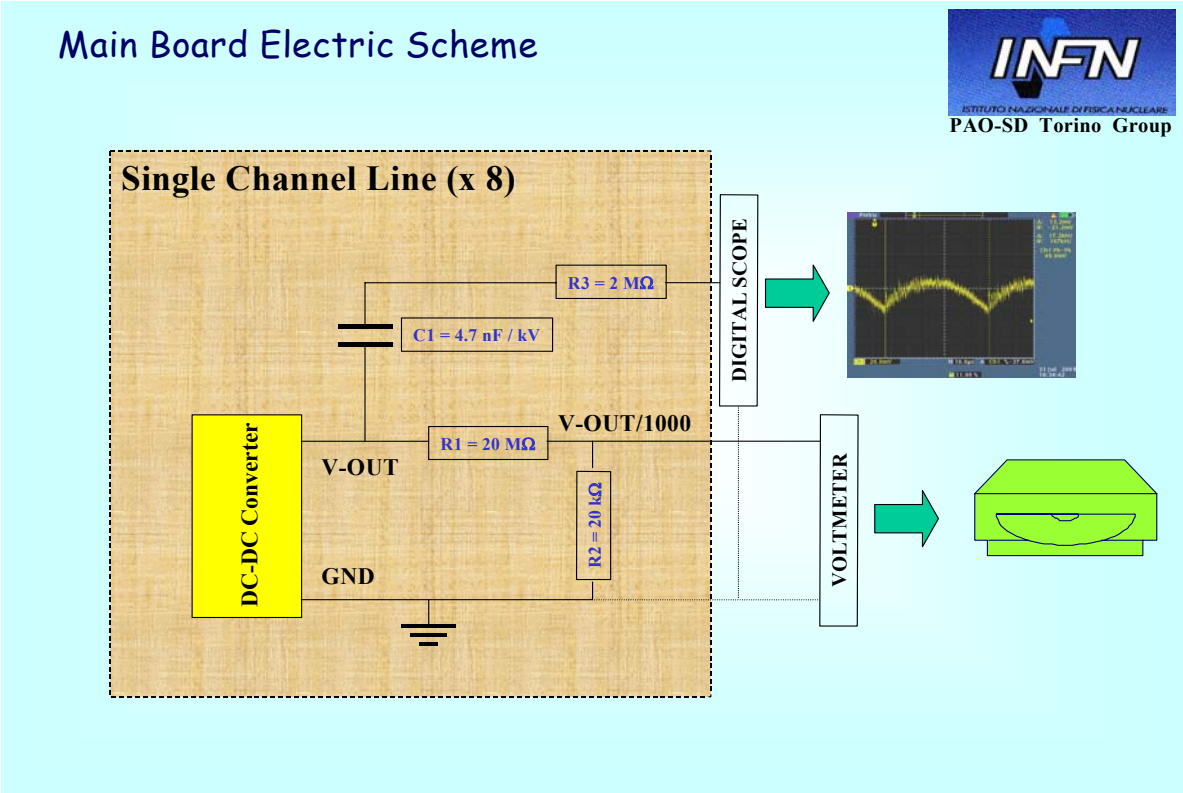

Figure 3: Electric scheme of a single channel on the main board. (See appendix 1 for details).

3. MULTI-METER & DAC RESOLUTION

At standard temperature operating condition (i.e. T=23 ±5 °C) the multi-meter accuracy is a combination of 2 independent components: ***Reading error and Range error*** [3].
The ***Reading error*** compensates for inaccuracies that result from the input signal level at fixed selected range of measurement. At the 10 V dc range, used during our measurement , the reading error is 15 ppm (0.0015 %) of the input signal.
The ***Range error*** compensates for inaccuracies resulting from the selected range itself: 4 ppm (0.0004 %) of the selected range (i.e. 40 μV at Vdc=10 V range value).
Thus the instrument accuracy is always better than 100 μV for all measured parameters.

The input command (Vcin) accuracy is mainly due to the DAC resolution. Using a self correcting procedure, which is software implemented, the precision reached on the Vcin command applied to the dc-dc module is better than 1 mV over the full operational range between 0.0 to 2.5 V. Such a precision is high enough to ensure the stability of the output voltage parameter with respect to the command. So far we can monitor the intrinsic fluctuations due to the module's behaviour.

4. TESTING PROCEDURES

The testing procedures have been fixed in order to measure the main DC-DC converter features shown in table 1 within the expected sensitivity. The basic test sequence includes 4 different steps: short circuit, stability, ramp up and ripple measurements. They are summarized in the flow chart in figure 4.

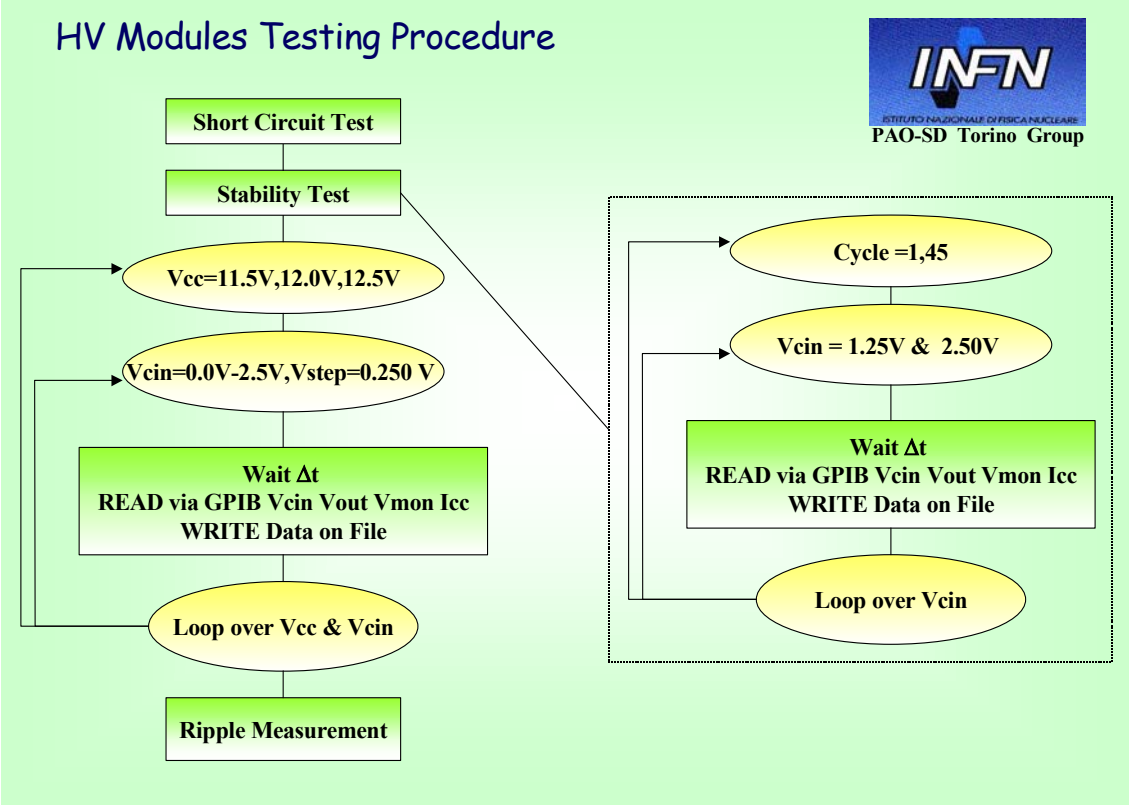

Figure 4: Flow chart of executable testing procedures of the HV modules.

1. A 1 minute short circuit is applied to test the native mortality for unproper use ;
2. The stability measurement is performed at constant Vcc=+12 V value on the 8 channels. A systematic repetition (45 cycles) of 2 values of the Vcin command (1.25 and 2.50 V alternatively applied) is performed. Each cycle takes about 30 minutes of continuous data acquisition, during which HV modules are expected to reach the stability point (warm up), typically 20 minutes after start time. Due to this reason the last 16 points (i.e. last 10 minutes of data) can be safely used to estimate the capability of the converter to reproduce the same output for a constant input command. The output response as a function of time for modules of 2 different companies is shown in figure 5. Finally mean value and dispersion of Vout, Vmon and Pabs parameters, as well as their maximum deviation, are calculated.
3. Response of each module in the full range of the Vcin command (i.e. the ramp up measurement) is studied as a function of the Vcc values. This study is achieved by mean of a loop over the Vcc e Vcin inputs as shown in the flow chart in figure 4. The Vcin command is provided by DAC, which is on-line optimized. Response of the module, i.e. the measurement of Vout, Vmon, and Pabs, is therefore obtained. The parameters read-out is performed 10 s after applying the command.
4. For each channel the output ripple at maximum voltage is checked with the scope. The peak to peak value is measured and the pulse shape is stored.

The full 4 steps cycle takes about 60 minutes for testing 8 modules.

In addition to the previous tests this equipment has been used to:

- check the response of a sample set of HV modules as a function of temperature from -10 °C up to +60 °C in a climatic chamber in order to measure the coefficient of the drift;
- verify the stability of modules after long time use (i.e. after the ageing process by module burn-in at +70 °C for 7 days).

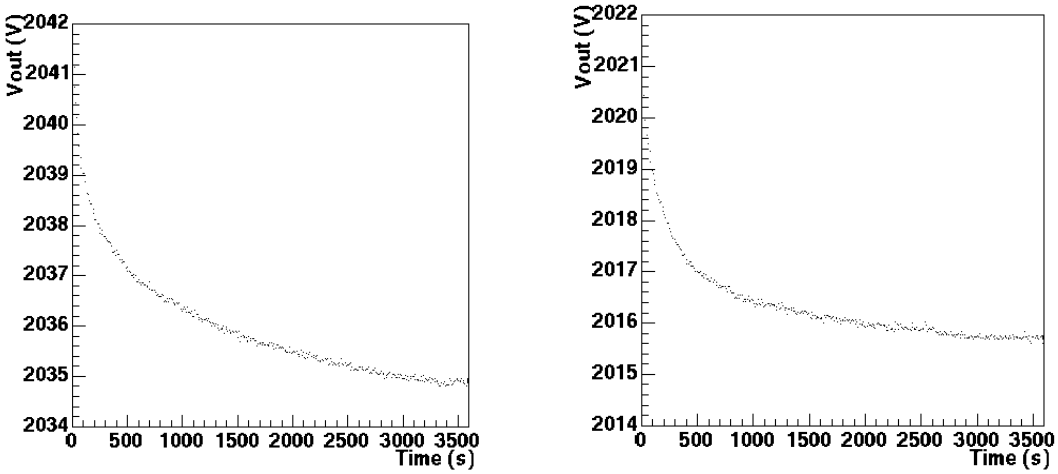

Figure 5 Vout response versus time for 2 different DC-DC converters at constant Vcc= 12V and Vcin=2.5 V values: (left side) SDS company, Paris - France [4] (right side) ETL company, London - United Kingdom [5].

5. TEST RESULTS ON THE SDS MODULES

A) Standard test at room temperature

This section reports on the results of the test of 152 DC-DC modules (SDS company, Paris – France [4]). The measured characteristics, which fix the mean properties of the set, are summarized in table 2.
They have been obtained through the analysis of all data measured by applying the standard procedure described in the previous sections. Histograms in figure 6 show the distributions of main parameters (measured at fixed Vcc=12 V) for the whole sample: the output voltage Vout (top left), the output monitor Vmon (top right), the absorbed power Pabs (bottom left). These are mean values for each module at the upper edge of the command range (Vcin=2.5 V) and they are calculated over the last 16 points of stability measurement. Finally the Vout uniformity (bottom right) is the maximum absolute deviation from the mean Vout value over the 16 points range considered.

Parameter Definition	*Mean Value*
Mean Output Voltage Vout @ Cin=2.5 V & Vcc=12 V (see note 1)	**2044 V**
Mean Monitor Output Vmon @ Cin=2.5 V & Vcc=12 V (see note 1)	**5.1 V**
Mean Absorbed Power Pabs @ Cin=2.5 V & Vcc=12 V (see note 1)	**544 mW**
Output Voltage Uniformity @ Cin=2.5 V & Vcc=12 V (see note 2)	**0.45 $^{0}/_{00}$**
Maximum ΔVout/Vout Fluctuation vs Vcc @ Vout > 500 V (see note 3)	**2.7 $^{0}/_{00}$**
Vout vs Vcin Integral Non Linearity (see note 4)	**2.36 $^{0}/_{00}$**
Vmon vs Vout Integral Non Linearity (see note 4)	**2.39 $^{0}/_{00}$**
Ripple (Peak to Peak)	**55 mV (0.03 $^{0}/_{00}$)**

Table 2 Measured characteristics of pre-production SDS HV power supplies.

Notes:
1. For each module mean values are calculated over the distribution of last 16 points (10 minutes data) of the stability measurement.
2. Maximum deviation from the Mean Output Voltage is estimated using last 16 points of the stability measurement.
3. Maximum deviation of Output Voltage Vout, over the full Vcin range, measured at Vcc=11.5 V or Vcc=12.5 V compared with value measured at Vcc=12 V. Ramp up measurement is considered.
4. Maximum deviation of the measured parameter from the one estimated by the linear fit. Ramp up measurement is considered.

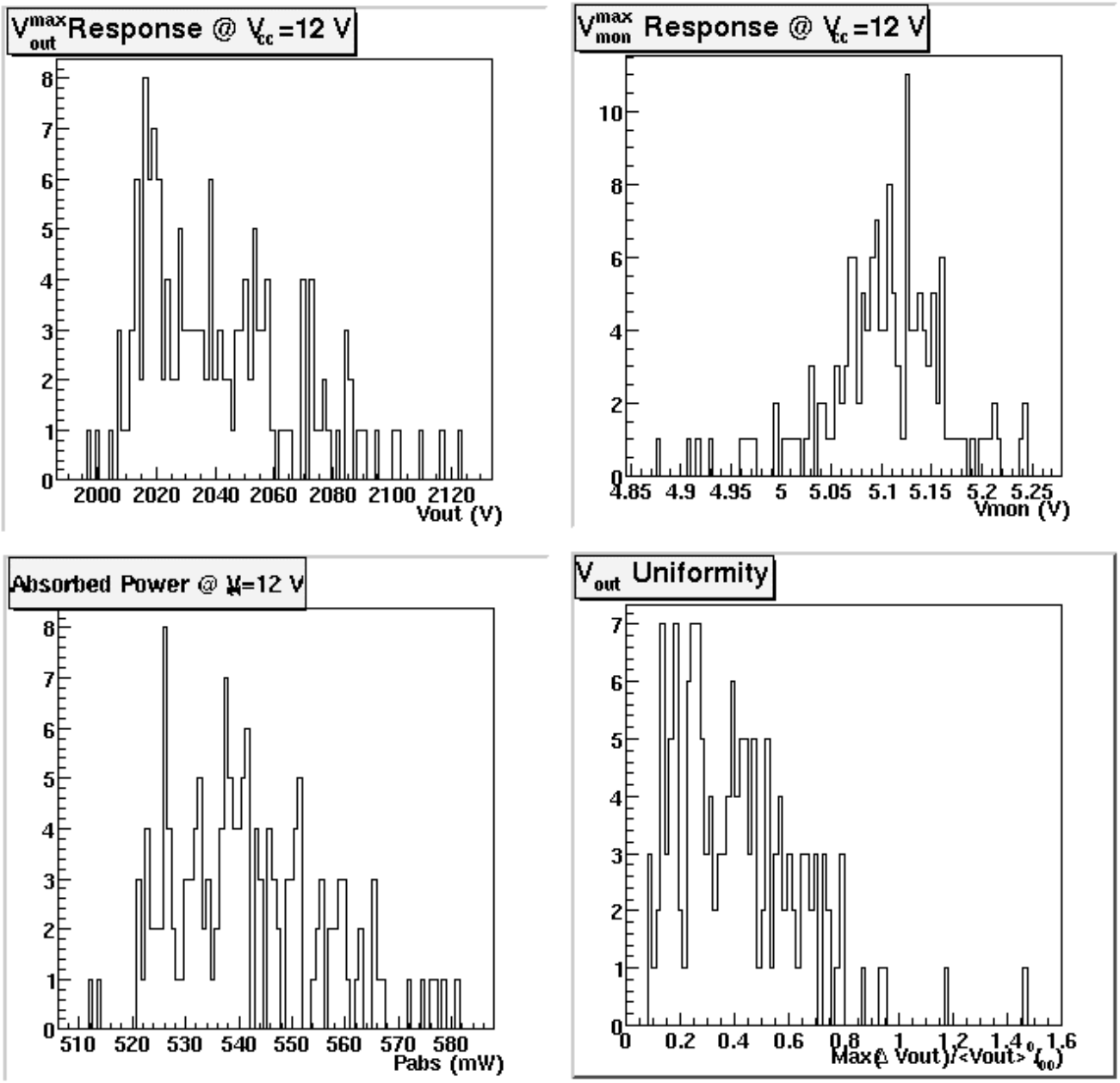

Fig.6 Response characteristics of 152 HV modules. For comments on measured values see text, table 2 and related notes.

B) Stability versus temperature

On a sample of 8 HV modules we studied the response characteristics over a wide range of temperature values. A temperature climatic chamber including a drying system has been used. The variations of the main parameters have therefore been checked at temperature values 0, 15, 30, 45 and 60 °C.
To measure changes on the output voltage with temperature, stability and ramp-up measurements have been repeated following standard procedures. A confident waiting time, between 20 and 40 minutes for each point, has been applied to reach the temperature stability inside the chamber. The value has been verified twice by a standard Hg termo-meter (accuracy 0.5 °C) and a termo-couple sensor, both inside the climatic chamber.
Figure 7 shows for 1 tested module the trend of maximum output voltage for Vcc=12 V and Vcin=2.5 V as a function of temperature values. A linear fit (e.g. Vout(V)=p0+p1*T(°C)) is used to obtain the value of temperature drift C:

$$C = \frac{\Delta V}{V \cdot \Delta T} = \frac{|p1| \cdot \Delta T}{V \cdot \Delta T} = \frac{|p1|}{V}$$

where V is the output voltage measured at 30 °C.

The obtained drift values (see table 3) are contained in the range $[0.9 - 1.4] \cdot 10^{-4} \frac{V}{V \cdot °C}$ with a mean value $1.2 \cdot 10^{-4} \frac{V}{V \cdot °C}$.

HV PS Serial Number	***Slope of the Fit (V/°C)***	***Drift Parameter (10^{-4} V/V°C)***
46013606	**0.26**	**1.3**
46013607	**0.24**	**1.2**
46013608	**0.27**	**1.3**
46013609	**0.18**	**0.9**
46013610	**0.22**	**1.1**
46013611	**0.24**	**1.2**
46013612	**0.27**	**1.3**
46013613	**0.28**	**1.4**

Table 3 Temperature Drift parameter for a sample of 8 DC-DC converters.

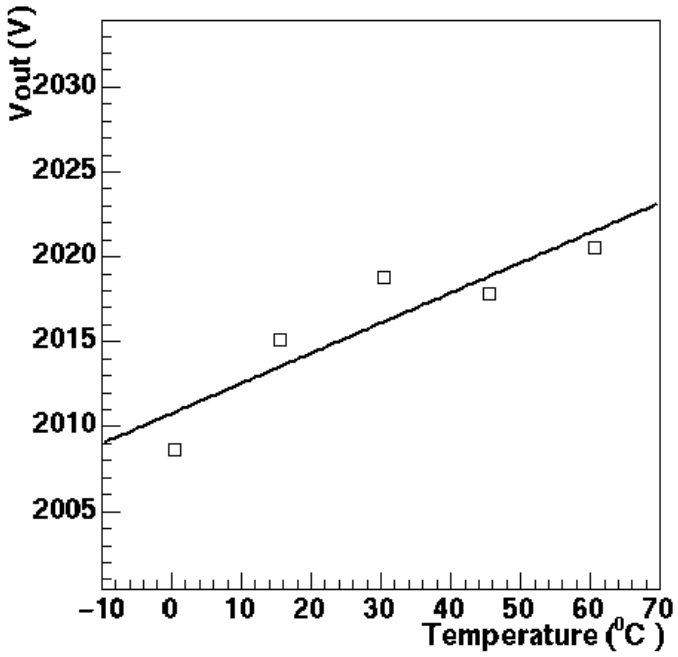

Fig. 7 Temperature Drift of 1 SDS Module in the range 0-60 °C. The Y-values are the output voltage at Vcin=2.5 V. The regression curve is also presented.

C) The long term stability

A sample of 71 modules randomly choosen and already tested, has been checked again after the ageing process in order to verify the long term stability. The ageing consists in the burn-in at high temperature (70 ^{0}C) for a week of the dc-dc converters supplied with Vcc= +12 V. All tests have thus been repeated on the standard test bench at the end of the process.
Main parameters of the subset before and after burn-in are obtained and shown in table 4.

Parameter Definition	*Before Burn-in*	*After Burn-in*
Mean Output Voltage Vout @ Cin=2.5 V & Vcc=12 V)	**2038 V**	**2054 V**
Mean Monitor Output Vmon @ Cin=2.5 V & Vcc=12 V	**5.095 V**	**5.106 V**
Mean Absorbed Power Pabs @ Cin=2.5 V & Vcc=12 V	**539 mW**	**551 mW**
Output Voltage Uniformity @ Cin=2.5 V & Vcc=12 V	**0.36 $^0/_{00}$**	**0.40 $^0/_{00}$**
Maximum ΔVout/Vout Fluctuation vs Vcc @ Vout > 500 V	**2.2 $^0/_{00}$**	**2.0 $^0/_{00}$**

Vout vs Vcin Integral Non Linearity	**2.3 $^{0}/_{00}$**	**2.4 $^{0}/_{00}$**
Vmon vs Vout Integral Non Linearity	**2.4 $^{0}/_{00}$**	**2.5 $^{0}/_{00}$**

Table 4 Comparison of main characteristics of a subset of dc-dc modules obtained before and after the burn-in process.

From values in table 4 no significant difference has been found: we can conclude that the converters of subset tested twice keep quite constant response after the ageing .

6. TEST RESULTS ON THE ETL MODULES

The first batch of 150 pieces has been fully checked. We schematically report here on main results of the standard test (table 5 and figure 8), temperature test (figure 10) and ageing effects (table 6) already discussed in the previous section for SDS modules.
In addition in figure 9 the distributions of parameters p0 and p1 obtained by the linear fit of the Vout vs Vcin (top side) and Vmon vs Vout (bottom side) relationships are shown. The constant value p0 (left side) and the slope p1 (right side), where Vout(V)=p0+p1*Vcin(V) or Vmon(V)=p0+p1*Vout(kV) are assumed, are given.
From the distributions of the slopes (i.e. p1 parameters) the uniformity of the whole set (i.e. the ratio RMS/MEAN VALUE) has been found to be better than 1 %.

Parameter Definition	***Mean Value***
Mean Output Voltage Vout @ Cin=2.5 V & Vcc=12 V (see note 1)	**2022 V**
Mean Monitor Output Vmon @ Cin=2.5 V & Vcc=12 V (see note 1)	**4.9 V**
Mean Absorbed Power Pabs @ Cin=2.5 V & Vcc=12 V (see note 1)	**314 mW**
Output Voltage Uniformity @ Cin=2.5 V & Vcc=12 V (see note 2)	**0.1 $^{0}/_{00}$**
Maximum ΔVout/Vout Fluctuation vs Vcc @ Vout > 500 V (see note 3)	**0.4 $^{0}/_{00}$**
Vout vs Vcin Integral Non Linearity (see note 4)	**1.22 $^{0}/_{00}$**
Vmon vs Vout Integral Non Linearity (see note 4)	**0.14 $^{0}/_{00}$**
Ripple (Peak to Peak)	**42 mV (0.02 $^{0}/_{00}$)**

Table 5 Measured characteristics of pre-production ETL dc-dc converters.

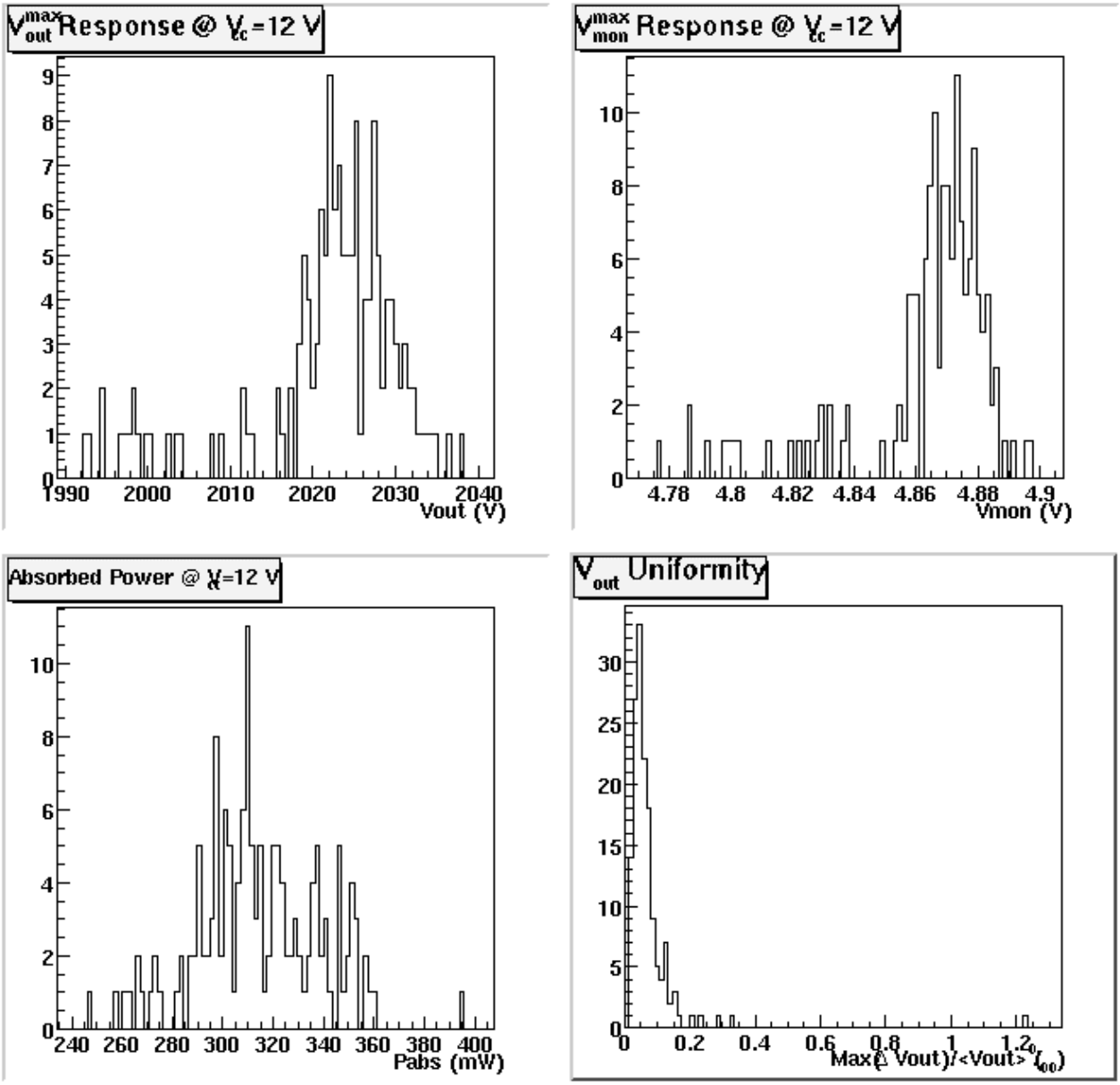

Fig. 8 Main properties of 150 dc-dc converters of the ETL Company. For comments on measured values see text and table 5.

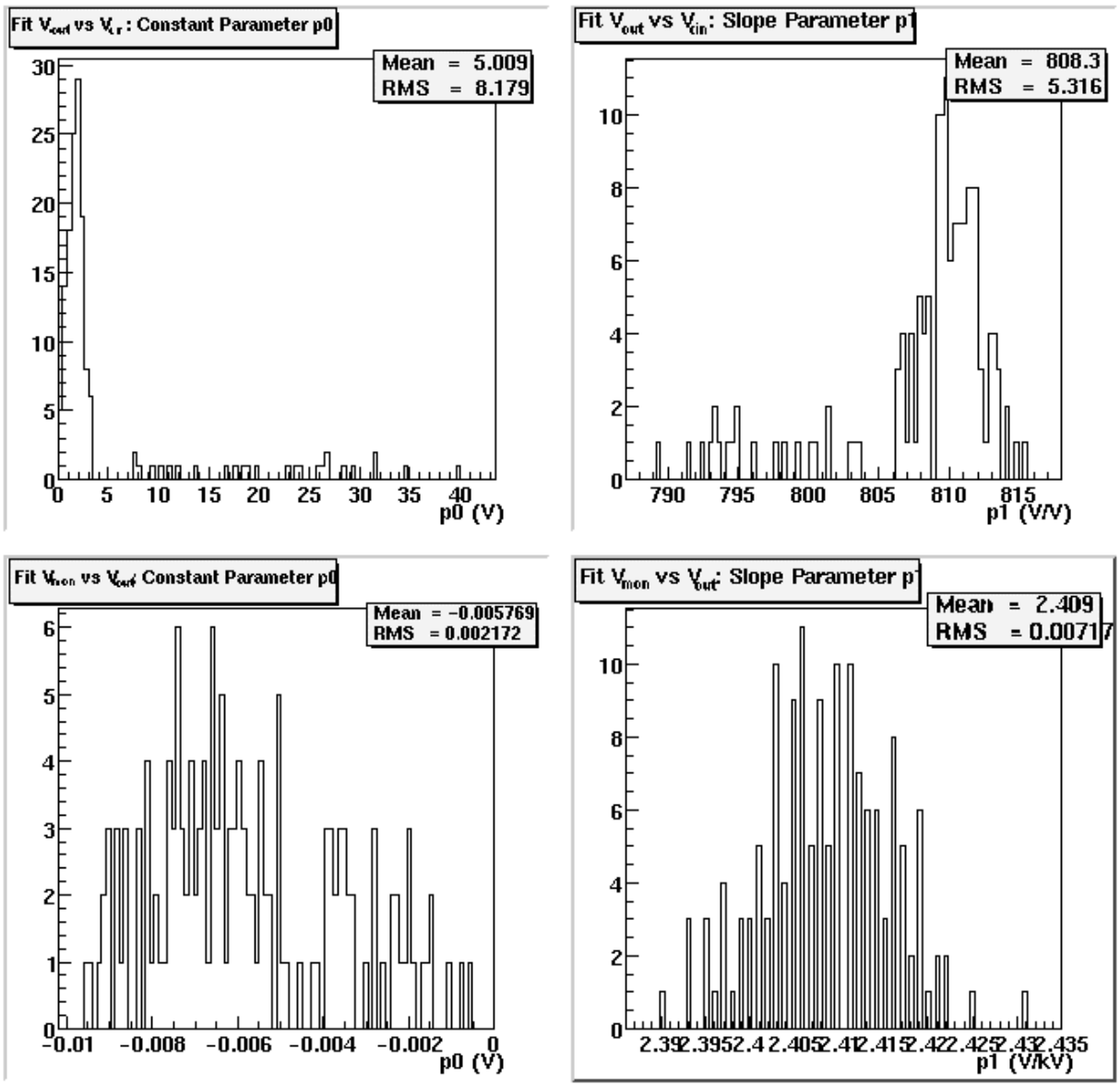

Fig. 9 Distribution of constant (p0) and slope (p1) parameters obtained by the linear fit of Vout vs Vcin (top) and Vmon vs Vout (bottom) relationships. From the distributions of the slopes (right side) the uniformity (i.e. the measured RMS/MEAN value) of the full set is better than the upper limit of 1 % which has been requested to the manufacturer.

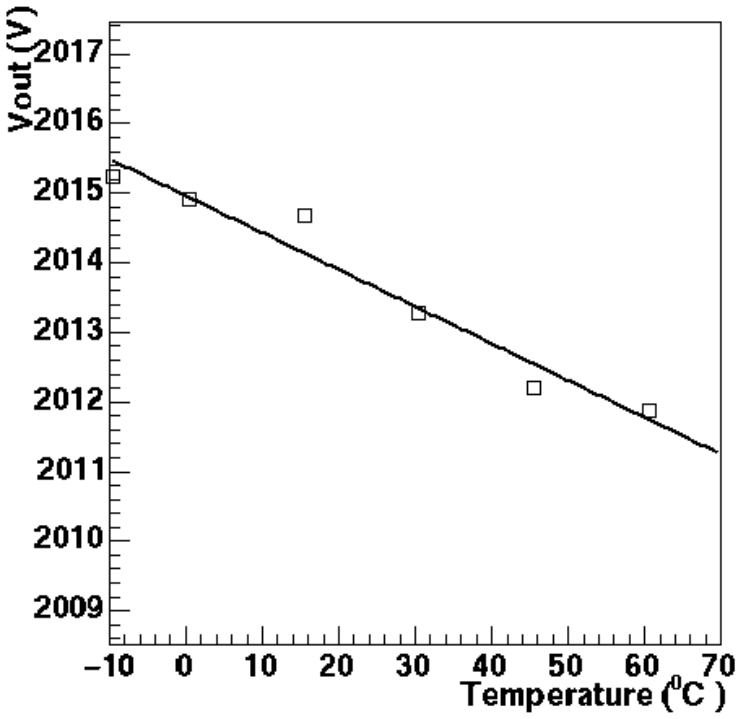

Fig.10 Temperature Drift of 1 ETL Module in the range –10 to 60 °C. The Y-values are the output voltage at Vcin=2.5 V. The regression curve is also presented.

The obtained drift values over 5 tested modules are contained in the range $[0.2-2.0]\cdot 10^{-4}\,\frac{V}{V\cdot °C}$ with a mean value.

Parameter Definition	*Before Burn-in*	*After Burn-in*
Mean Output Voltage Vout @ Cin=2.5 V & Vcc=12 V)	**2022 V**	**2020 V**
Mean Monitor Output Vmon @ Cin=2.5 V & Vcc=12 V	**4.88 V**	**4.87 V**
Mean Absorbed Power Pabs @ Cin=2.5 V & Vcc=12 V	**314 mW**	**325 mW**
Output Voltage Uniformity @ Cin=2.5 V & Vcc=12 V	**0.1 $^{0}/_{00}$**	**0.1 $^{0}/_{00}$**
Maximum ΔVout/Vout Fluctuation vs Vcc @ Vout > 500 V	**0.4 $^{0}/_{00}$**	**0.6 $^{0}/_{00}$**
Vout vs Vcin Integral Non Linearity	**1.2 $^{0}/_{00}$**	**0.5 $^{0}/_{00}$**
Vmon vs Vout Integral Non Linearity	**0.14 $^{0}/_{00}$**	**0.15 $^{0}/_{00}$**

Table 6 Comparison of main characteristics of all 150 dc-dc converters obtained before and after the burn-in process.

7. CONCLUSIONS

We have designed a test bench to check main properties of high voltage power supplies which are going to be mounted on the photomultiplier bases of the AUGER Surface Detector. Characteristics of the bench and testing procedures have been described.

Using this facility, the main specifications of pre-production (SDS & ETL) dc-dc converters have been fully tested in order to verify that they meet all requirements.

The test bench is going to be used for sample tests during production phase to monitor production quality.

8. REFERENCES

[1] Low power high dynamic range photomultiplier bases for the surface detectors of the Pierre Auger Observatory, Beaune 2002, GAP note 2002-038.

[2] Choice of the high voltage power supply for the surface detector photomultiplier bases (IPN Orsay) (see Technical Design Report).

[3] Agilent HP 34970A Data Acquisition / Switch Unit, Manual and User's Guide.

[4] SDS, Service et Developpement Scientifique[, 47 Rue de Clisson 75013 Paris, France.

[5] ETL, Electron Tubes Limited, Bury Street Ruislip Middx HA4 7TA, United Kingdom.

APPENDIX 1

HV TEST BENCH: MAIN BOARD SCHEMATICS