



Datasheet

Low-power, high-sensitivity infrared sensor for presence and motion detection



Product status

Custom data

Product summary

STHS34PF80TR

-40 to +85

LGA-10L

Tape and reel

Order code

Temperature

range [°C]

Package

Packing

Features

Key features

- · High-sensitivity, infrared presence and motion sensor
- Reach up to 4 meters without lens for objects measuring 70 x 25 cm²
- Integrated silicon IR filter
- · SMD friendly
- Capable of detecting stationary objects
- Capable of distinguishing between stationary and moving objects
- 80° field of view
- Factory calibrated
- Low power
- Embedded smart algorithm for presence / motion detection

Electrical specifications

- Supply voltage: 1.7 V to 3.6 V
- Supply current: 10 μA
- 2-wire I²C / 3-wire SPI serial interface
- Programmable ODRs from 0.25 Hz to 30 Hz
- One-shot mode

Sensing specifications

- IR sensitivity: 2000 LSB/°C
- RMS noise: 25 LSB_{rms}
- Operating wavelength: 5 μm to 20 μm
- Local temperature sensor accuracy: ±0.3 °C

Product resources

TN0018 (Design and soldering)

Product label



Package specifications

- LGA 10-lead, 3.2 x 4.2 x 1.455 (max) mm
- ECOPACK and RoHS compliant

Applications

- · Alarm / security systems
- Home automation
- Smart lighting
- lol
- · Smart lockers
- Smart wall pads

Description

The STHS34PF80 is an uncooled, factory-calibrated, IR sensor with operating wavelength between 5 μm and 20 μm



The STHS34PF80 sensor has been designed to measure the amount of IR radiation emitted from an object within its field of view. The information is digitally processed by the ASIC which can be programmed to monitor motion, presence, or an overtemperature condition.

Thanks to its exceptional sensitivity, the STHS34PF80 can detect human presence at a distance up to 4 meters an object measuring $70 \times 25 \text{ cm}^2$ without the need of an optical lens.

The STHS34PF80 is housed in a small 3.2 x 4.2 x 1.455 (max) mm 10-lead LGA package.



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1 Overview

The STHS34PF80 is an infrared sensor that can be used to detect the presence of stationary and moving objects as well as overtemperature conditions. It measures the object's IR radiation with unique TMOS technology to detect its presence or motion when the object is inside the field of view.

An optical band-pass filter is deposited over the sensor limiting its operating range within the wavelengths of 5 μ m and 20 μ m, making it insensitive to visible light and other bands.

The sensor is based on a matrix of floating vacuum thermal transistors MOS (TMOS) connected together and acting as a single sensing element. A state-of-the-art thermal isolation is achieved thanks to ST's unique MEMS manufacturing technologies, allowing the sensor to translate the smallest temperature changes into electrical signals that, in turn, are fed to the ASIC.

The sensor is split into two parts, one exposed to IR radiation and the other one shielded. Differential reading between the two parts is implemented to remove the effect of sensor self-heating.

The STHS34PF80 embeds a high-accuracy temperature sensor to measure the ambient temperature and to enable measuring the precise IR radiation of an object.

The ASIC also implements dedicated smart processing to detect / discriminate between stationary and moving objects and which can assert dedicated interrupts.

Different ODRs from 0.25 Hz to 30 Hz and a one-shot mode are available.

The STHS34PF80 is equipped with an I²C / 3-wire SPI interface and is housed in an OLGA 3.2 x 4.2 x 1.455 mm 10L package compatible with SMD mounting.

The field of view guaranteed by the package is 80°.

TMOS Analog cs cs I²C ADC1 Front SCL/SPC SPI End **TMOS** Digital **Digital Interface** SDA/SDI/O Sensor Logic (Registers / LPF etc..) Temperature INT ADC₂ Interrupt . Sensor Voltage & Power Calibration Clock generator **Current bias** registers management

Figure 1. Block diagram

Pin description

2 Pin description

Figure 2. Pin configuration (package bottom view)

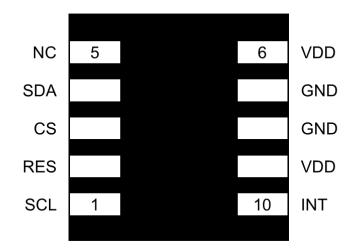


Table 1. Pin description

Pin number	Name	Function
1	SCL / SPC	I ² C / SPI serial interface clock
2	RES	Reserved (connect to GND)
3	CS	I ² C / SPI interface selection (1: I ² C enabled; 0: SPI enabled)
4	SDA / SDI/O	I ² C / SPI serial data line
5	NC	Leave floating (do not connect)
6	VDD	Power supply
7	GND	0 V supply
8	GND	0 V supply
9	VDD	Power supply
10	INT	Interrupt signal

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Sensor and electrical specifications

3 Sensor and electrical specifications

Conditions at V_{DD} = 1.8 V, T = 25 °C.

Table 2. Sensor specifications

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit	
T _{bit}	Temperature output data (object and ambient)		_	16	_	Bit	
T _{amb_s}	Ambient temperature sensitivity	70	_	100	_	LSB/°C	
T _{obj_s}	Object temperature sensitivity ⁽²⁾	15 °C to 35 °C		2000		LSB/°C	
т.	Ambient temperature copeer acquirecy	-10 °C to 60 °C		±0.3		°C	
T _{amb_a}	Ambient temperature sensor accuracy	-40 °C to 85 °C		±0.6			
		ODR [3:0] = 0001		0.25			
		ODR [3:0] = 0010		0.5			
		ODR [3:0] = 0011	: 0011 1.0				
ODR	Object and ambient temperature output data rate	ODR [3:0] = 0100		2.0		Hz	
ODK	Object and ambient temperature output data rate	ODR [3:0] = 0101		4.0			
		ODR [3:0] = 0110		8.0			
		ODR [3:0] = 0111		15.0			
		ODR [3:0] = 1xxx		30.0			
RMS noise	AVG_TMOS = 32 ⁽³⁾			25		LSB _{rms}	
FFOV	Full field of view ⁽⁴⁾			80		Degree	

^{1.} Typical specifications are not guaranteed.

Table 3. Electrical specifications

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{DD}	Supply voltage		1.7	_	3.6	V
las	Cupply ourrant	128 average @ 1 Hz ODR		10		
I _{DD}	Supply current	32 average @ 1 Hz ODR		5		μΑ
Idd _{PDN}	Power-down supply current			1		μA
Тор	Operating temperature range		-40	_	85	°C

1. Typical specifications are not guaranteed.

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The object temperature measurement is specified for a full field-of-view coverage by a black body with more than 99% emissivity. The accuracy specifications apply under settled isothermal conditions only.

^{3.} Tobj RMS noise can be different based on the AVG_TMOS value. Further detailed information can be found in Table 13.

^{4.} Angle to have 50% IR intensity.

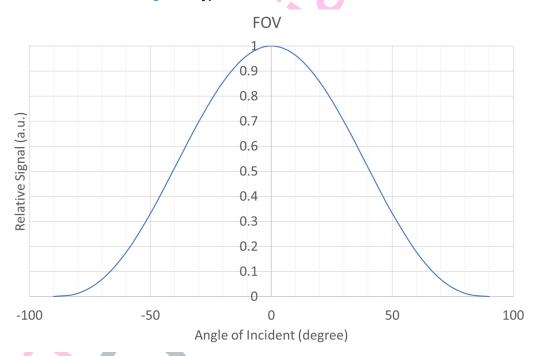
4 Optical specifications

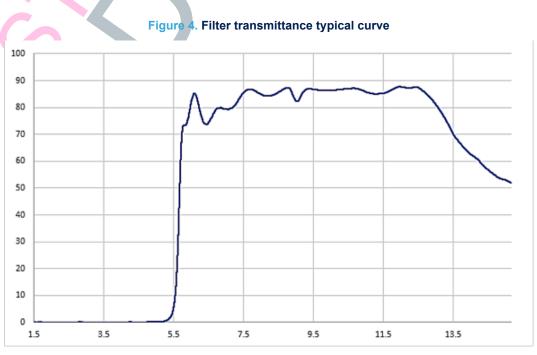
Table 4. Optical specification

Symbol	Parameter	Test condition	Min.	Typ. ⁽¹⁾	Max.	Unit
FFOV	Full field of view	At 50% intensity		80		Degree

^{1.} Typical specifications are not guaranteed.

Figure 3. Typical field of view measurements





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5 Digital interfaces

The registers embedded inside the STHS34PF80 can be accessed through both an I²C and a 3-wire SPI slave interface

The serial interfaces are mapped to the same pins. The selection between the two interfaces is made through the CS pin, refer to Table 1. Pin description.

5.1 I²C interface

Following the correct protocols, the device behaves as an I²C slave. The registers embedded inside the ASIC device may be accessed through the I²C serial interfaces.

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to VDD through an external pull-up resistor. When the bus is free, both the lines are high.

All transactions begin with a start (ST) and are terminated by a stop (SP) (see Figure 5). A high to low transition on the SDA line while SCL is high defines a start condition (ST). A low to high transition on the SDA line while SCL is high defines a stop condition.

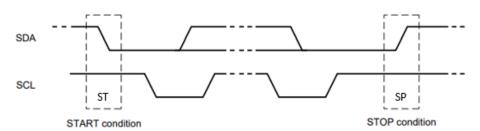


Figure 5. Start and stop conditions

After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the ST condition contains the address of the slave in the first 7 bits (SAD) and the eighth bit is W='0' which indicates that the master is transmitting data to the slave (SAD+W). When a slave address (SAD) is sent, each device in the system compares the first seven bits after a start condition (ST) with its slave address. If they match, the device considers itself addressed by the master.

The slave address of the STHS34PF80 is SAD=1011010.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse (SAK). A receiver which has been addressed must generate an acknowledge after each byte of data has been received.

After the SAK from slave (STHS34PF80) the master sends an 8-bit subaddress (SUB): the 7 LSB represent the actual register address while the MSB has no meaning. For this I²C the auto increment is always active. Since auto increment is enabled by default, the SUB (register address) is automatically incremented to allow multiple data read/write at increasing addresses. When the slave receives the subaddress it responds with an ACK.

After this SAK from the slave, the master can do a write (single or multiple) or a read (single or multiple).

When the master wants to write, it sends a DATA (8-bit) and the slave responds with SAK. At this point if the master wants to close the communication, it sends a stop condition (SP) otherwise, it sends a new DATA.

When the master wants to read, it sends a repeated start condition (SR) and resends the slave address (SAD) with a read bit (R='1') (SAD+R). The slave responds with a SAK and sends the DATA (8-bit) to the master to read. The master responds with a MAK (master acknowledge) if it wants to read from the next SUB address, otherwise it responds with a NMAK (no master acknowledge) and closes the communication, sending a stop condition (SP).

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I²C high-speed mode

5.1.1 I²C read and write sequences

The previous sequences are used to perform actual write and read sequences described in the following tables.

Table 5. Transfer when the master is writing one byte to slave

Master	ST	SAD+W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 6. Transfer when master is writing multiple bytes to slave

Master	ST	SAD+W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 7. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Master	ST	SAD+W		SUB			SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SA	K			SAK	DATA		DATA		DATA		

5.2 I²C high-speed mode

High-speed mode devices can transfer information at bit rates of up to 3.4 Mbit/s, yet they remain fully downward compatible with fast- or standard-mode (F/S-mode) devices for bidirectional communication in a mixed-speed bus system. With the exception that arbitration and clock synchronization are not performed during the high-speed mode transfer, the same serial bus protocol and data format are maintained as with the F/S-mode system.

High-speed mode can only commence after the following conditions (all of which are in F/S-mode):

- 1. Start condition (S)
- 2. 8-bit master code (00001XXX)
- not-acknowledge bit (A)

This master code has two main functions: it allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winning master. It also indicates the beginning of a high-speed mode transfer.

High-speed mode master codes are reserved 8-bit codes, which are not used for slave addressing or other purposes. The master code indicates to other devices that a high-speed mode transfer is to begin and the connected devices must meet the high-speed mode specification. As no device is allowed to acknowledge the master code, the master code is followed by a not-acknowledge (A). After the not-acknowledge bit (A), and the SCLH line has been pulled up to a high level, the active master switches to high-speed mode and enables the current-source pull-up circuit for the SCLH signal. As other devices can delay the serial transfer before t_H by stretching the low period of the SCLH signal, the active master enables its current-source pull-up circuit when all devices have released the SCLH line and the SCLH signal has reached a high level, thus speeding up the last part of the rise time of the SCLH signal. The active master then sends a repeated start condition (SR) followed by a 7-bit slave address (or 10-bit slave address, see previous section) with a R/W bit address, and receives an acknowledge bit (A) from the selected slave.

After a repeated start condition and after each acknowledge bit (A) or not-acknowledge bit (A), the active master disables its current-source pull-up circuit. This enables other devices to delay the serial transfer by stretching the low period of the SCLH signal. The active master re-enables its current source pull-up circuit again when all devices have released and the SCLH signal reaches a high level and so speeds up the last part of the SCLH signal's rise time.

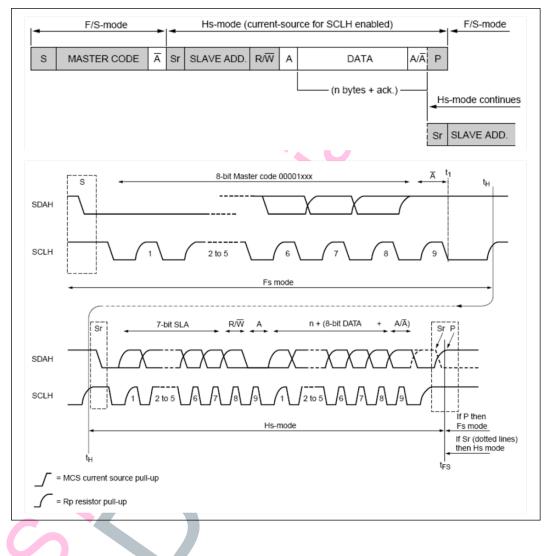
Data transfer continues in high-speed mode after the next repeated start (SR), and only switches back to F/S mode after a stop condition (P). To reduce the overhead of the master code, it is possible that a master links a number of high-speed mode transfers, separated by repeated start conditions (SR).

Each high-speed mode the device can switch from fast mode to high-speed mode and back and is controlled by the serial transfer on the I²C bus.

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I²C high-speed mode

Figure 6. Data transfer in high-speed mode



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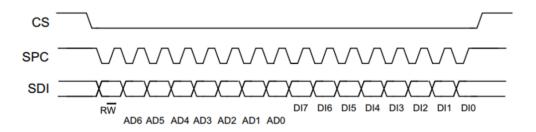
SPI interface

5.3 SPI interface

The ASIC SPI is a bus slave. The SPI allows writing and read the registers of the device. The serial interface interacts with the application using 3 wires: CS, SPC, SDI/O.

5.3.1 SPI write

Figure 7. SPI write protocol



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

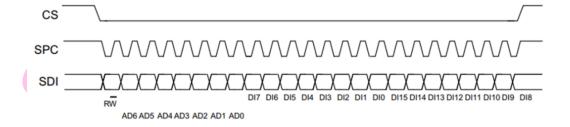
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-...: data DI(...-8). Additional data in multiple byte writes.

Figure 8. Multiple byte SPI write protocol (2-byte example)

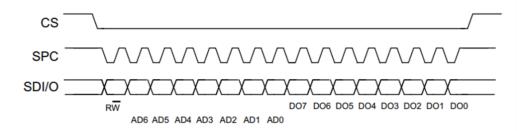


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SPI interface

5.3.2 SPI read

Figure 9. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clocks pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSB first).

The multiple write command is also available in 3-wire mode.



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6 Smart digital algorithms

The STHS34PF80 embeds smart digital algorithms to support the following three different detection modes:

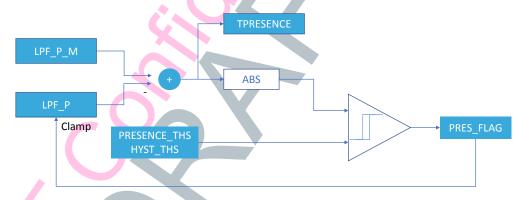
- Presence detection
- Motion detection
- Ambient temperature shock detection

6.1 Presence detection

Presence detection is performed by observing the difference between the two output signals of each low-pass filter (LPF_P_M & LPF_P) from the TMOS raw data of TOBJECT.

Then, the difference of the two signals is compared with the two thresholds of PRESENCE_THS and HYST_PRES which can be configured for the target application. Finally, the presence detection flag signal (PRES_FLAG) is set when the difference of the two filtered signals exceeds the threshold value as described in the figure below. When the PRES_FLAG is asserted, the LPF_P output remains at its last value. The LPF_P starts processing again the input data, providing filtered output when the PRES_FLAG is de-asserted

Figure 10. Presence algorithm block diagram

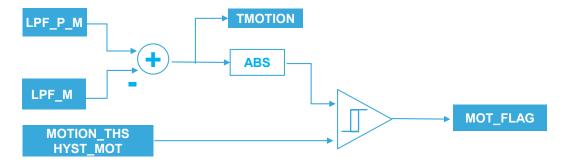


6.2 Motion detection

Motion detection is performed by observing the difference between the two output signals of each low-pass filter (LPF_P_M & LPF_M) from the TMOS raw data of TOBJECT.

Then, the difference of the two signals is compared with the two thresholds of MOTION_THS and HYST_MOT which can be configured for the target application. Finally, the motion detection flag signal (MOT_FLAG) is set when the difference of the two filtered signals exceeds the threshold value as described in the figure below.

Figure 11. Motion detection algorithm block diagram



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6.3 Ambient temperature shock detection

The ambient temperature shock detection is supported with the output signal of LPF_A_T and the signal of TAMBIENT. The difference of the two signals is compared with the hysteresis of TAMB_SHOCK_THS and HYST_TAMBS. The detection of the ambient shock flag (TAMB_SHOCK_FLAG) is set when the difference of the two signals (LPF_A_T & TAMBIENT) exceeds the threshold values to indicate a sudden change of ambient temperature.

TAMB_SHOCK

TAMB_SHOCK_THS
HYST_TAMBS

TAMB_SHOCK_FLAG

Figure 12. Ambient temperature shock detection algorithm block diagram

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7 Application schematics

The device power supply must be provided through the VDD line, a power supply decoupling capacitor (100 nF) must be placed as near as possible to the supply pins of device (VDD). Depending on the application, an additional capacitor of 1 μ F could be placed on the VDD line to avoid power noise on VDD.

The functionality of the device and the measured data outputs are selectable and accessible through the I²C and SPI digital interface as shown in the following figures.

Figure 13. Application schematic with I²C connection

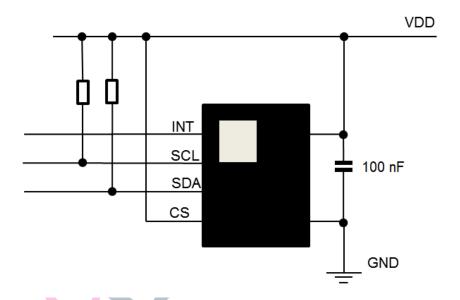
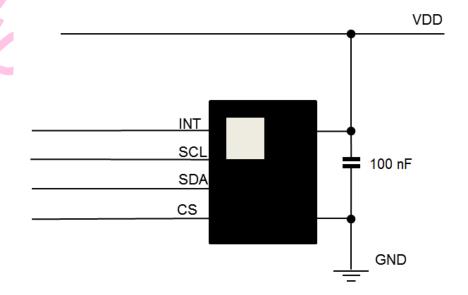


Figure 14. Application schematic with SPI connection



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Table 8. Internal pin status

Pin number	Name	Default pin status
1	SCL / SPC	Default: input without pull-up
2	RES	
3	CS	Default: input with pull-up
4	SDA / SDI/O	Default: input without pull-up
5	NC	
6	VDD	* . * ()*
7	GND	4
8	GND	
9	VDD	
10	INT	Default: input without pull-up



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Soldering guidelines

8 Soldering guidelines

The soldering profile depends on the number, size and placement of components on the application board. For this reason, it is not possible to define a unique soldering profile for the sensor only. The customer should use a time and temperature reflow profile based on PCB design and manufacturing expertise. In any case, the soldering profile should not exceed profiles as specified in Jedec J-STD-020.

LGA packages show metal traces on the side of the package so solder material must be avoided on the side of package during reflow.

The product package is not sealed as there is a 0.1 mm hole on the bottom of the package as illustrated in Figure 16. OLGA-10L (3.2 x 4.2 x 1.455 mm) package outline and mechanical data. A dry reflow process such as convection reflow is recommended. Vapor phase reflow is not suitable for this type of optical component.

'No-wash' assembly process has to be used. "Self-cleaning" / "no flux" solder paste are to be used.

The product top surface can be eventually protected by suitable tape during reflow and other manufacturing steps to avoid contamination or scratches on the optical filter section of the component.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.



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Register mapping

9 Register mapping

Table 9. Register map

Name	Туре	Register address	Default	Function and comment
Reserved		00-0Bh		Reserved
LPF1	RW	0Ch	04h	
LPF2	RW	0Dh	22h	
Reserved		0Eh	701	Reserved
WHO_AM_I	R	0Fh	D3h	Who am I
AVG_TRIM	RW	10h	03h	
Reserved		11-1Fh		Reserved
CTRL1	RW	20h	00h	
CTRL2	RW	21h	00h	
CTRL3	RW	22h	00h	Interrupt control
STATUS	R	23h		
Reserved		24h		Reserved
FUNC_STATUS	R	25h		
TOBJECT_L	R	26h		
TOBJECT_H	R	27h		
TAMBIENT_L	R	28h		
TAMBIENT_H	R	29h		
TPRESENCE_L	R	3Ah		
TPRESENCE_H	R	3Bh		
TMOTION_L	R	3Ch		
TMOTION_H	R	3Dh		
TAMB_SHOCK_L	R	3Eh		
TAMB_SHOCK_H	R	3Fh		

9.1 Embedded functions page register mapping

Table 10. Embedded functions page register map

Name	Туре	Register address	Default	Function and comment
PRESENCE_THS	RW	20h	C8h	
MOTION_THS	RW	22h	C8h	
TAMB_SHOCK_THS	RW	24h	0Ah	
HYST_MOTION	RW	26h	32h	
HYST_PRESENCE	RW	27h	32h	
ALGO_CONFIG	RW	28h	00h	
HYST_TAMB_SHOCK	RW	29h	02h	

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Registers description

10 Registers description

10.1 LPF1 (0Ch)

RW – default = 04h

7	6	5	4	3	2	1	0
-	-	LPF_P_M2	LPF_P_M1	LPF_P_M0	LPF_M2	LPF_M1	LPF_M0

LPF_P_M[2:0]	Low-pass filter configuration for motion and presence detection, see Table 11.
LPF_M[2:0]	Low-pass filter configuration for motion detection, see Table 11.

Table 11. Low-pass filter configuration

LPF_P_M[2:0] / LPF_M[2:0] / LPF_P[2:0] / LPF_A_T[2:0]	Low-pass filter configuration
000	ODR/9
001	ODR/20
010	ODR/50
011	ODR/100
100	ODR/200
101	ODR/400
111	ODR/800

10.2 LPF2 (0Dh)

RW – default = 22h

7	6	5	4	3	2	1	0	
-	-	LPF_P2	LPF_P1	LPF_P0	LPF_A_T2	LPF_A_T1	LPF_A_T0	

LPF_P[2:0]	Low-pass filter configuration for presence detection, see Table 11.
LPF_A_T[2:0]	Low-pass filter configuration for ambient temperature, see Table 11.

10.3 WHO_AM_I (0Fh)

Read only – default = D3h

7	6	5	4	3	2	1	0	
1	1	0	1	0	0	1	1	

WHO_AM_I	Device identification – Who am I
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AVG_TRIM (10h)

10.4 AVG_TRIM (10h)

RW - default = 03h

7	6	5	4	3	2	1	0
-	-	AVG_T1	AVG_T0	-	AVG_TMOS2	AVG_TMOS1	AVG_TMOS0

AVG_T[1:0]	Select the number of averages for ambient temperature, see Table 12.
AVG_TMOS[2:0]	Select the number of averages for object temperature, see Table 13.

Table 12. Averaging selection for ambient temperature

AVG_T[1:0]	Number of averages for ambient temperature
00	8 (Default)
01	4
10	2
11	1

Table 13. Averaging selection for object temperature and noise

AVG_TMOS [2:0]	Number of average for object temperature	RMS Noise (LSB _{rms})
000	2	90
001	8	50
010	32	25
011	128 (Default)	20
100	256	15
101	512	12
110	1024	11
111	2048	10

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STHS34PF80 CTRL1 (20h)

10.5 CTRL1 (20h)

RW - default = 00h

7	6	5	4	3	2	1	0
-	-	-	BDU	ODR3	ODR2	ODR1	ODR0

BDU	Block data update for output registers TOBJECT (26h and 27h) and TAMBIENT (28h and 29h).
ODR[3:0]	Output data rate, refer to Table 14 for ODR configuration

Table 14. ODR configuration

ODR [3:0]	ODR frequency [Hz]	Time [ms]
0000	Standby mode	-
0001	0.25	4000
0010	0.5	2000
0011	1	1000
0100	2	500
0101	4	250
0110	8	126
0111	15	66.67
1xxx	30	33.33

Device power consumption depends on the AVG_TMOS configuration and continuous mode at different ODRs as described in the following table.

Table 15. Current consumption at different ODRs and AVG_TMOS setting

AVG TMOS [2:0]	One-shot mode	Continuous mode – current consumption (μA) vs ODR								
AVG_TWOS [2.0]	Current consumption (μA) @ 1Hz	0.25 Hz	0.5 Hz	1 Hz	2 Hz	4 Hz	8 Hz	15 Hz	30 Hz	
000 (2)	3.23	3.2	3.52	4.39	6.58	10.54	18.32	33	64.1	
001 (8)	3.74	3.27	3.82	4.9	7.23	11.4	20.62	38.3	74.94	
010 (32)	5.10	3.6	4.48	6.26	9.58	17.05	30.75	59	115.65	
011 (128)	9.95	4.7	6.83	11.1	19.6	36.75	71.2			
100 (256)	16.89	6.55	10.55	18.02	33.1	65.5				
101 (512)	31.16	10.05	17.45	32.25	57.59					
110 (1024)	56.34	16.97	31.3	57.36						
111 (2048)		30.86	58.97							

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CTRL2 (21h)

CTRL2 (21h) 10.6

RW - default = 00h

7	6	5	4	3	2	1	0
воот	-	-	FUNC_ CFG_ACCESS	-	-	-	ONE_SHOT

воот	Reboot OTP memory content. Self-clearing upon completion. Default value : 0 (0: normal mode; 1: reboot memory content)
FUNC_CFG_ACCESS	Enable access to the registers ⁽¹⁾ for embedded functions. Default value: 0 (0: disable access to the embedded function page; 1: enable access to the embedded function page)
ONE_SHOT	Enable ONE_SHOT. Default value: 0 (0 : idle mode; 1 : new data set is acquired)

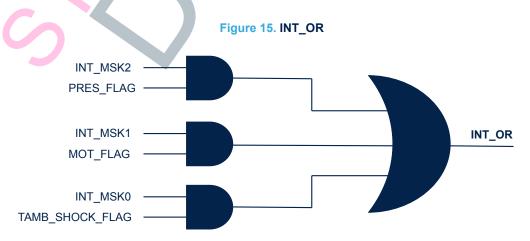
^{1.} It is not possible to write or read registers in main page if this bit is set to 1. In order to go back to the main page, this bit should be written to

10.7 CTRL3 (22h)

RW - default = 00h

7	6	5	4	3	2	1	0
INT_H_L	PP_OD	INT_MSK2	INT_MSK1	INT_MSK0	-	IEN1	IEN0

INT_H_L	Interrupt active-high & active-low. Default value: 0
	(0: active high; 1: active low)
PP OD	Push-pull / open-drain selection on the INT pin. Default value: 0
FF_OD	(0: push-pull; 1: open drain)
INT_MSK[2:0]	Interrupt masks for flag of FUNC_STATUS (25h), see Figure 15.
IEN[1:0]	Configure the signal routed to the INT pin, see Table 16.



- PRES_FLAG , MOT_FLAG, TAMB_SHOCK_FLAG from FUNC_STATUS (25h)
- ❖ INT_OR is enabled by IEN[1:0] = "10"

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STATUS (23h)

Table 16. IEN[1:0] configuration

IEN[1:0]	INT pin
00	high-Z
01	Data ready (DRDY)
10	INT_OR

10.8 STATUS (23h)

Read only - default = 00h

7	6	5	4	3	2	1	0
-	-	-	-	-	DRDY	-	-

Data ready for TAMB, TOBJ, TAMB_SHOCK, TPRESENCE, TMOTION. This bit is reset to 0 when reading the FUNC_STATUS (25h) register.

(0: no set of output data is available; 1: new set of output data is available)

10.9 FUNC_STATUS (25h)

Read only – default = 00h

7	6	5	4	3	2	1	0
-	-	-	-		PRES_FLAG	MOT_FLAG	TAMB_ SHOCK_FLAG

PRES FLAG	Presence detection flag. This bit is reset to 0 when reading the FUNC_STATUS (25h) register. Default value: 0
FRES_FLAG	(0: no presence is detected; 1: presence is detected)
MOT FLAG	Motion detection flag. This bit is reset to 0 when reading the FUNC_STATUS (25h) register. Default value: 0
MOT_I LAG	(0: no motion is detected; 1: motion is detected)
TAMB_SHOCK_FLAG	Ambient temperature shock detection flag. This bit is reset to 0 when reading the FUNC_STATUS (25h) register. Default: 0
	(0: no ambient temperature shock is detected; 1: ambient temperature shock is detected)

10.10 TOBJECT_L (26h)

Read only – default = 00h

7	6	5	4	3	2	1	0	
TOBJECT7	TOBJECT6	TOBJECT5	TOBJECT4	TOBJECT3	TOBJECT2	TOBJECT1	TOBJECT0	

TOBJECT[7:0] TOBJECT LSB data

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TOBJECT_H (27h)

10.11	│ TOBJECT_H(27h)

Read only – default = 00h

7	6	5	4	3	2	1	0
TOBJECT15	TOBJECT14	TOBJECT13	TOBJECT12	TOBJECT11	TOBJECT10	TOBJECT9	TOBJECT8

TOBJECT[15:8]

TOBJECT MSB data

The TOBJECT (object temperature) output value is 16-bit data that contains the measured temperature of the object. It is composed of TOBJECT_H (27h) and TOBJECT_L (28h). The value is expressed as 2's complement and its sensitivity is 2000 LSB/°C.

10.12 TAMBIENT_L (28h)

Read only - default = 00h

7	6	5	4	3	2	1	0
TAMBIENT7	TAMBIENT6	TAMBIENT5	TAMBIENT4	TAMBIENT3	TAMBIENT2	TAMBIENT1	TAMBIENT0

TAMBIENT[7:0]

Ambient temperature LSB data

10.13 TAMBIENT_H (29h)

Read only - default = 00h

7	6	5	4	3	2	1	0	
TAMBIENT15	TAMBIENT14	TAMBIENT13	TAMBIENT12	TAMBIENT11	TAMBIENT10	TAMBIENT9	TAMBIENT8	

TAMBIENT[15:8]

Ambient temperature MSB data

The TAMBIENT (ambient temperature) output value is 16-bit data that contains the ambient temperature. It is composed of TAMBIENT_H (28h) and TAMBIENT_L (29h). The value is expressed as 2's complement and its sensitivity is 100 LSB/°C.

10.14 TPRESENCE_L (3Ah)

Read only - default = 00h

7	6	5	4	3	2	1	0	
TPRESENCE7	TPRESENCE6	TPRESENCE5	TPRESENCE4	TPRESENCE3	TPRESENCE2	TPRESENCE1	TPRESENCE0	

TPRESENCE[7:0]

Presence detection output using embedded algorithms, LSB data

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TPRESENCE_H (3Bh)

10.15 TPRESENCE_H (3Bh)

Read only - default = 00h

7	6	5	4	3	2	1	0
TPRESENCE15	TPRESENCE14	TPRESENCE13	TPRESENCE12	TPRESENCE11	TPRESENCE10	TPRESENCE9	TPRESENCE8

TPRESENCE[15:8] Presence detection output using embedded algorithms, MSB data

The TPRESENCE (presence) output value is 16-bit data that contains the presence data. It is composed of TPRESENCE_H (3Bh) and TPRESENCE_L (3Ah). The value is expressed as 2's complement.

10.16 TMOTION_L (3Ch)

Read only - default =00h

7	6	5	4	3	2	1	0	
TMOTION 7	TMOTION 6	TMOTION 5	TMOTION 4	TMOTION 3	TMOTION 2	TMOTION 1	TMOTION 0	

TMOTION[7:0] Motion detection output using embedded algorithms, LSB data

10.17 TMOTION_H (3Dh)

Read only - default = 00h

/	0	5	4	3	2	1	0
TMOTION 15	TMOTION 14	TMOTION 13	TMOTION 12	TMOTION 11	TMOTION 10	TMOTION 9	TMOTION 8

TMOTION[15:8] Motion detection output using embedded algorithms, MSB data

The TMOTION (motion) output value is 16-bit data that contains the motion data. It is composed of TMOTION_H (3Dh) and TMOTION_L (3Ch). The value is expressed as 2's complement.

10.18 TAMB_SHOCK_L (3Eh)

Read only - default = 00h

7	6	5	4	3	2	1	0
TAMB_SHOCK7	TAMB_SHOCK6	TAMB_SHOCK5	TAMB_SHOCK4	TAMB_SHOCK3	TAMB_SHOCK2	TAMB_SHOCK1	TAMB_SHOCK0

TAMB_SHOCK[7:0] Ambient shock detection output using embedded algorithms, LSB data

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TAMB_SHOCK_H (3Fh)

10.19 TAMB_SHOCK_H (3Fh)

Read only - default = 00h

7	6	5	4	3	2	1	0
TAMB_SHOCK15	TAMB_SHOCK14	TAMB_SHOCK13	TAMB_SHOCK12	TAMB_SHOCK11	TAMB_SHOCK10	TAMB_SHOCK9	TAMB_SHOCK8

TAMB_SHOCK[15:8]

Ambient shock detection output using embedded algorithms, MSB data

The TAMB_SHOCK (ambient temperature shock) output value is 16-bit data that contains the ambient temperature shock data. It is composed of TAMB_SHOCK_H (3Fh) and TAMB_SHOCK_L (3Eh). The value is expressed as 2's complement.



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Embedded functions description

11 Embedded functions description

The following registers are used to configure the embedded functions page. These registers are accessible when the FUNC CFG ACCESS bit in CTRL2 (21h) is set to '1'.

11.1 FUNC_CFG_ADDR (08h)

RW - default = 00h

7 6 5 4 3 2 1 0

FUNC_CFG_ADDR[7:0]

FUNC_CFG_ADDR[7:0]

Address of embedded feature that has to be read or written according to the configuration bits in the PAGE_RW (11h) register.

11.2 FUNC_CFG_DATA (09h)

RW - default = 00h

Tive actuall out

7 6 5 4 3 2 1 0

FUNC_CFG_DATA[7:0]

FUNC_CFG_DATA[7:0]

Data byte that will be read or written to the address of the page indicated by FUNC_CFG_ADDR (08h) according to the configuration bit in PAGE_RW (11h).

11.3 PAGE_RW (11h)

RW default = 00h

7	6	5	4	3	2	1	0
-	FUNC_CFG WRITE	FUNC_CFG READ		-	-	-	-

FUNC_CFG_WRITE

When set to '1', enables the write procedure for embedded functions.

FUNC_CFG_READ

When set to '1', enables the read procedure for embedded functions.

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11.4 FUNC CFG WRITE procedure

Write procedure example: write value yyh in the register at address xxh of the embedded functions page

Write bit FUNC_CFG_ACCESS = 1 in CTRL2 (21h) // Enable access to the embedded functions registers

Write bit FUNC_CFG_WRITE = 1 in PAGE_RW (11h) // Select write operation mode

Write xx in FUNC_CFG_ADDR (08h) // Set address

Write yy in FUNC_CFG_DATA (09h) // Set value to be written

Write bit FUNC_CFG_WRITE = 0 in PAGE_RW (11h) // Disable write operation

Write bit FUNC_CFG_ACCESS = 0 in CTRL2 (21h) // Disable access to the embedded functions registers

11.5 FUNC_CFG READ procedure

Read procedure example: read the value of the register at address xxh of the embedded functions page

Write bit FUNC_CFG_ACCESS = 1 in CTRL2 (21h) // Enable access to the embedded functions registers

Write bit FUNC_CFG_READ = 1 in PAGE_RW (11h) // Select read operation mode

Write xx in FUNC_CFG_ADDR (08h) // Set address

Read value of FUNC_CFG_DATA (09h) // Get register value

Write bit FUNC_CFG_READ = 0 in PAGE_RW (11h) // Disable read operation

Write bit FUNC_CFG_ACCESS = 0 in CTRL2 (21h) // Disable access to the embedded functions registers

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Embedded functions registers description

12 Embedded functions registers description

To read/write the embedded functions registers, refer to Section 11.4 FUNC_CFG WRITE procedure and Section 11.5 FUNC CFG READ procedure.

12.1 PRESENCE_THS (20h - 21h)

Presence threshold for presence detection algorithms. This value is 15-bit unsigned.

The default value is 200 (00C8h).

7	6	5	4	3	2	1	0
PRESENCE_THS7	PRESENCE_THS6	PRESENCE_THS5	PRESENCE_THS4	PRESENCE_THS3	PRESENCE_THS2	PRESENCE_THS1	PRESENCE_THS0
15	14	13	12	11	10	9	8
-	PRESENCE_THS14	PRESENCE_THS13	PRESENCE_THS12	PRESENCE_THS11	PRESENCE_THS10	PRESENCE_THS9	PRESENCE_THS8

12.2 MOTION_THS (22h - 23h)

Motion threshold for motion detection algorithm. This value is 15-bit unsigned.

The default value is 200 (00C8h).

7	6	5	4	3	2	1	0
MOTION_THS7	MOTION_THS6	MOTION_THS5	MOTION_THS4	MOTION_THS3	MOTION_THS2	MOTION_THS1	MOTION_THS0
15	14	13	12	11	10	9	8
-	MOTION_THS14	MOTION_THS13	MOTION_THS12	MOTION_THS11	MOTION_THS10	MOTION_THS9	MOTION_THS8

12.3 TAMB_SHOCK_THS (24h - 25h)

Ambient temperature shock threshold for Tambient shock detection algorithm. This value is 15-bit unsigned. The default value is 10 (000Ah).

7	6	5	4	3	2	1	0
TAMB_SHOCK7	TAMB_SHOCK6	TAMB_SHOCK5	TAMB_SHOCK4	TAMB_SHOCK3	TAMB_SHOCK2	TAMB_SHOCK1	TAMB_SHOCK0
15	14	13	12	11	10	9	8
-	TAMB_SHOCK14	TAMB_SHOCK13	TAMB_SHOCK12	TAMB_SHOCK11	TAMB_SHOCK10	TAMB_SHOCK9	TAMB_SHOCK8

12.4 HYST_MOTION (26h)

Hysteresis configuration value for motion detection algorithm. It is an 8-bit unsigned value in the registers. The default value is 32h.

7	6	5	4	3	2	1	0
HYST_MOTION7	HYST_MOTION6	HYST_MOTION5	HYST_MOTION4	HYST_MOTION3	HYST_MOTION2	HYST_MOTION1	HYST_MOTION0

12.5 HYST_PRESENCE (27h)

Hysteresis configuration value for presence detection algorithm. It is an 8-bit unsigned value in the registers. The default value is 32h.

7	6	5	4	3	2	1	0
HYST_							
PRESENCE7	PRESENCE6	PRESENCE5	PRESENCE4	PRESENCE3	PRESENCE2	PRESENCE1	PRESENCE0

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ALGO_CONFIG (28h)

12.6 ALGO_CONFIG (28h)

Algorithm configuration with 00h default value

7	6	5	4	3	2	1	0
-	-	-	-	INT_PULSED	-	SEL_ABS	-

INT_PULSED	When '1', the flags as a result of the algorithms will be pulsed (high for ODR defined) on INT pin. Default value: 0
	(0: latched mode; 1: pulsed mode)
SEL ABS	Selects the absolute value in presence detection algorithm. Default value: 0
OLL_ABS	(0 : ABS is not applied ; 1: ABS is applied)

12.7 HYST_TAMB_SHOCK (29h)

Hysteresis configuration value for ambient temperature shock detection algorithm. It is an 8-bit unsigned value in the registers. The default value is 02h.

7	6	5	4	3	2	1	0
HYST_TAMB_	HYST_TAMB_S						
SHOCK7	HOCK6	HOCK5	HOCK4	HOCK3	HOCK2	HOCK1	HOCK0

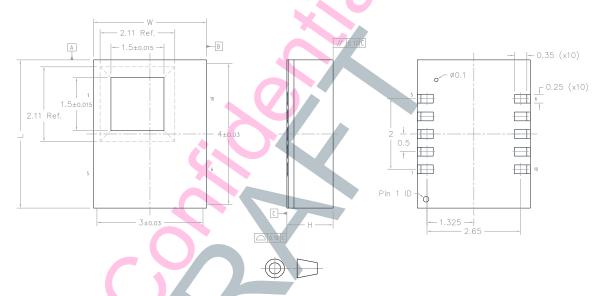
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13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

13.1 OLGA-10L 3.2 x 4.2 x 1.455 mm package information

Figure 16. OLGA-10L (3.2 x 4.2 x 1.455 mm) package outline and mechanical data



Dimensions are in millimeter unless otherwise specified General Tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Width [W]	3.2	±0.1
Length [L]	4.2	±0.1
Height [H]	1.455	MAX

DM00488758 4

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Revision history

Table 17. Document revision history

Date	Version	Changes
19-Mar-2021	0.1	Initial draft release
		Updated Section 6.1 Presence detection, Section 6.2 Motion detection, and Section 6.3 Ambient temperature shock detection
		Updated Section 9.1 Embedded functions page register mapping
		Updated LPF1 (0Ch), LPF2 (0Dh), AVG_TRIM (10h), CTRL2 (21h), CTRL3 (22h), STATUS (23h), FUNC_STATUS (25h), removed register 24h (reserved)
28-May-2021	0.2	Updated Section 11 Embedded functions description and subsections.
20	V	Updated Section 12 Embedded functions registers description
		Updated HYST_MOTION (26h)
		Added HYST_PRESENCE (27h)
		Updated ALGO_CONFIG (28h)
		Added HYST_TAMB_SHOCK (29h)
		Added product resources table on page 1
04-Jun-2021	0.3	Updated Section 8 Soldering guidelines
		Updated 101 (512)
	0.4	Updated "Sensing specification" in Features
		Updated Table 2. Sensor specifications
17-Sep-2021		Added Table 8. Internal pin status
17-3ep-2021		Updated Table 9. Register map
		Updates throughout Section 10 Registers description
		Textual updates
		Added sustainable technology logo
12-Oct-2021	0.5	Updated 101 (512)
		Updated FUNC_STATUS (25h) and TAMB_SHOCK_THS (24h - 25h)
		Updated package image, Features, Applications, Section 1 Overview
28-Jan-2022	0.6	Updated Section 6.1 Presence detection and Figure 10. Presence algorithm block diagram
		Updated Section 10.5 CTRL1 (20h) and Table 15. Current consumption at different ODRs and AVG_TMOS setting
		Updated Features, Description, and Section 1 Overview
		Updated Table 2. Sensor specifications
18-Apr-2022	0.7	Updated Table 13. Averaging selection for object temperature and noise
		Updated Table 15. Current consumption at different ODRs and AVG_TMOS setting
OF Mar: 0000	0.0	Updated Table 2. Sensor specifications (T _{obj_s} and T _{amb_a})
25-May-2022	8.0	Minor textual updates

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