

Fast-Switching GaN-Based Class-D/H Audio Power Amplifier

STUDENT RESEARCH PROJECT

Submitted by

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Period: 01.11.2024 – 01.06.2025

Stuttgart, 01.06.2025

Overview

Type of thesis:	Student Research Project
English title:	Fast-Switching GaN-Based Class-D/H Audio Power Amplifier
German title:	Schnell Schaltende GaN basierte Klasse-D/H Audio Leistungsverstärker
Student:	Chenyan Jia
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Date of Examination:	01.06.2025

Statutory Declaration

I hereby declare that this thesis is my own work and effort and follows the regulations related to good scientific practice of the University of Stuttgart in its latest form. All sources cited or quoted are indicated and acknowledged by means of a comprehensive list of references.

Stuttgart, 01.06.2025

Chenyan Jia

A handwritten signature in black ink, appearing to read "Chenyan Jia".

Executive Abstract

In recent years, the rising demand for high-efficiency and high-fidelity audio amplification has driven significant interest in digital switching amplifier technologies, particularly Class D and its extensions. Traditional analog amplifiers like Class A, B, and AB offer excellent linearity and low total harmonic distortion (THD) around 0.001% but are limited to peak efficiencies around 60%, requiring large heat sinks due to substantial heat dissipation. Silicon-based Class D amplifiers improve efficiency to about 90%, but at switching frequencies above 500 kHz, MOSFET gate charge and switching losses become significant, leading to trade-offs between efficiency, size, and EMI performance.

GaN devices offer higher electron mobility, low gate charge, and low on-resistance, resulting in lower losses and enabling higher switching frequencies for increased power density. This makes GaN technology highly promising for compact, high-performance audio systems with low harmonic distortion.

This thesis presents the development of a digital Class D/H audio amplifier leveraging GaN technology. It covers system architecture, hardware and software design, electrical design, theoretical and optimal controller parameter calculations, simulations, and experimental validation.

The final prototype achieves 96% efficiency at up to 200 W output power, with a power density of 6 W/cm³ and a switching frequency of 300 kHz. The amplifier maintains a low THD of 0.03%. A Class H adaptive voltage control dynamically adjusts supply voltage to improve efficiency under varying audio amplitudes. Software features include an audio signal detector, RTOS-based multitasking, an enhanced THD analyzer, and digital Butterworth filtering to enhance audio quality, closely matching the Harman curve.

Zusammenfassung

In den letzten Jahren hat die steigende Nachfrage nach hocheffizienter und hochwertiger Audioverstärkung das Interesse an digitalen Schaltverstärkertechnologien, insbesondere an Class-D-Verstärkern und deren Erweiterungen, erheblich verstärkt. Traditionelle analoge Verstärker wie Class A, B und AB bieten zwar eine ausgezeichnete Linearität und eine geringe Gesamte harmonische Verzerrung (THD) von etwa 0,001%, sind jedoch auf Spitzeneffizienzen von rund 60% begrenzt. Aufgrund erheblicher Wärmeverluste im Betrieb erfordern sie große Kühlkörper.

Siliziumbasierte Class-D-Verstärker steigern die Effizienz auf etwa 90%. Allerdings nehmen bei Schaltfrequenzen über 500 kHz die Gate-Ladung der MOSFETs und die Schaltverluste deutlich zu, was zu Zielkonflikten zwischen Effizienz, Baugröße und EMV-Verhalten führt.

GaN-Bauelemente bieten eine höhere Elektronenbeweglichkeit, eine geringe Gate-Ladung und einen niedrigen Durchlasswiderstand, was zu geringeren Verlusten führt und höhere Schaltfrequenzen ermöglicht. Dadurch kann die Leistungsdichte gesteigert werden. Diese Eigenschaften machen die GaN-Technologie zu einer vielversprechenden Lösung für kompakte, leistungsstarke Audiosysteme mit niedrigen harmonischen Verzerrungen.

Diese Arbeit präsentiert die Entwicklung eines digitalen Class-D/H-Audioverstärkers auf Basis der GaN-Technologie. Sie behandelt die Systemarchitektur, die Hard- und Softwaregestaltung, das elektrische Design, die theoretische und optimale Auslegung der Reglerparameter, Simulationen sowie die experimentelle Validierung.

Der entwickelte Prototyp erreicht eine Effizienz von 96% bei einer Ausgangsleistung von bis zu 200 W, eine Leistungsdichte von 6 W/cm³ sowie eine Schaltfrequenz von 300 kHz. Der Verstärker weist eine niedrige THD von 0,03% auf. Eine adaptive Class-H-Spannungsregelung passt die Versorgungsspannung dynamisch an, um die Effizienz bei variierenden Audioamplituden zu verbessern. Zu den Software-Funktionen gehören ein Audio-Signaldetektor, RTOS-basiertes Multitasking, ein verbesserter THD-Analysator sowie eine digitale Butterworth-Filterung zur Verbesserung der Audioqualität, die sich eng an der Harman-Kurve orientiert.

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Abbreviations and Symbols

Abbreviations

Notation	Description
ACR	ac resistance
ADC	analog-to-digital converter
BP	band pass
CPU	central processing unit
CSI	common source inductor
DCR	dc resistance
DMA	direct memory access
DSP	digital signal processor
EMI	electromagnetic interference
ESR	equivalent series resistance
FET	field-effect transistor
FFT	fast fourier transform
FPGA	field-programmable gate array
GaN	gallium nitride
HP	high pass
HS	high side
LP	low pass
MCU	microcontroller unit
MMCX	micro-miniature coaxial
MOSFET	metal–oxide–semiconductor field-effect transistor
NMOS	n-metal-oxide-semiconductor field-effect transistor
OPAMP	operational amplifier
PC	personal computer

Abbreviations

Notation	Description
PCB	printed circuit board
PMOS	p-metal-oxide-semiconductor field-effect transistor
PWM	pulse width modulation
RTOS	real-time operating system
THD	total harmonic distortion
ZVS	zero voltage switching

Symbols

Symbol	Description	Unit
C_{GS}	gate-source capacitance	F
C_{OSS}	output capacitance	F
E_{OSS}	output capacitance loss energy	J
g_m	transconductance	S
L_{CSI}	commen source inductor	H
$P_{Conduction}$	conduction loss	W
$P_{Dynamic}$	total dynamic loss	W
P_G	gate loss	W
P_{HS}	total device hard-switching loss	W
P_L	inductor loss	W
P_{OSS}	output capacitance loss	W
P_{SD}	3rd Quadrant Conduction Loss	W
P_{sw}	switching Loss	W
P_{Total}	total estimated loss	W
Q_{GS}	gate-source charge	C
Q_{OSS}	output charge	C
R_{CSI}	common source resistance	Ω
V_{bias}	bias voltage	V
V_{CSI}	common source inductor voltage	V
V_{DS}	drain-source voltage	V
V_{GS}	gate-source voltage	V
V_{gseff}	effective gate-source voltage	V
V_{SD}	reverse-blocking voltage	V
V_{th}	threshold voltage	V

1 Introduction

1.1 Concept of Audio Amplifier

An audio amplifier is an electronic device or circuit designed to increase the amplitude (volume) of audio signals. It takes a low-power audio signal, such as one from a microphone, smartphone, or media player, and boosts it to a level powerful enough to drive output devices like loudspeakers or headphones.

An audio amplifier receives a small analog audio signal / (now gradually) digital audio signal (usually a few millivolts), then:

- Amplifies the voltage and/or current
- Maintains the original waveform shape (i.e., fidelity)
- Outputs a stronger signal capable of moving a speaker cone
- The amplifier ensures minimal distortion, low noise, and stable gain to preserve audio quality.

In recent years, the growing demand for high-efficiency, high-fidelity audio amplification has sparked considerable interest in digital switching amplifier technologies, particularly Class D and its extensions. However, traditional analog amplifiers, such as Class A, B, and AB, though offering excellent linearity and low total harmonic distortion (THD) around 0.001%, are limited by low peak efficiency of only around 60%, with a significant portion of power dissipated as heat during static bias operation. This necessitates large heat sinks and bulky designs.

Silicon-based Class D amplifiers improve peak efficiency to approximately 90% by operating in a switching mode. However, at carrier frequencies above 500 kHz, metal–oxide–semiconductor field-effect transistor (MOSFET) gate charge and switching losses increase significantly. Further increasing the switching frequency to reduce the size of the output LC filter introduces an exponential trade-off between efficiency and electromagnetic interference (EMI) performance.

To address these challenges, gallium nitride (GaN) devices offer significant advantages due to their higher electron mobility, low gate charge, and low on-resistance, all contributing to lower losses. Furthermore, their ability to operate at higher switching frequencies enables increased power density, making GaN technology a promising solution for achieving compact layouts and maintaining low harmonic distortion in high-performance audio systems.

1 Introduction

The following sections of this chapter will provide a detailed explanation of the characteristics of various amplifier topologies and highlight the advantages of the GaN-based Class D/H amplifier.

1.1.1 Analog Audio Amplifier

Firstly, the analog Audio Amplifier is introduced. The most traditional types are the following: Class A, B and AB amplifier.

A Class A amplifier, according to fig. 1.1 is consisting of 2 transistors (here 2 n-metal-oxide-semiconductor field-effect transistor (NMOS)) to drive the output signal; with the transistor below always ON with a given bias source, which ensures that $V_{GS} > V_{th}$, here the V_{GS} and V_{th} correspond respectively the gate-source voltage of transistor and threshold voltage of transistor. A constant bias V_B , and the current I_Q can be also regarded as constant. Now the bottom NMOS is equivalent as a current source to provide a DC working point.

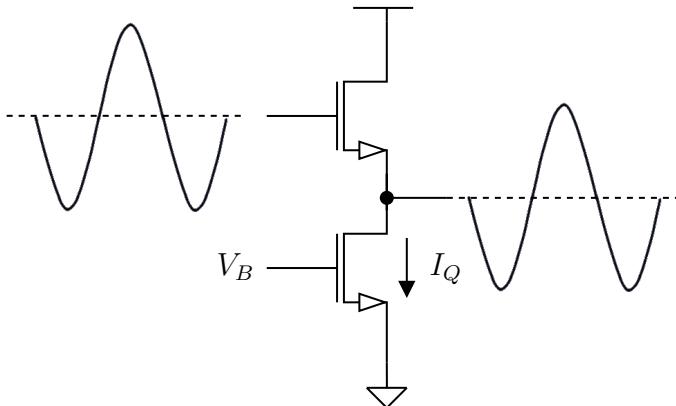


Figure 1.1: Topology of class A amplifier

As a classic analog amplifier it shows a very low THD around 0.001%, but the low efficiency about 60 % (Low side transistor is always on no matter if there is any input signal) and high heating problem cause it to not be widely implemented for practical use.

Class B amplifier, according to the fig. 1.2, avoid such a disadvantage with connecting the Gate of both NMOS and p-metal-oxide-semiconductor field-effect transistor (PMOS) to increase the efficiency. However, lack of bias source it products a dead zone around the zero Voltage. It causes big distortion especially for tiny input signal.

Class AB amplifier, according to fig. 1.3, is a combination of both class A and B amplifiers. It uses 2 diodes or 2 symmetric groups of diodes to produce a small bias, which enables that $V_{bias} > V_{th}$, to run the amplifier above the cut-off point.

But there are still some disadvantages for it[10]:

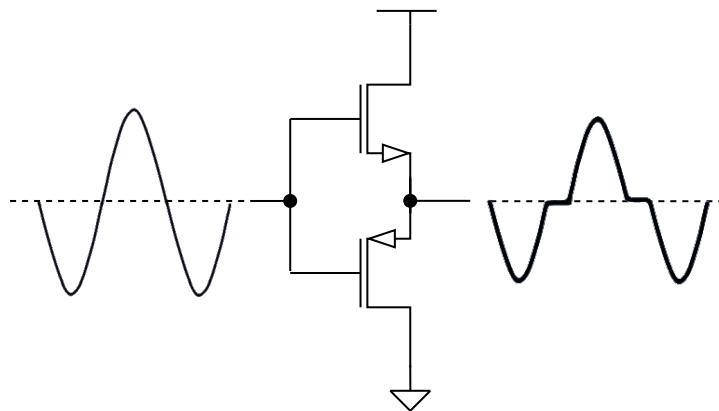


Figure 1.2: Topology of class B amplifier

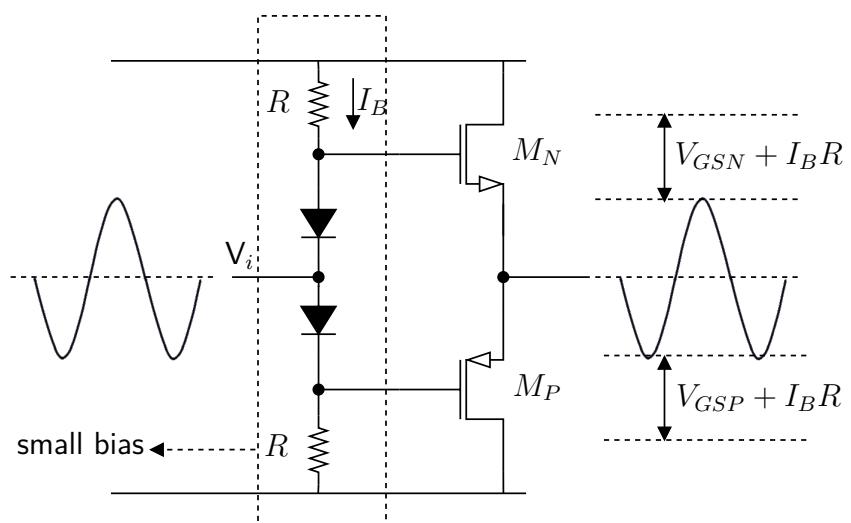


Figure 1.3: Topology of class AB amplifier

1 Introduction

- static loss: the bias circuit produces static loss over diodes and resistors.
- cross-distortion: each transistor will conduct slightly more than one half cycle, which depends on the practically chosen bias point.
- NMOS based class AB amplifier: limited output range due to headroom requirements.
- a fixed voltage supply, which is defined by the peak value of input, can be inefficient for tiny audio signals.

1.1.2 Digital Audio Amplifier

The most famous topology of digital audio amplifier could be class G, class H and class D amplifier. Class G and H amplifier are designed to solve the loss caused by the fixed voltage supply, which is mentioned above.

Classic class G amplifier, according to the fig. 1.4, includes a class AB amplifier and a signal detector connecting with an adjustable voltage supply. It ensures that the amplifier has several optional levels of voltage supply, which can be adjusted to reduce the loss.

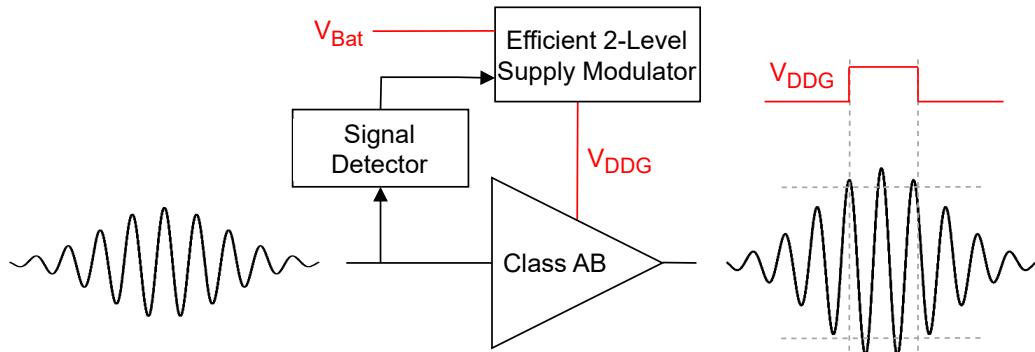


Figure 1.4: Topology of class G amplifier

Class H amplifier, according to fig. 1.5, corresponds to an ideal case, when the number of levels of voltage supply from class G is increased to infinity (or a much higher range), which leads to a higher efficiency.

However, another disadvantage here is that the transistors always operate as amplifiers in the linear or saturation range. The loss of the transistors themselves, especially when a large current flows through them, causes some distortion.

An ideal switch therefore could be:

- large current passing through and no voltage dropping across (switch ON);
- large voltage dropping across and no current passing through (switch OFF).

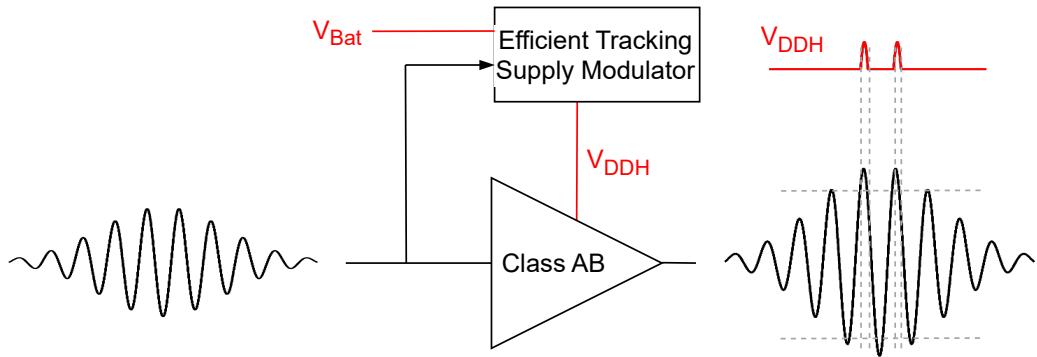


Figure 1.5: Topology of class H amplifier

These requirements promoted the birth of class D amplifier. With pulse width modulation (PWM) technology, the power loss can although practically not 100% be eliminated, but uniformly, not proportionally with the loading current. According to fig. 1.6 [10], which shows only one direction of output voltage, for bi-directional output, a H-bridge is useful. Afterwards, the output will be filtered by either external filter or by the speaker coil itself.

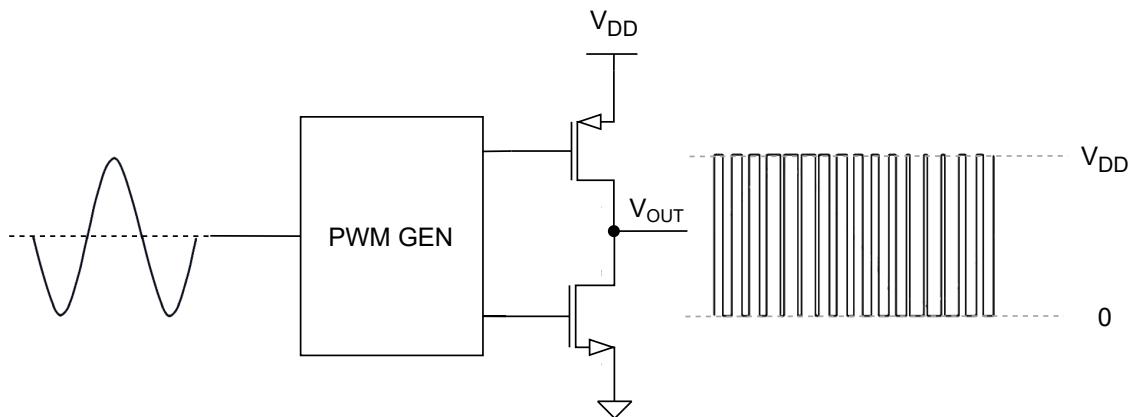


Figure 1.6: Topology of class D amplifier

1.2 Comparison of different types of Audio Amplifier

A summery list is here provided in table 1.1 [10], to describe the feature of all common audio amplifiers, including the amplifiers written above.

The thesis [10] also provides fig. 1.7 describing about the comparison of common audio amplifiers' efficiency. The figure shows a significant difference of efficiency for different kinds of common

Table 1.1: Property of common audio amplifiers

Amplifier's Type	Feature
Class A	Audio signal loading on the high side of half bridge, with low side transistor connecting to a voltage bias working as a current source
Class B	Audio signal loading on gates of both high and low side of half bridge, save power however with deadzone
Class AB	combining both feature of class A and B amplifier but with relatively big static loss
Class G	based on class AB (traditional) or class D (advanced) amplifier, with 2 multiple constant level of voltage supply for higher efficiency
Class H	based on class AB (traditional) or class D (advanced) amplifier, with multiple constant level of voltage supply for higher efficiency
Class D	use PWM modulation with bridge to generate a square wave output
Class C	has the greatest efficiency but the poorest linearity
Class E/F	uses harmonic resonators in the output network to shape the output waveform into a square wave, are capable of high efficiencies of more than 90% if infinite harmonic tuning is used
Class I	has two sets of complementary output switching devices arranged in a parallel pushpull configuration with both sets of switching devices sampling the same input waveform
Class S	is a nonlinear switching mode amplifier similar in operation to the class D amplifier
Class T	combines both the low distortion signal levels of a class AB amplifier and the power efficiency of a class D amplifier

audio amplifiers. The development of power electronic provide class D amplifier components with higher frequency and lower power loss, which makes it nowadays the most effective audio amplifier with excellent performance and acceptable loss ration.

1.3 Class D/H Audio Amplifier

Therefore a class D audio amplifier will be implemented in this thesis. In order to further reduce the power loss, an additional class H/G Intermediate Processor would also be put into use, which supports an automatic adjustment of DC side voltage supply of PWM. Besides in order to reduce the complexity of the DC side of PWM, a Full Bridge (H Bridge) rather than a half bridge will be implemented. The whole structure of the class D/H audio amplifier is shown in fig. 1.8:

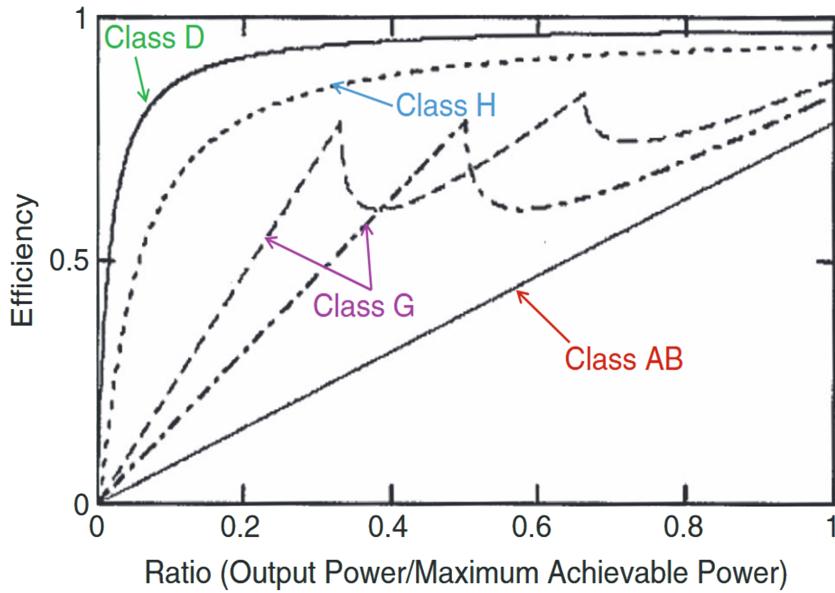


Figure 1.7: Comparison of common audio amplifiers' efficiency [10]

1.4 Structure and Block Diagram of the Class D + H Audio Amplifier

According to discussions above, the basic structure of the whole audio amplifier is designed as the following fig. 1.9:

It clarifies, that the whole system consists of 4 types of main elements:

- microcontroller unit (MCU) (red): STM series chip will be used.
- Peripheral-devices (blue): included input/output interface.
- Functional block (purple): each corresponds a concrete function, for example operational amplifier (OPAMP), DC-DC converter
- Sub-block (green): each sub-block is also a block with lower-level, integrated in each functional block.

Furthermore, it can be divided into 3 boards as showed in fig. 1.10

Based on this design approach, high-voltage, high-power signals are isolated from low-voltage, low-power signals, thereby enabling safer and more reliable operation.

Based on the structure above, the theoretical foundation of the model will be discussed in following sections in two parts:

1 Introduction

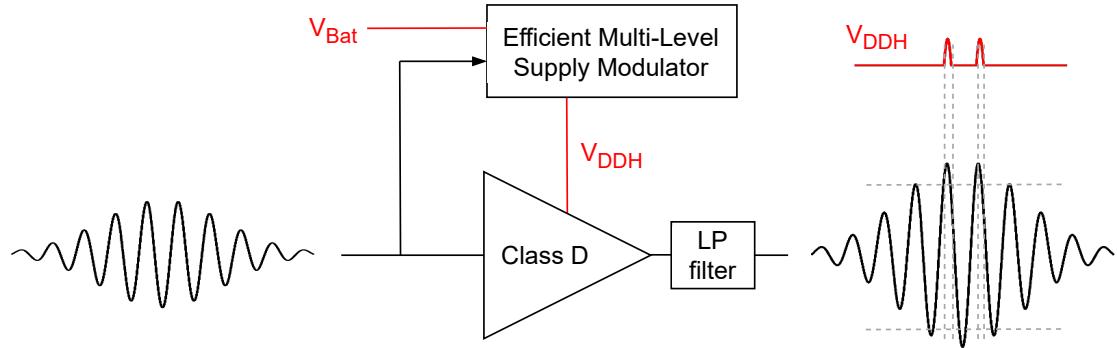


Figure 1.8: Topology of class D/H audio amplifier

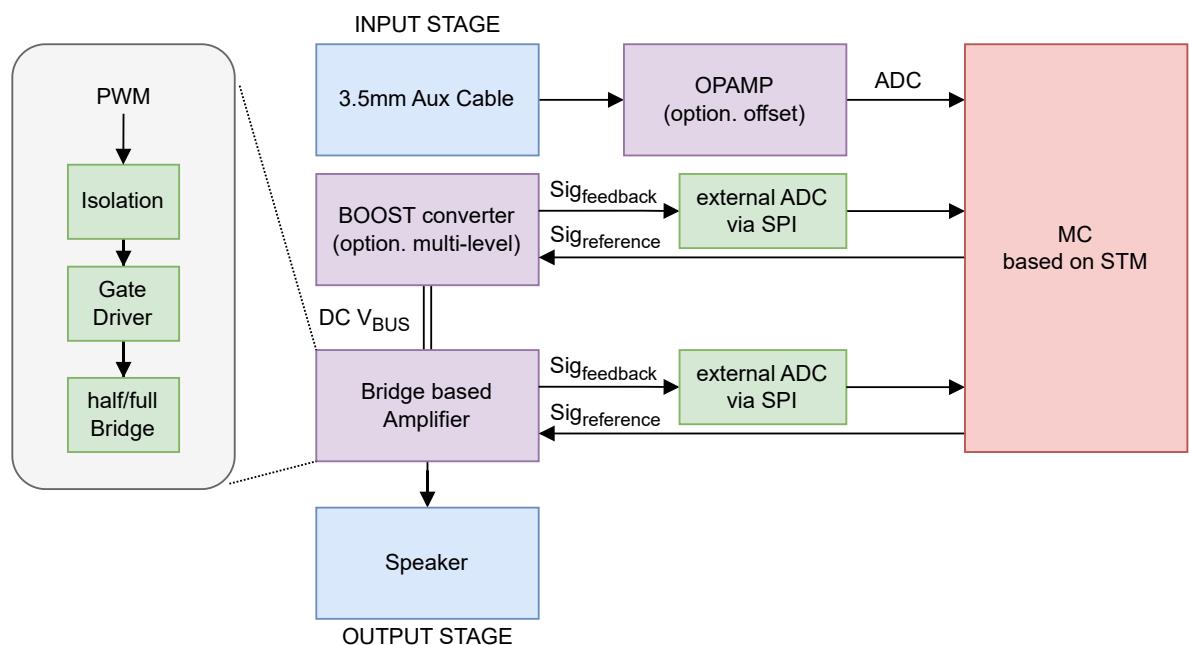


Figure 1.9: System's block diagram

1.4 Structure and Block Diagram of the Class D + H Audio Amplifier

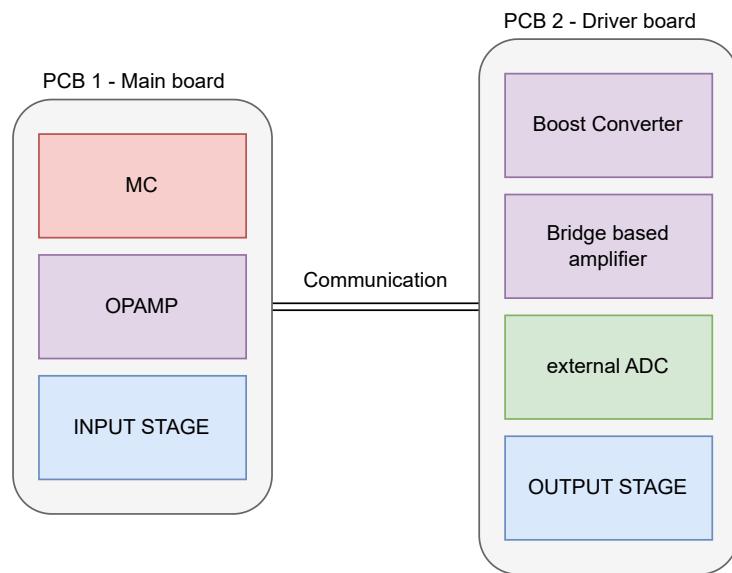


Figure 1.10: Board division

- Boost controller: modeling and controlling strategy
- H-Bridge PWM Amplifier: modulation strategy and topology

2 Modeling and Simulation of the Boost Converter

Given that this is a Class D/H system, the boost converter requires a robust controller, and traditional uncontrolled multi-level boost converter is unsuitable. In this chapter the system topology is presented and then continued with an efficient controller.

2.1 Topology of a Boost Converter

The whole model can be simplified as the following fig. 2.1.

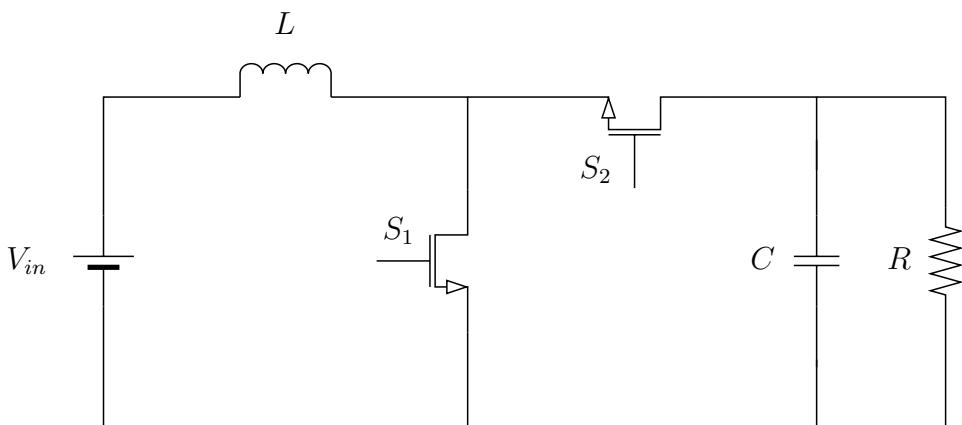


Figure 2.1: Topology of boost converter with synchronous rectifier

Here S_1 and S_2 are two complementary GaN switches with a necessary dead-time zone, namely $\overline{S_1} = S_2$. S_1 works as a control switch, and S_2 works as a synchronous rectifier. The implementation of S_2 can eliminate voltage drop caused by diodes, which is used in conventional topology, in meanwhile the dead-time optimization makes the use of 3rd Quadrant of the synchronous rectifier for freewheeling no longer necessary.

2.2 Dynamic Modeling

2.2.1 Steady State Modeling

Defining the state vector as $x = [i_l \ v_c]^T$ and the output voltage $v_o = v_c$, the state space from during the S1::ON mode can be written as follows:

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}$$

$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix}$$
(2.1)

And during the S1::OFF mode:

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in}$$

$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix}$$
(2.2)

A state-space averaging approach is utilized to obtain a converter model across one switching period. In other words, the state-space descriptions of the two modes must be replaced with a single state-space description that approximates the behavior of the circuit across the whole time T. By using the state-space averaging technique, the averaged modified model is given by:

$$A = A_1d + A_2(1 - d) \quad (2.3)$$

$$B = B_1d + B_2(1 - d)$$

where A_x and B_x are given below, and d is the duty cycle:

$$\begin{aligned}
 A_1 &= \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \\
 A_2 &= \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \\
 B_1 &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \\
 B_2 &= \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}
 \end{aligned} \tag{2.4}$$

With these 2 equations given above, the whole system can be described as the following:

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-d)}{L} \\ \frac{(1-d)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_{in} \tag{2.5}$$

$$v_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} i_l \\ v_c \end{bmatrix}$$

The steady state can be calculated assuming:

$$\begin{bmatrix} \frac{di_l}{dt} \\ \frac{dv_c}{dt} \end{bmatrix} = 0 \tag{2.6}$$

so that:

$$\frac{v_o}{v_{in}} = \frac{1}{1-d} \tag{2.7}$$

2.2.2 Small Signal Modelling

To obtain the boost converter's transfer function, the model given by equations 2.5 must first be linearized around a particular operating point[11]:

2 Modeling and Simulation of the Boost Converter

$$\begin{cases} i_l = I_l + \tilde{i}_l \\ v_c = V_c + \tilde{v}_c \\ v_{in} = V_{in} + \tilde{v}_{in} \\ d = D + \tilde{d} \end{cases} \quad (2.8)$$

Use these new forms to replace previous equations:

$$\frac{d}{dt} \begin{bmatrix} I_l + \tilde{i}_l \\ V_c + \tilde{v}_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_l \\ V_c \end{bmatrix} + \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_l \\ \tilde{v}_c \end{bmatrix} + \begin{bmatrix} 0 & \frac{\tilde{d}}{L} \\ -\frac{\tilde{d}}{C} & 0 \end{bmatrix} \begin{bmatrix} I_l \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} [V_{in} + \tilde{v}_{in}] \quad (2.9)$$

In this equation it contains a steady-state:

$$\begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} I_l \\ V_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{in} = 0 \quad (2.10)$$

and simplify one part by:

$$\begin{bmatrix} 0 & \frac{\tilde{d}}{L} \\ -\frac{\tilde{d}}{C} & 0 \end{bmatrix} = \begin{bmatrix} \frac{V_c}{L} \\ -\frac{I_l}{C} \end{bmatrix} [\tilde{d}] \quad (2.11)$$

Hence, the Equation is reduced to:

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_l \\ \tilde{v}_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{(1-D)}{L} \\ \frac{(1-D)}{C} & -\frac{1}{RC} \end{bmatrix} \begin{bmatrix} \tilde{i}_l \\ \tilde{v}_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & \frac{V_c}{L} \\ 0 & -\frac{I_l}{C} \end{bmatrix} \begin{bmatrix} \tilde{v}_{in} \\ \tilde{d} \end{bmatrix} \quad (2.12)$$

$$\tilde{v}_o = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \tilde{i}_l \\ \tilde{v}_c \end{bmatrix} \quad (2.13)$$

In this research, we design a controller to generate duty cycle correction \tilde{d} in such a way that the output voltage remains constant. In this regard, we consider the transfer function given following using the state transition matrix, which may be expressed as follows in terms of the converter's

parameters:

$$G_{id}(s) = \frac{\tilde{i}_l(s)}{\tilde{d}(s)} = \frac{(V_c CR) \cdot s + 2V_c}{(LCR) \cdot s^2 + L \cdot s + RD'^2} \quad (2.14)$$

$$G_{vi}(s) = \frac{\tilde{v}_o(s)}{\tilde{i}_l(s)} = \frac{-L \cdot s + RD'^2}{D'(CR \cdot s + 2)} \quad (2.15)$$

where the $D' = 1 - D$.

To determine the appropriate parameter ranges for the inductors and output capacitors in the topology, the following electrical design criteria should be followed [3]

- for inductor,

$$\begin{aligned} \Delta I_L &= (0.2 \text{ to } 0.4) \cdot I_{out(max)} \cdot \frac{V_{out}}{V_{in}} \\ L &= \frac{V_{in} \cdot (V_{out} - V_{in})}{\Delta I_L \cdot f_s \cdot V_{out}} \end{aligned} \quad (2.16)$$

- for output capacitor,

$$C_{out,min} = \frac{I_{out,max} \cdot D}{f_s \cdot \Delta V_{out}} \quad (2.17)$$

According to eq. (2.16) and eq. (2.17), the value range of inductor and output capacitor in boost converter topology are respectively $L \geq 1\mu H$, $C \geq 8\mu F$.

Each parameter can be further determined in table 2.1 with some practical consideration of stability. Parameters from some commercially available boost converters were also taken into consideration [13].

Table 2.1: Parameters of boost converter

$P_{out,max}$	P_{RMS}	V_c	I_L	R	C	L	D	D'
400 W	200 W	48 V	16.67 A	11.52Ω	$20 \mu F$	$20 \mu H$	0.75	0.25

2.3 Double Closed Loop Controller

According to the figure fig. 2.2, the whole system can be divided into 3 parts:

- physical system

2 Modeling and Simulation of the Boost Converter

- current loop controller (internal loop)
- voltage loop controller (outer loop)

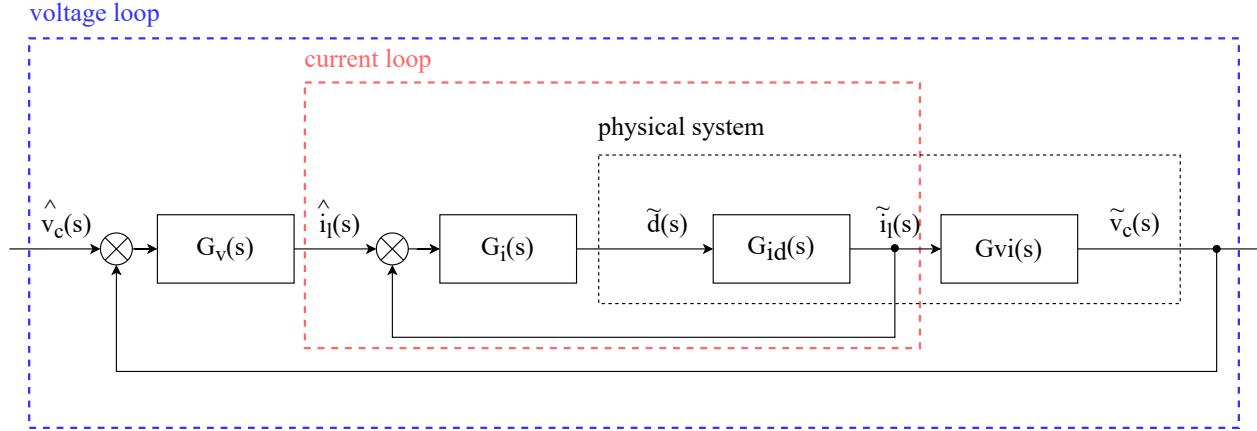


Figure 2.2: Boost controller

where the bandwidth of internal loop is around 10 times than that of outer loop, so when outer loop is running, the internal loop can be approximately seen as:

$$\hat{i}_l(s) = \tilde{i}_l(s) \quad (2.18)$$

where $\hat{i}_l(s)$ and $\tilde{i}_l(s)$ are respective the input and output of the current controller.

2.3.1 Controller $G_i(s)$ of Current Loop

Here we consider using ‘root locus of open loop transfer function’ to design the parameters of controller in current loop [9].

The open loop transfer function $G_{open,i}(s)$ is:

$$\begin{aligned} G_{open,i}(s) &= G_i(s) \cdot G_{id}(s) \\ &= \frac{K_{p,i} \cdot s + K_{i,i}}{s} \cdot \frac{a_1 \cdot s + a_0}{b_2 \cdot s^2 + b_1 \cdot s + b_0} \\ &= \frac{a_1 K_{p,i} s^2 + (a_1 K_{i,i} + a_0 K_{p,i}) s + a_0 K_{i,i}}{b_2 s^3 + b_1 s^2 + b_0 s} \end{aligned} \quad (2.19)$$

In order to get the equivalent Characteristic equation for $K_{p,i}$ from open loop transfer function,

the equivalent equations can be used here:

$$1 + G_{open,i}(s) = Q(s) + K_{p,i} \cdot P(s) = 0 \quad (2.20)$$

$$\begin{aligned} G_{open,i}^*(s)|_{K_{p,i}} &= \frac{P(s)}{Q(s)} \\ &= \frac{a_1 s^2 + a_0 s}{b_2 s^3 + b_1 s^2 + (a_1 K_{i,i} + b_0) s + a_0 K_{i,i}} \end{aligned} \quad (2.21)$$

Firstly the coefficient of $K_{i,i}$ in eq. (2.21) is selected to meet $a_1 \cdot K_{i,i} \gg b_0$, therefore the change of $K_{i,i}$ can be sensitive to influence the location of poles. And the value of $K_{i,i}$ should be big enough ensuring the bandwidth (speed) of current loop as high as possible (around 10^{-4} s), at least ten times bigger than the voltage loop [17].

The coefficient of $K_{i,i}$ in eq. (2.21) is selected to meet $a_1 \cdot K_{i,i} \gg b_0$, therefore the change of $K_{i,i}$ can greatly influence the location of poles.

Considering here $a_1 = 0.011$, $b_0 = 0.72$, it could be temporarily assumed that $K_{i,i} = 2e4$.

Root locus is applied with implementation of equivalent open loop transfer function $G_{open,i}^*(s)$ to choose a suitable $K_{p,i}$. Given 2 basic system requirements:

- the ‘system response time’ should be around 10^{-4} s, normally the bandwidth of current loop should be around 1/10 of the PWM Frequency (800 kHz), so here designed at least (800 kHz);
- the ‘system damping’ should be big enough, hence as small output overshoot as possible.

As for the first requirement, we consider two situations, the number of dominate poles in the final closed-loop transfer function (3 poles totally) is:

- $N = 1$: only one dominate pole, the whole system can be approximately regarded as a 1st-order System, $s = -\frac{1}{\tau}$. The bandwidth w_{BW} defines the frequency where the system gain drops until 70.7%(-3dB) of the DC gain. For a 1st-order system:

$$w_{BW} = \frac{1}{\tau} \geq 80 \text{ kHz} \quad (2.22)$$

- $N = 2$: two dominate poles as conjugate poles, the whole system can be approximately regarded as a 2nd-order System, $s = -\sigma \pm j\omega_d$. Here for a 2nd-order system (considered as critical damping), the bandwidth can be calculated as:

2 Modeling and Simulation of the Boost Converter

$$w_{BW} \approx 0.64\sigma \geq 80k\text{Hz} \quad (2.23)$$

In conclusion a line can be drawn here $x = -1.25e5 + j0$ in the 's-plane' as our critical line.

For the second requirement, we can consider a condition of 'Less than 5% overshoot'. This can be indicated by adding diagonal lines through the origin with a slope of $\frac{\Re}{\Im} = \pm|\frac{\ln(5\%)}{\pi}| \approx \pm 0.95$. where \Re and \Im represents the real and imaginary axis respectively, it shows in fig. 2.3.

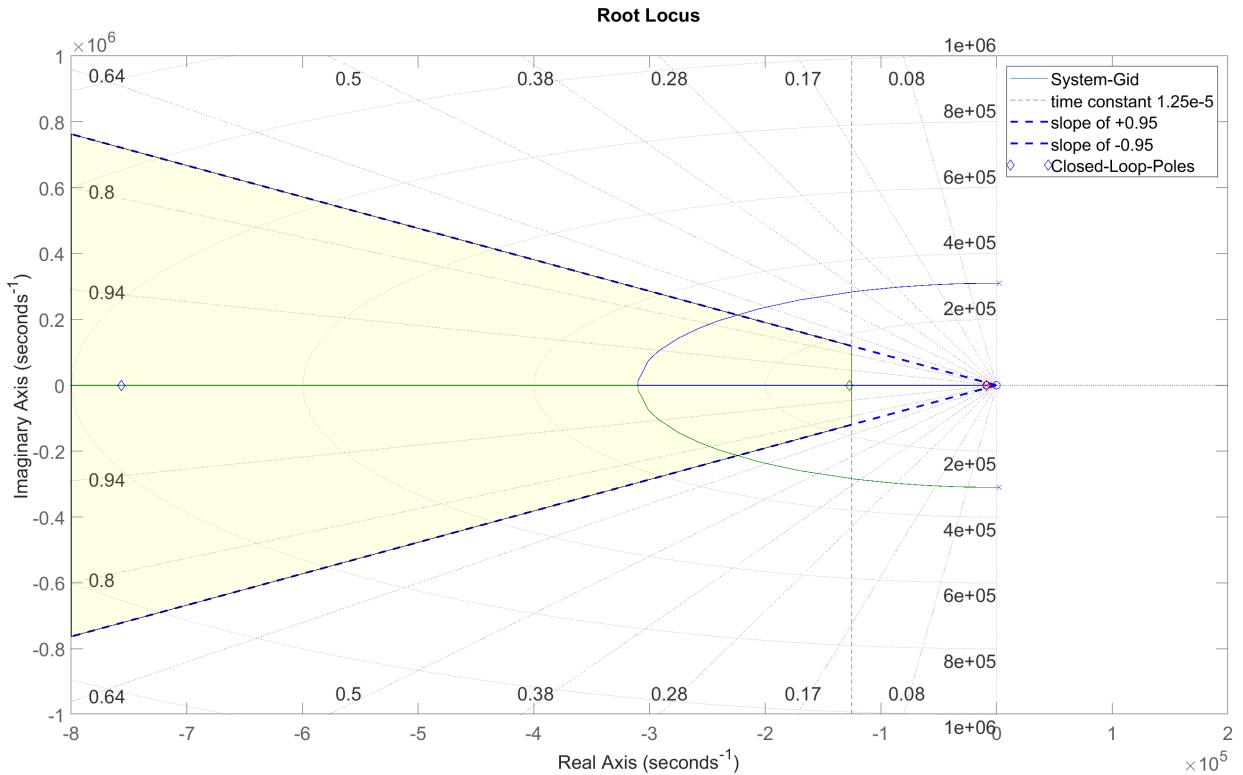


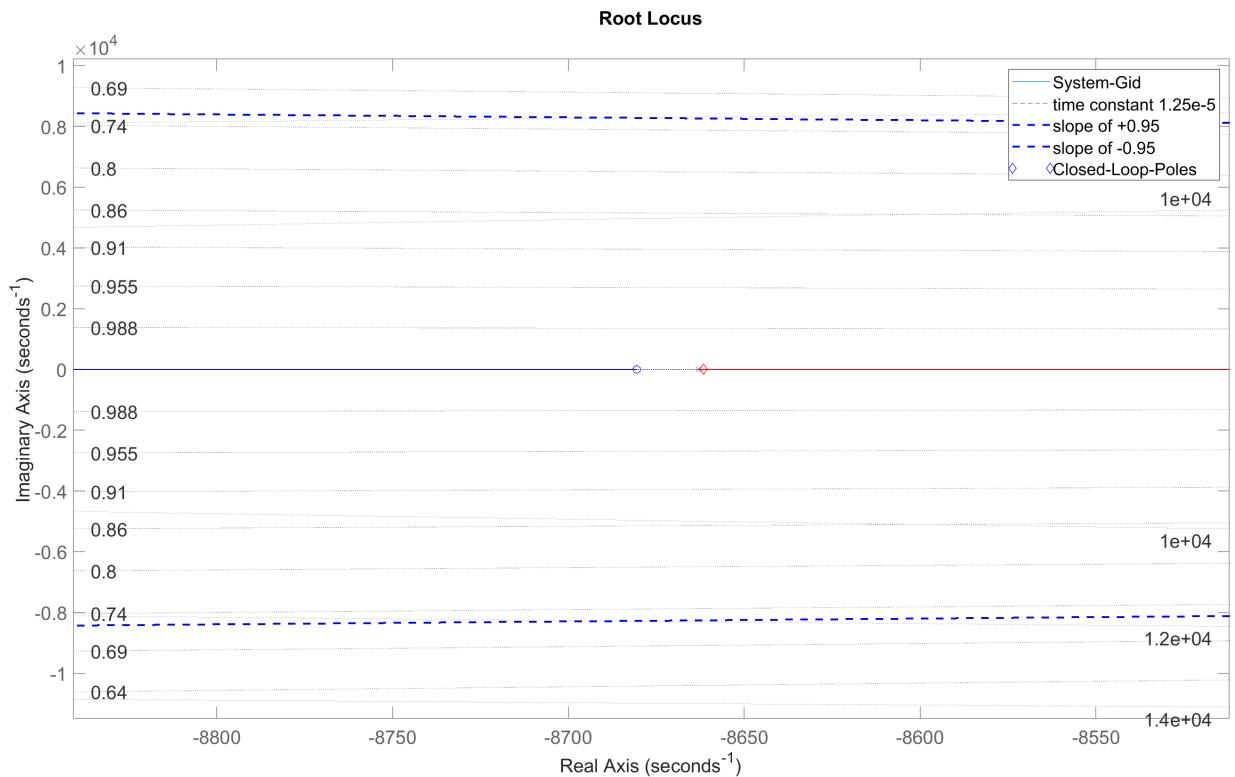
Figure 2.3: Root locus of $G_{id}(s)$

The yellow region corresponds the feasible region, which is constrained by the system damping and time constant. Here we choose a suitable $K_{p,i} = 0.37$ and $K_{i,i} = 4e4$.

According to the Figures fig. 2.3 and fig. 2.4 there are 3 poles:

$$\begin{cases} p_1 = -8.66e3 + j0 \\ p_2 = -1.27e5 + j0 \\ p_3 = -7.56e5 + j0 \end{cases} \quad (2.24)$$

with 2 zeros:

Figure 2.4: Root locus of $G_{id}(s)$ (zoom in)

$$\begin{cases} z_1 = -8.68e3 + j0 \\ z_2 = -1.08e5 + j0 \end{cases} \quad (2.25)$$

In this case, p_1 and z_1 can be regarded together as a 'Dipole' therefore their effect towards the whole system can be ignored. Considering that p_3 is at least 6 times bigger than p_2 , and p_2 locates in the feasible region so that it can be the 'Dominant Pole', and be used to estimate and evaluate the system's performance.

2.3.2 Controller $G_v(s)$ of Voltage Loop

Considering that there is a positive zero in the transfer function $G_{vi}(s)$, which makes the system a non-minimum phase system:

$$G_{vi}(s) = \frac{\widetilde{v_o}(s)}{\widetilde{i_l}(s)} = \frac{-L \cdot s + RD'^2}{D'(CR \cdot s + 2)} \quad (2.26)$$

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The non-minimum phase system means, the system has a response in the opposite direction to the given input at the initial moment. In meanwhile the existance of such a positive zero makes it harder to design a suitable controller.

One effective method is with the expanded pure delay link $e^{-\tau s}$ using the 'Padé Approximant' [8]:

$$e^{-\tau s} = \frac{1 - 0.5\tau s}{1 + 0.5\tau s} \quad (2.27)$$

Hence here the voltage transfer function can be replaced as:

$$G_{vi}(s) \approx G'_{vi}(s) = \frac{RD'^2 + L \cdot s}{D'(CR \cdot s + 2)} e^{-\frac{2L}{RD'^2}s} \quad (2.28)$$

Here the bandwidth should be smaller than 1/5 of current loop, which is around 16 kHz, with $t_r = \frac{2.2}{w_{BW}} = 0.14ms$. And in case of a voltage controller with a speed slower than 1.55 ms, this delay could be ignored. Hence we configurate a PI voltage controller using root locus method. In conclusion, given a critical line of $x = -\frac{2.2}{1.5ms} = 1420$.

With similar process using root locus, we get $K_{p,v} = 0.43$ and $K_{i,v} = 1.5e3$.

In such configuration, the root locus of this system shows in fig. 2.5.

Accoring to the Figure, the poles in the closed loop system is:

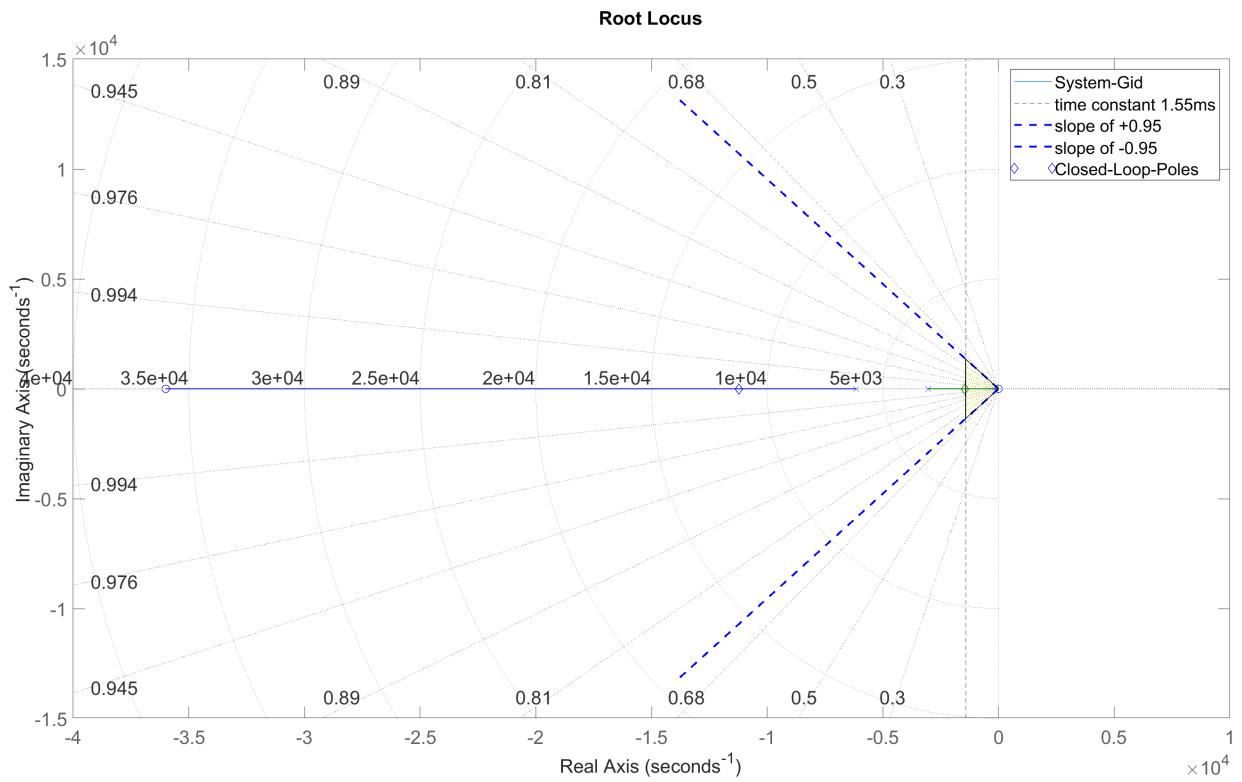
$$\begin{cases} p_1 = -1.12e4 + j0 \\ p_2 = -1.45e3 + j0 \end{cases} \quad (2.29)$$

Considering that p_1 is around 10 times more than p_2 , and p_2 also locates in the feasible region, regarding it as the dominant pole.

2.3.3 Stability Analysis of System with respect to R

The stability analysis with respect to R using root locus as analytical tool could be more challenging than before, because for both transfer functions $G_{di}(s)$ and $G_{vi}(s)$, R exists in both the numerator and the denominator. So here there is no mathematical analysis with specific formula, only a numerical approach.

R is here changed from 3.84Ω to 5760Ω ,corresponding to the 0.1% - 150% of the max power $P_{max} = 400 W$, far from the rated working point with respect to $R = 32.9 \Omega$, the root locus of

Figure 2.5: Root locus of $G_{vi}(s)$

current loop and voltage loop are shown respectively in fig. 2.6 and fig. 2.7.

According to both figures fig. 2.6 and fig. 2.7, in the range that the load changes, the system always keep stable. However with the increment of Load, the speed of the system, especially the voltage loop, will decrease.

2 Modeling and Simulation of the Boost Converter

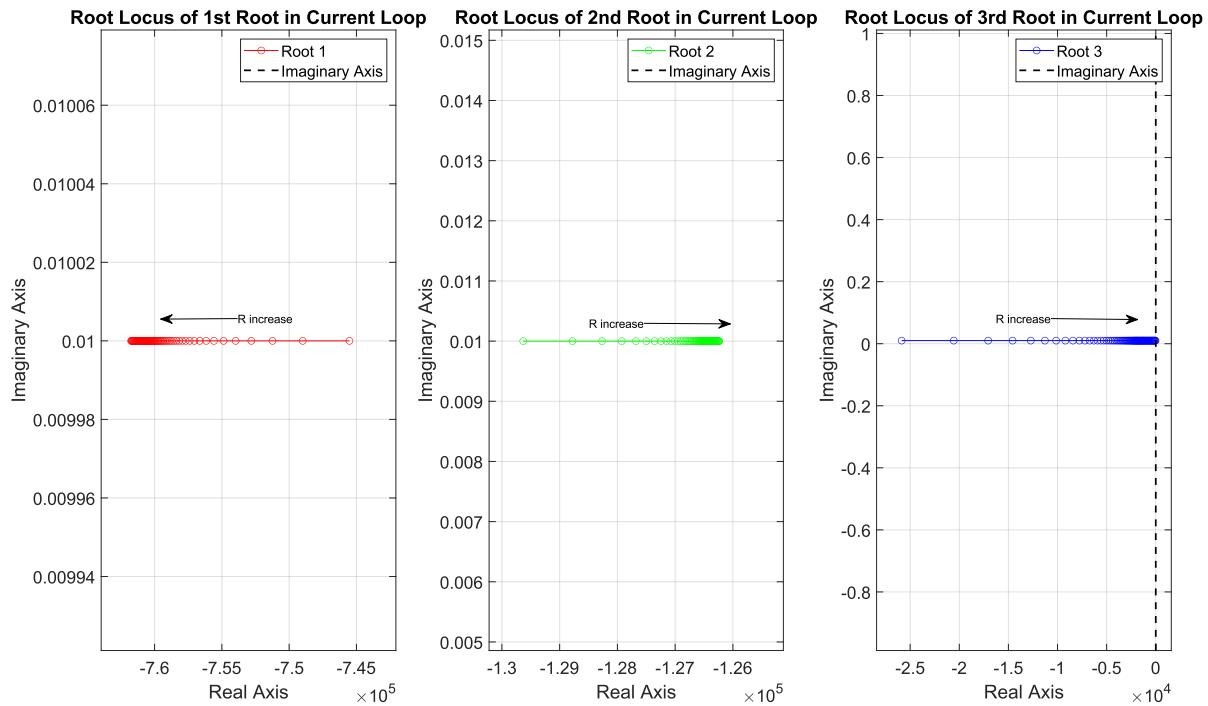


Figure 2.6: Stability of G_{id} based on R

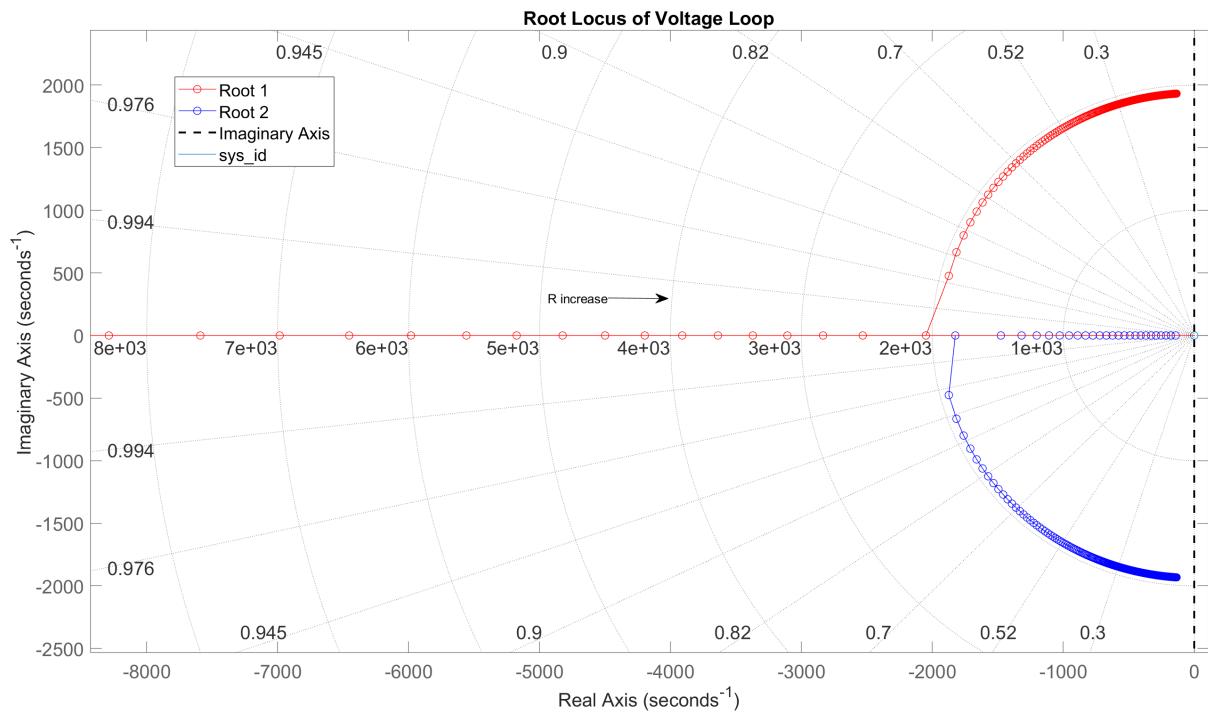


Figure 2.7: Stability of G_{vi} based on R

3 Modulation and Simulation of the H-Bridge Amplifier

The design of the H-Bridge is also an essential part of this thesis, because the overall system performance is dependent on the boost converter and the H-Bridge. The input filter and intermediate capacitor groups are similarly implemented next to the port of input voltage, based on electrical design criteria described in the previous chapter. Given the H-bridge amplifier is a PWM driven topology, first consideration is to determine the PWM modulation strategy.

3.1 PWM Modulation Strategy

3.1.1 Conventional Modulation

Conventional PWM modulation with freewheeling normally uses 2 groups of triangle wave to make a subtract from the given signal, facing a H-bridge structure with 2 half bridges. The schematic of it is shown in fig. 3.1.

In the meantime in order to balance the load across each transistor and ensure similar on-time and off-time durations, it's necessary to distribute the conducting time of each transistor, which is listed in table 3.1.

Table 3.1: Conventional switching logic

U_{st}	PWM upper (U)	PWM lower (L)	T1	T2	T3	T4
1	0	1	1	0	1	0
1	1	1	1	0	0	1
0	0	0	0	1	1	0
0	0	1	0	1	0	1
		Total	2	2	2	2

Here 1 corresponds to positive or conducting, 0 corresponds to negative or OFF. According to the sheet given above, we can summarize the logic formula of each switch with respect to eq. (3.1).

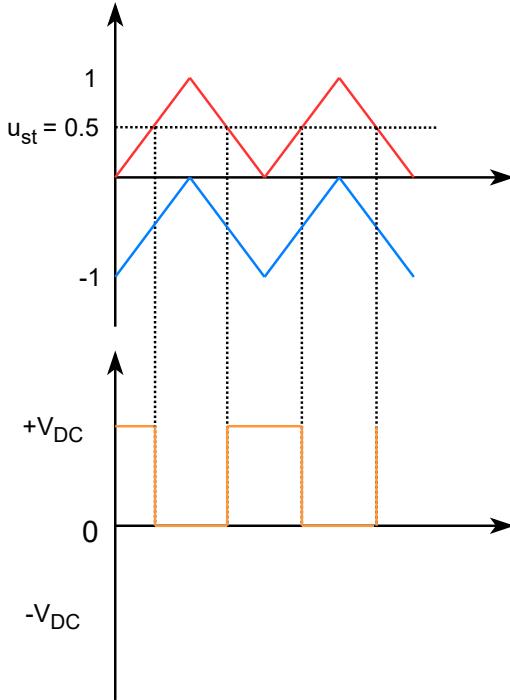


Figure 3.1: Conventional PWM modulation

$$T_1 = u_{st} = \overline{T_2} \quad (3.1)$$

$$T_3 = \overline{U}(u_{st} \odot L) = \overline{T_4}$$

3.1.2 Single Phase Shift (SPS) Modulation

Single phase shift modulation is a powerful modulation technique for dual active bridge converters. It uses $D_1 = D_2 = 0.5$ (i.e. 2-level switched voltages), reducing the degrees of freedom to ϕ only. The switching logic of this modulation is shown in fig. 3.2.

The performance of each modulation scheme is evaluated in chapter simulation and chosen accordingly.

3.2 Design of LP Filter in the Output Stage

According to [2], the low pass (LP) filter in final stage can be designed with following features:

- firstly, a LC filter with a relatively narrow range

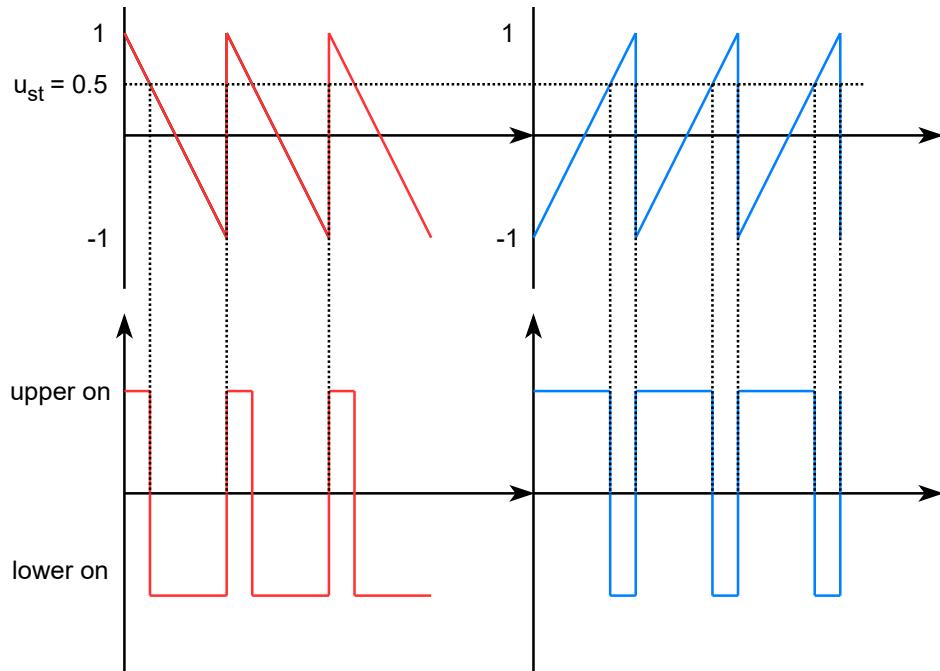


Figure 3.2: SPS modulation

- next to the first part, add a RC filter with a relatively wide range
- add an additional big resistor acting like a protector, to avoid too much current leading into the load

The schematic in the given document is showed in fig. 3.3. According to this figure, there is only one switching cell which corresponds to a single half bridge amplifier. Therefore for practical use, it should be modified with following steps, the modified version is showed in fig. 3.4:

- reference ground is replaced into the output from the other half bridge, which achieves now Dual Input and Dual Output
- replace the original L_1 into two inductors with half value than before but with smaller package which is better for printed circuit board (PCB) integration
- reserved space for two additional electrolytic capacitors C_3 and C_4 are for further adjustment in practical using, when performance is not satisfied

The theoretical cut off frequency at -3 dB here can be approximately calculated with following equation:

3 Modulation and Simulation of the H-Bridge Amplifier

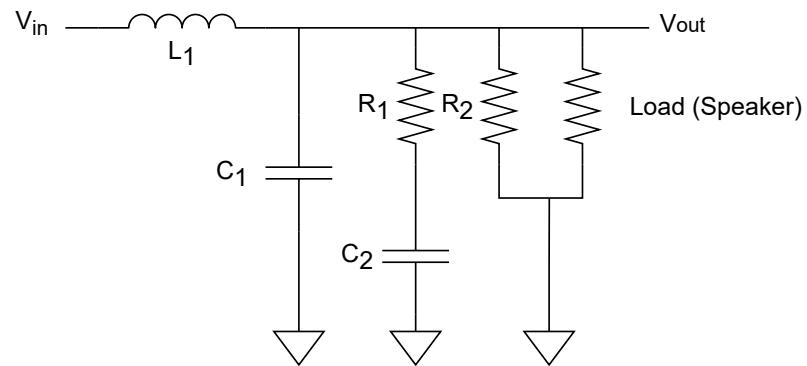


Figure 3.3: LP filter

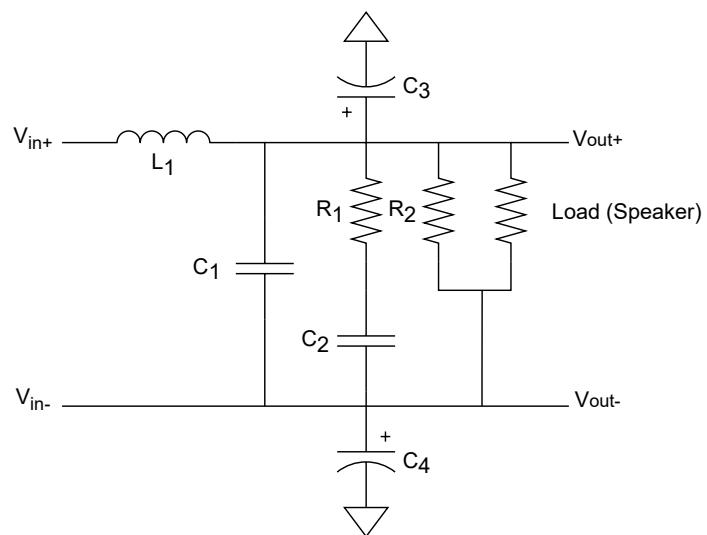


Figure 3.4: LP filter (modified)

3.2 Design of LP Filter in the Output Stage

$$\begin{aligned}f_{c,total} &= \min\{f_{c,LC}, f_{c,RC}\} \\&= \min\left\{\frac{1}{2\pi\sqrt{L_1C_1}}, \frac{1}{2\pi R_1 C_2}\right\}\end{aligned}\tag{3.2}$$

4 Analysis of Power Dissipation

4.1 Concept of power dissipation

With the development of Power Electronic technology, the switching frequency of semiconductor switches have been increased, which not only results in lower ripple and improved output performance, but also leads to higher power losses, especially the switching loss, accounting for a significant proportion of the total power dissipation. So, it is necessary for both calculation and simulation analysis of a system based on power electronic technology.

According to the statistical data [20], the proportions of various losses during the operation of the converter can be illustrated as shown in the fig. 4.1 below.

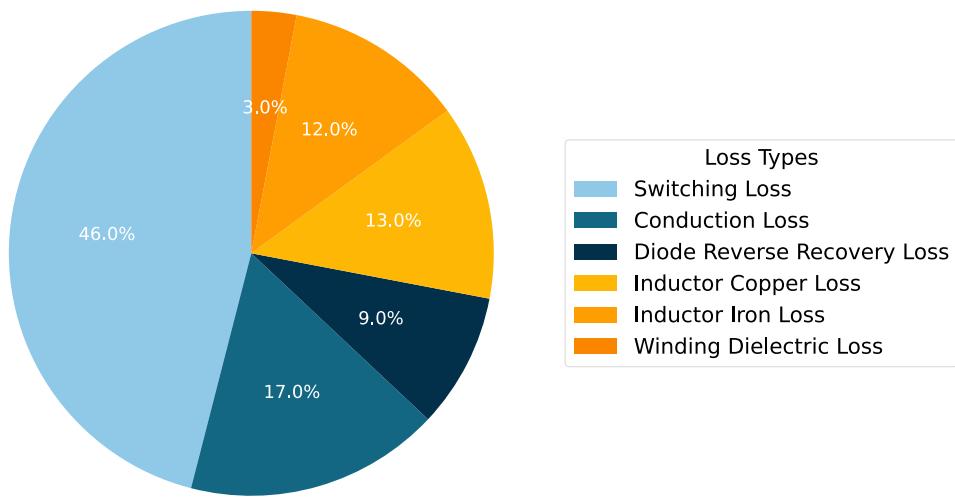


Figure 4.1: Loss distribution chart

These are the main parts of power loss, as to some other loss for example the loss from output capacitor can be neglected comparing with these types of loss. So the analytical calculation of power dissipation can be also divided into following parts:

- switching loss

4 Analysis of Power Dissipation

- conduction loss
- inductor loss caused by CSI

Because of the dead time optimization, the body diode equivalent to GaN transistors is not necessary, so only the loss caused by third quadrant, the conduction of GaN transistor will be considered instead of the loss of diode in reverse recovery.

4.2 Concept of Common Source Inductor (CSI)

CSI usually occupies a large proportion in the analytical calculation of power loss [19]. For a simple schematic of half bridge, fig. 4.2 shows the structure of CSI.

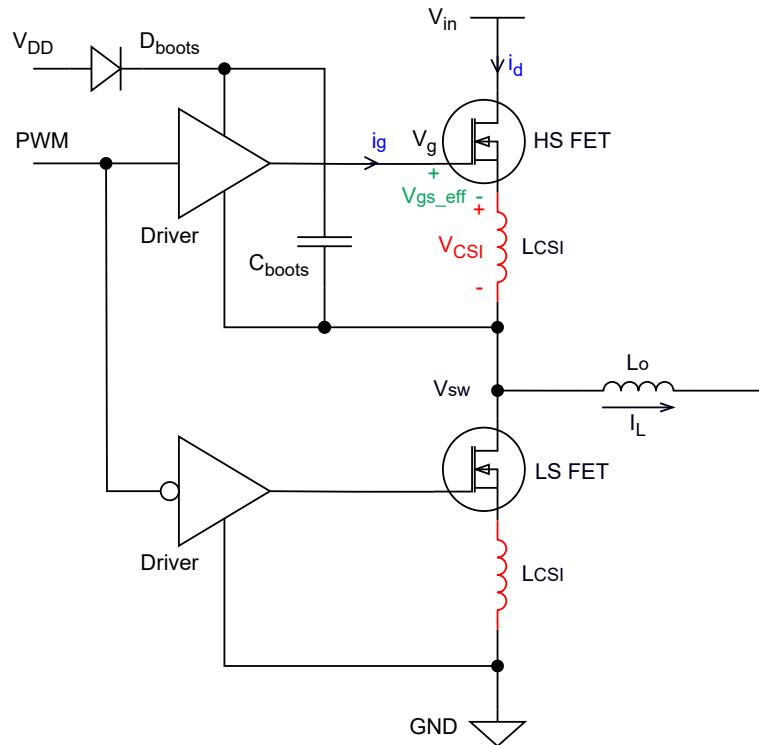


Figure 4.2: Schematic of CSI

This voltage V_{CSI} degenerates field-effect transistor (FET) V_{GS} and reduces switching speed, the effective gate source voltage V_{gs_eff} can be calculated by:

$$V_{gs_eff} = V_g - V_{sw} - V_{csi} \quad (4.1)$$

The standard working waveform of a high side (HS) FET without considering CSI is showed in fig. 4.3. After introducing the influence of CSI, as HS FET turn-on, the increasing drain current induces a positive voltage on L_{CSI} , which reduces the effective HS gate source voltage and slows

down the device turn-on. While HS turn-off, the decreasing drain current forces a negative voltage on L_{CSI} , which slows down the device turn-off. The extended switching time increases the switching power loss.

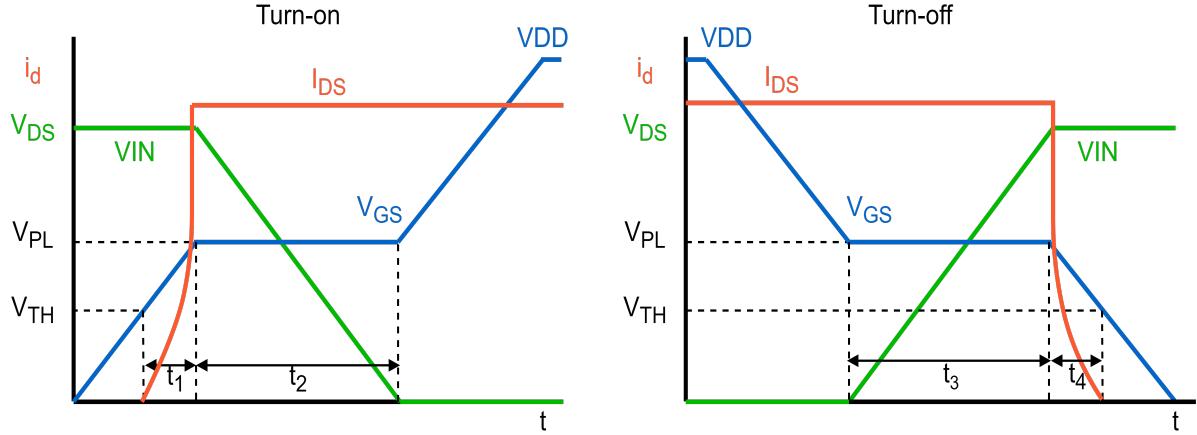


Figure 4.3: Waveform of working HS FET

4.3 Analytical Loss Calculation

According to [12], losses can be analyzed more accurately, with the additional influence of the common source inductance (CSI). The whole analytical process can be divided into following parts:

- Output Capacitance Losses P_{OSS}
- Gate Losses P_G
- 3rd Quadrant Conduction Losses P_{SD}
- Loss Analysis Accounting for Common Source Inductance
- Switching Losses P_{sw}
- Total Dynamic Losses $P_{Dynamic}$
- Conduction Losses $P_{Conduction}$
- Total Device Hard-Switching Losses P_{HS}
- Inductor Losses P_L
- Total Estimated Losses P_{Total}

4.3.1 Output Capacitance Losses P_{OSS}

From the *EPC2015* datasheet [5], the C_{OSS} as a function of drain-to-source voltage can be used to determine E_{OSS} as a function of drain-to-source voltage using following Equation.

$$E_{OSS} = \int_0^{V_{bus}} v_{DS} \cdot C_{OSS}(v_{DS}) \cdot dv_{DS} \quad (4.2)$$

C_{OSS} is a function of V_{DS} , can be found as a figure given in the datasheet.

4.3.2 Gate Losses P_G

The gate power now can be determined using following Equation. For both control switch and synchronous rectifier:

$$P_G = Q_G \cdot V_{DR} \cdot f_{sw} \quad (4.3)$$

4.3.3 3rd Quadrant Conduction Losses P_{SD} - Turn-Off Transient Conduction Losses

The Q_{OSS} for the converter is used to determine the effective dead-time.

$$t_{fall} = \frac{Q_{OSS}}{I_{off}} = \frac{2 \cdot Q_{OSS'}}{I_{off}} \quad (4.4)$$

It is extremely important to include the Q_{OSS} of both devices in Equation above. If both devices are the same, Q_{OSS} simply doubles. If both devices are not the same, each device's Q_{OSS} needs to be determined independently for the same voltage condition and added together, and the total Q_{OSS} is used to calculate the fall-time.

Having chosen effective dead-time, the diode conduction time will be:

$$t_{diode} = t_{dead} - t_{fall} \quad (4.5)$$

It is important to note that a negative result for t_{diode} would mean that the converter is operating in the partial zero voltage switching (ZVS) region, which should be avoided due to the high losses. Next, the voltage drop across the body diode needs to be determined. Again, the datasheet is referenced for the drain current value. This value should be similar to the plateau voltage in the case of an enhancement-mode GaN transistor only.

Now the turn-off reverse conduction losses can be calculated using following Equation:

$$P_{SD,off} = V_{SD} \cdot I_{turn-off} \cdot t_{diode} \cdot f_{sw} \quad (4.6)$$

4.3.4 3rd Quadrant Conduction Losses P_{SD} - Turn-On Transient Conduction Losses

Since this transition is forced-commutating, the Boost inductor current at the time of turn-on needs to be determined. In this case, the diode will conduct nearly instantaneously after the synchronous rectifier is turned off and will keep conducting until the control switch is turned on. This is due to the Boost Inductor's current keeping the diode in the conduction state. Thus, the diode conduction time is equal to the effective dead-time. Now the turn-on reverse conduction losses can be calculated using Equation:

$$P_{SD,on} = V_{SD} \cdot I_{turn-on} \cdot t_{dead} \cdot f_{sw} \quad (4.7)$$

4.3.5 Loss Analysis Accounting for Common Source Inductance

Ignoring the effect of CSI can lead to an artificially low loss prediction. Therefore, in this section, the switching losses will be recalculated to include the effect of CSI. By the very nature of CSI, it is impossible to measure without significant perturbation of the circuit.

CSI can be estimated using a commercial parametric extraction simulation program [22] that can compute the inductance from the layout and the device design. This would require knowledge of the internal design of the device that would seldom be made available. Alternatively, CSI can be estimated using circuit simulation software and using an ideal switch in the simulation. In the simulation, CSI can be added and waveforms compared with measured waveforms until enough correlation is found. For this calculation, a value of 110 pH will be used as a reasonable approximation.

To calculate R_{CSI} , the value of C_{GS} and transconductance (g_m) at the operating conditions are required. First, the transconductance can be determined using the small signal model for a MOSFET:

$$g_m = \frac{2 \cdot I_{DS}}{V_{pl} - V_{th}} \quad (4.8)$$

Then C_{GS} needs to be determined. This value can be derived from Q_{GS} , which yields a time equivalent capacitance, by reading off the values at the plateau voltage:

4 Analysis of Power Dissipation

$$C_{GS} = \frac{Q_{GS}}{V_{pl}} \quad (4.9)$$

The equivalent CSI impedance (R_{CSI}) was then calculated using Equation:

$$R_{CSI} = \frac{L_s \cdot g_m}{C_{GS}} \quad (4.10)$$

4.3.6 Switching Losses P_{sw} - Control Switch Dynamic Losses

The control switch experiences both hard turn-on and turn-off losses. Since all the components have already been determined, Following equations can be used to determine the switching power losses.

$$P_{on,cs} = \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw} \cdot R_{Gon}}{2} \cdot \left[\frac{Q_{GD}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}}{V_{DR} - \frac{V_{pl}+V_{th}}{2}} \right] \quad (4.11)$$

$$P_{off,cs} = \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw} \cdot R_{Goff}}{2} \cdot \left[\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{\frac{V_{pl}+V_{th}}{2}} \right] \quad (4.12)$$

In cases of considering also the influence of CSI:

$$P_{on,cs} = \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw}}{2} \cdot \left[\frac{Q_{GD} \cdot R_{Gon}}{V_{DR} - V_{pl}} + \frac{Q_{GS2} \cdot (R_{Gon} + R_{CSI})}{V_{DR} - \frac{V_{pl}+V_{th}}{2}} \right] \quad (4.13)$$

$$P_{off,cs} = \frac{V_{BUS} \cdot I_{DS} \cdot f_{sw}}{2} \cdot \left[\frac{Q_{GD} \cdot R_{Goff}}{V_{pl}} + \frac{Q_{GS2} \cdot (R_{Goff} + R_{CSI})}{\frac{V_{pl}+V_{th}}{2}} \right] \quad (4.14)$$

It should be pointed out, that here the Q_{GS2} is:

$$\begin{aligned} Q_{GS2} &= Q_{GS(op)} - Q_{GS1} \\ &= Q_{GS(op)} - \left(\frac{Q_{GS}}{V_{pl}} \right) \cdot V_{th} \end{aligned} \quad (4.15)$$

All relevant parameters can be found in corresponding datesheet of choosen GaN transistor.

4.3.7 Switching Losses P_{sw} - Synchronous Rectifier Dynamic Losses

The synchronous rectifier's switching losses are small because it only switches to and from a diode voltage drop, therefore, equations above it can be used to calculate the switching power losses

with V_{BUS} equated to V_{SD} .

$$P_{on,sr} = \frac{V_{SD} \cdot I_{DS} \cdot f_{sw} \cdot R_{Gon}}{2} \cdot \left[\frac{Q_{GD}}{V_{DR} - V_{pl}} + \frac{Q_{GS2}}{V_{DR} - \frac{V_{pl}+V_{th}}{2}} \right] \quad (4.16)$$

$$P_{off,sr} = \frac{V_{SD} \cdot I_{DS} \cdot f_{sw} \cdot R_{Goff}}{2} \cdot \left[\frac{Q_{GD}}{V_{pl}} + \frac{Q_{GS2}}{\frac{V_{pl}+V_{th}}{2}} \right] \quad (4.17)$$

In cases of considering also the influence of CSI:

$$P_{on,cs} = \frac{V_{SD} \cdot I_{DS} \cdot f_{sw}}{2} \cdot \left[\frac{Q_{GD} \cdot R_{Gon}}{V_{DR} - V_{pl}} + \frac{Q_{GS2} \cdot (R_{Gon} + R_{CSI})}{V_{DR} - \frac{V_{pl}+V_{th}}{2}} \right] \quad (4.18)$$

$$P_{off,cs} = \frac{V_{SD} \cdot I_{DS} \cdot f_{sw}}{2} \cdot \left[\frac{Q_{GD} \cdot R_{Goff}}{V_{pl}} + \frac{Q_{GS2} \cdot (R_{Goff} + R_{CSI})}{\frac{V_{pl}+V_{th}}{2}} \right] \quad (4.19)$$

4.3.8 Total Dynamic Losses $P_{Dynamic}$

Table 4.1: Loss breakdown of control switch and synchronous rectifier

Loss Characteristic (mW)	Control	Switch	Synchronous	Rectifier
	Turn-off	Turn-on	Turn-on	Turn-off
P_{oss}	0	P_{oss1}	P_{oss2}	0
P_G	$\frac{P_G}{2}$	$\frac{P_G}{2}$	$\frac{P_G}{2}$	$\frac{P_G}{2}$
P_{SD}	0	0	$P_{SD,on}$	$P_{SD,off}$
P_{RR}	0	0	0	0
P_{on}	N/A	$P_{on,cs}$	$P_{on,sr}$	N/A
P_{off}		N/A	N/A	$P_{off,sr}$
Total Power Loss		$\sum P_{cs}$		$\sum P_{sr}$

4.3.9 Conduction Losses $P_{Conduction}$

The conduction losses ($P_{Conduction}$) for the control switch can then be calculated using equation:

$$P_{Conduction,cs} = (I_{Load}^2 + I_{Ripple}^2/12) \cdot R_{DS(on)} \cdot D \quad (4.20)$$

and for the synchronous rectifier:

$$P_{Conduction,sr} = (I_{Load}^2 + I_{Ripple}^2/12) \cdot R_{DS(on)} \cdot (1 - D) \quad (4.21)$$

4.3.10 Total Device Hard-Switching Losses P_{HS}

$$P_{HS(cs/sr)} = P_{Dynamic(cs/sr)} + P_{Conduction(cs/sr)} \quad (4.22)$$

4.3.11 Inductor Losses P_L

The final loss component is the inductor loss (P_L). The difference between dc resistance (DCR) and ac resistance (ACR) cannot be neglected for switching frequencies in the multi-MHz region. The manufacturer also provides a core loss calculator on its website. Alternative methods can be used to determine core losses that include referencing the manufacturers' core losses as a function of flux density and frequency.

$$P_L = I_{Load}^2 \cdot DCR + \frac{I_{Ripple}^2}{12} \cdot ACR + P_{Core} \quad (4.23)$$

4.3.12 Total Estimated Losses P_{Total}

$$P_{total} = P_{HS,cs} + P_{HS,sr} + P_L \quad (4.24)$$

In the next chapter of simulation, all loss will be calculated according to their given parameters from datasheet of GaN transistor *EPC2361* [6], the chosen one of GaN transistor for our implementation and simulation.

4.4 Dead-Time Optimization

According to the fig. 4.1 and contents above, dead time can also greatly affect the power loss through influencing the body diode conduction loss, here for GaN transistor, namely the 3rd quadrant conduction loss, which takes around 10% of the total loss. On the other hand, compared with other kinds of switches like MOSFET which is made up with P-N junction, the GaN transistor is without P-N junction however with higher forward conduction voltage during 3rd quadrant conduction which means larger body diode conduction loss [16].

According to the eq. (4.5), the power loss from body diode conduction loss can be minimized with the constraints

$$t_{dead} = t_{fall} \quad (4.25)$$

In this case the turn-on body diode conduction loss can be eliminated, and the turn-off body diode conduction loss can be minimized.

4.5 Analytical Thermal Calculation

Since the vast majority of power loss will ultimately manifest in the form of heat, it's necessary to check whether the junction temperature of GaN transistor will exceed the specified limitation, under assumption that all power dissipation is converted into heat energy. At the same time assuming that there is a heat sink with given thermal resistance, to ensure the junction temperature of the GaN transistor always below the limitation.

The heat dissipation design is based on the thermal resistance network model, and the core formula is:

$$T_j = T_a + P_d \cdot (R_{\theta jc} + R_{\theta cs} + R_{\theta sa}) \quad (4.26)$$

Objective is to calculate the maximum allowable thermal resistance of the required heat sink:

$$R_{\theta sa} \leq \frac{T_j - T_a}{P_d} - (R_{\theta jc} + R_{\theta cs}) \quad (4.27)$$

The parameters are defined as follows:

- T_j : Device junction temperature (needs to be smaller than the maximum value in the specification, such as 120 °C for GaN)
- T_a : Ambient temperature (measured or estimated, such as 25 °C)
- P_d : Device heat generation power (unit: W)
- $R_{\theta jc}$: Thermal resistance from junction to case (provided in the device specification, such as 1.5 °C/W)
- $R_{\theta cs}$: Contact thermal resistance from case to heat sink (determined by the thermal conductive medium, such as silicone grease 0.2 °C/W)
- $R_{\theta sa}$: Thermal resistance from heat sink to environment (key heat sink parameter to be calculated)

If the calculated thermal resistance is too high, approaching that of direct connection to air, then there's no need to add an additional heatsink. This will be tested in the next chapter of simulation.

5 Simulation of Power Dissipation and Thermal Behaviour

In this chapter, the previously mentioned models will be validated. In order to better check the reliability of other simulations, the theoretical power loss should be firstly calculated. Matlab is implemented here as programming tool to calculate the corresponding detailed power loss according to eq. (4.1) to eq. (4.24), which appear in the previous chapter.

5.1 Analytical Calculation of Power Loss

Based on the performance metrics of the model from table 2.1 and the real parameters provided in the *EPC2361* datasheet, the power losses and system efficiency are calculated and presented in table 5.1.

Table 5.1: Feature and theoretical losses of the given transistor

Feature	
Figure of Merit (FOM)	2.800×10^{-12}
Loss in Boost Converter (W)	
Output Capacitance Losses	3.456
Gate Losses	0.224
Body Diode Conduction Losses	0.260
Switching Losses	2.135
Dynamic Losses	6.074
Conduction Losses	0.278
Inductor Losses	0.731
Total Loss	7.082
Efficiency	96.459%
Loss in H-Bridge (W)	
Gate Charge Loss	0.448
Switching Loss	9.756
Conducting Loss	0.126
Total Loss	10.331
Efficiency	94.835%

In practical situations, the efficiency of boost converter products available on the market is around 80% to 95%, for example TPS61288 from Texas Instrument [18], for some advanced improvements in lab also around 85% to 95% [1], so an calculated peak efficiency of around 95% is

5 Simulation of Power Dissipation and Thermal Behaviour

generally acceptable. Therefore, the theoretical power loss calculation presented above is considered reasonable.

With these given parameters, the eq. (4.27) can be here achieved with:

$$\begin{aligned} R_{\theta sa, Boost} &\leq 12 \text{ } C/W \\ R_{\theta sa, Bridge} &\leq 7.4 \text{ } C/W \end{aligned} \quad (5.1)$$

There are necessary constrains to maintain the transistor under operating under a safe temperature range. In practice a heat-sink with as small as possible thermal resistance should be used to ensure the safe operation.

5.2 Simulation of Boost Converter in PLECS

The theoretical design of a boost converter in the previous chapter should also be validated in simulation. PLECS (Piecewise Linear Electrical Circuit Simulation) is a simulation tool specifically designed for modeling and analyzing power electronic systems, and is widely used for its fast simulation speed and efficient handling of complex power converter topologies. The schematic of this model is illustrated in fig. 5.1, and the detailed schematic of controller is showed in fig. 5.2.

It is made up of several parts:

- Main circuit: consists of main components of a basic boost converter with synchronous rectifier
- Parasitic components: considering the equivalent series resistance (ESR) of both inductor and output capacitors
- Controller: dual closed-loop controller for both current (internal loop) and voltage loop (external loop)
- Measurements
- Disturbance: achieve a load fluctuation of 30% of the rated power

According to the given parameter from table 2.1 and the theoretically calculated parameters of the controller, the complete initialization parameters are presented in table 5.2

A simulation is carried out where the load fluctuates at times t_1 and t_2 , simulating a step disturbance of 30% of the rated power. As a result, the output power during the intervals $0-t_1$, t_1-t_2 , and t_2-t_{end} is 70% (140 W), 100% (200 W), and 70% (140 W), respectively. The results are illustrated in fig. 5.3.

5.2 Simulation of Boost Converter in PLECS

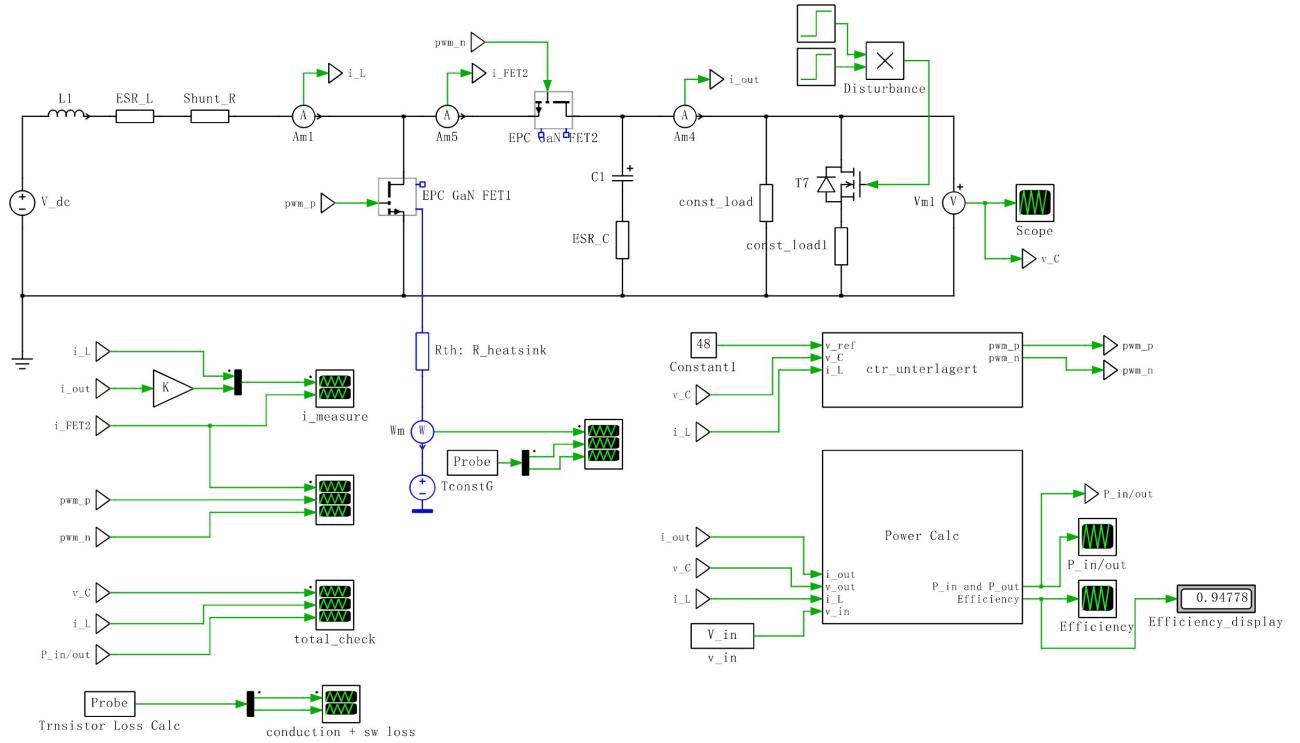


Figure 5.1: Schematic of boost converter in PLECS

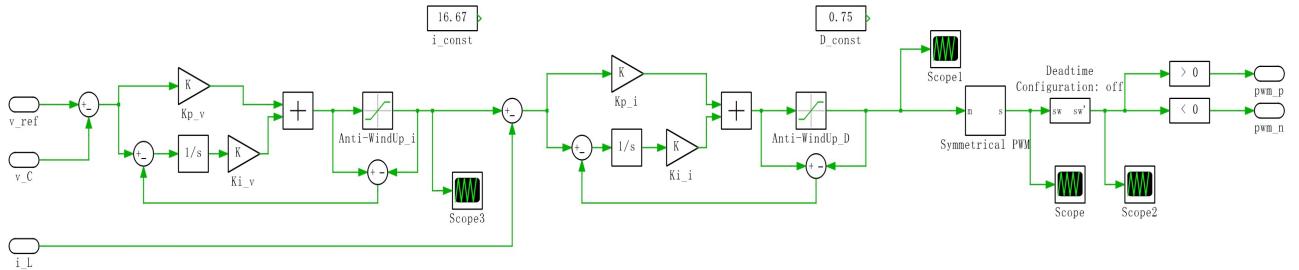


Figure 5.2: Schematic of controller in PLECS

It can be found that during the steady-state load conditions, the controller maintains the output voltage at 48 V with an error of approximately 0.02%. During the 30% rated load fluctuation, the output voltage exhibits an 8% deviation with a recovery time of 1.6 ms. According to common industry standards [4], this dynamic range is considered acceptable.

In order to verify the reliability of the thermal management based on the implemented heat sinks, a thermal model should be firstly assigned to the GaN transistors. In power electronics and thermal system modeling, the Foster and Cauer models are two widely used approaches to represent the transient thermal behavior of components using equivalent electrical circuits. Both models rely on the thermal-electrical analogy, where:

- Temperature difference: Voltage

5 Simulation of Power Dissipation and Thermal Behaviour

Table 5.2: Simulation parameters of boost converter

Parameter	Value
Input and Power Stage	
Input Voltage V_{in}	12 V
Duty Cycle D	0.75
Main Inductance L_{main}	$22 \mu\text{H}$
Main Capacitance C_{main}	$20 \mu\text{F}$
Capacitor ESR ESR_C	$50 \text{ m}\Omega$
Inductor ESR ESR_L	$0.65 \text{ m}\Omega$
Parasitic Inductance	1 nH
Shunt Resistance	$0.4 \text{ m}\Omega$
Load Resistance R_{load}	11.52Ω
Dead Time t_d	10 ns
PWM Frequency f_{PWM}	0.8 MHz
Simulation Timing	
Max Simulation Time t_{max}	120 ms
Thermal	
Heatsink Thermal Resistance $R_{heatsink}$	$4.7^\circ\text{C}/\text{W}$
Controller Parameters	
Current Loop Gain $K_{p,i}$	0.37
Current Loop Integral Gain $K_{i,i}$	4×10^4
Voltage Loop Gain $K_{p,v}$	0.43
Voltage Loop Integral Gain $K_{i,v}$	1.5×10^3

- Heat flow: Current
- Thermal resistance: Electrical resistance
- Thermal capacitance: Electrical capacitance

In this simulation the thermal model of GaN transistors will be described by Foster model, this is a kind of an empirical model, derived from measured transient thermal impedance data, then represented as series of parallel RC branches, connected in cascade. The schematic of the Foster model is illustrated in fig. 5.4.

The equivalent thermal impedance of Foster model can be expressed as eq. (5.2):

$$Z_{th}(t) = \sum_{i=1}^n R_{ti} \cdot (1 - e^{-\frac{t}{R_{ti}C_{ti}}}) \quad (5.2)$$

The parameters of each components in Foster model are given according to the datasheet of implemented GaN transistor.

Run simulation once again based on this given thermal model, with thermal resistance of the heat sink $R_{\theta sa} = 4.7^\circ\text{C}/\text{W}$, the result is illustrated in fig. 5.5.

According to the temperature record, the junction temperature of the control switch eventually settles at 65°C . Since many parasitic components are neglected, the result is more linear than what it supposed to be. So the body diode conduction of synchronous rectifier can also be ignored

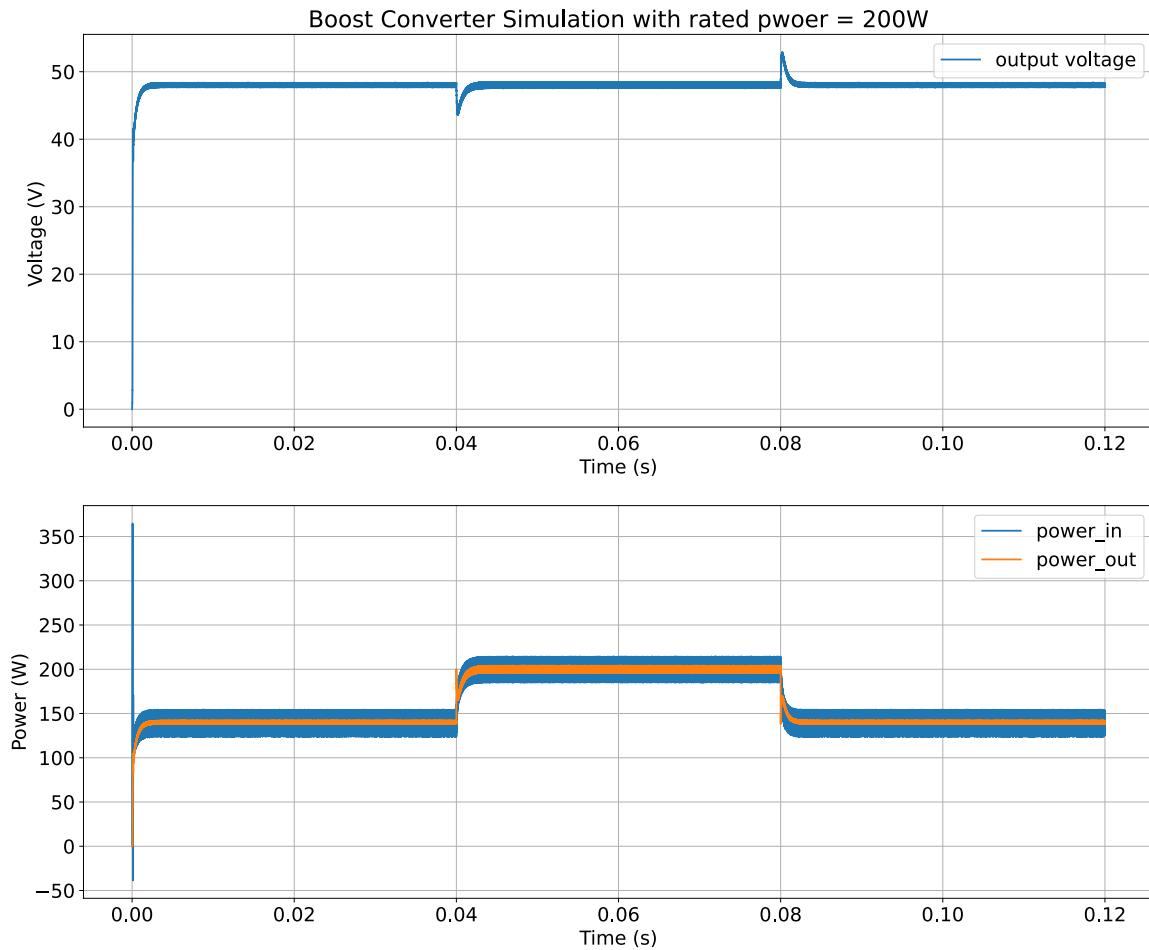


Figure 5.3: Scope of output voltage

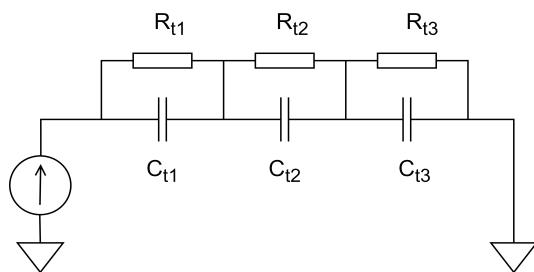


Figure 5.4: Schematic of foster thermal model

and the FET thermal simulation of both transistors can be assumed to be symmetric. The loss by body diode conduction of synchronous rectifier will be measured in chapter of implementation based on real PCB.

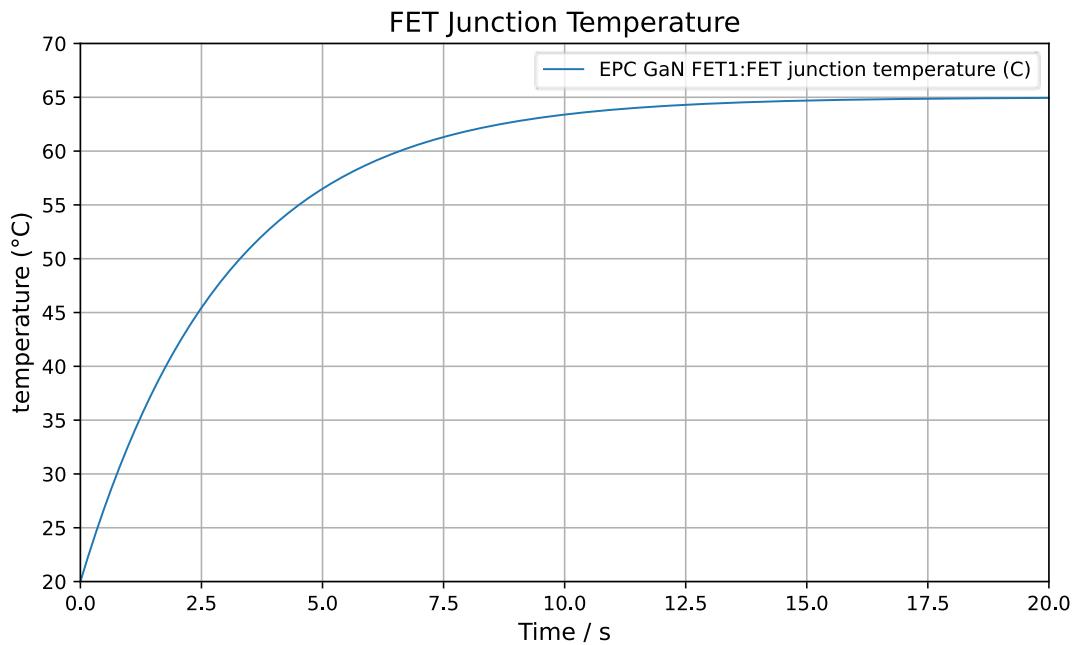


Figure 5.5: Thermal simulation of FET's junction

5.3 Simulation of LP filter at output stage in LTSpice

The topology of the LP filter is already discussed in the chapter of H Bridge in previous chapter in fig. 3.3 and fig. 3.4. To ensure that their cutoff frequency and performance match the theoretical design and numerical solutions, further validated in LTSpice, the schematic is shown in fig. 5.6.

The functionality of this simulation is to sweep the frequency from 20 Hz to 50 kHz, which contains the audio range of the human ear from 20 Hz to 20 kHz. The results of both structures, with or without 2 additional electrolytical capacitors, are respectively shown in fig. 5.7 and fig. 5.8.

According to the result of simulation shown in fig. 5.7 and fig. 5.8, the cutoff frequency of the case without additional capacitors is around 25 kHz, higher than the required max. audio frequency of 20 kHz, in contrast the other one with 2 additional $66\ \mu\text{F}$ is around 7 kHz, with a resonant peak and steeper frequency drop after the cut off frequency. It means the introduction of 2 additional capacitors can decrease the cut off frequency of the whole LP filter system, which can be in practical situation flexibly changed in order to get a better performance.

5.4 Simulation of H Bridge Amplifier in LTSpice

The schematic of H-Bridge Amplifier's simulation in LTSpice is shown in the following 5.9. According to this figure, it is divided into several sub blocks:

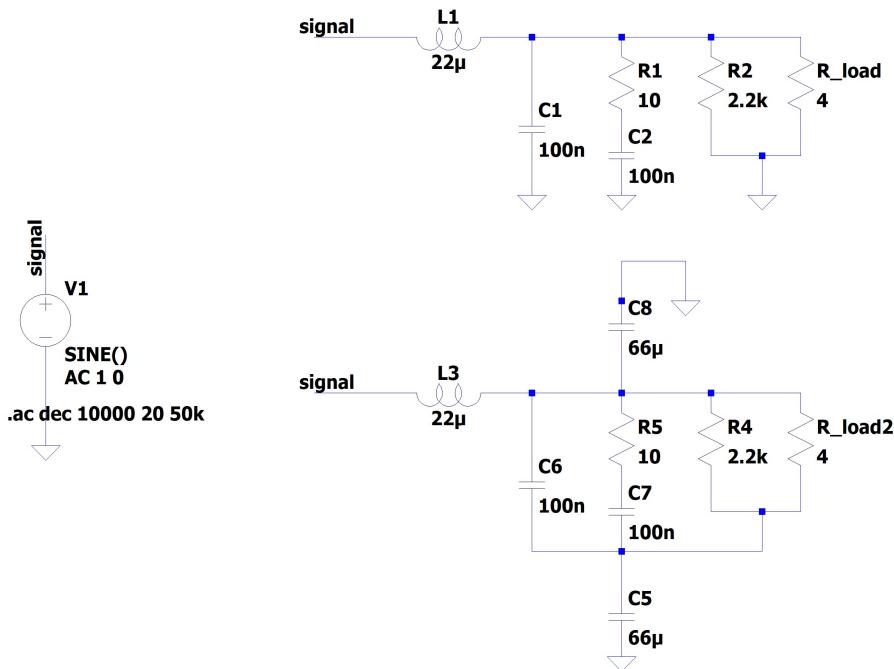


Figure 5.6: Schematic of LP filter in LTSpice

- PWM signal generator: generate PWM signal for 2 complemented transistor groups based on given reference sinus signal from 20 Hz to 20 kHz continuously comparing with high-frequency triangular wave
- Dead time generator: generate a 10 ns dead time signal between each upper and lower arm of H Bridge, which equals to the optimized dead time
- gate driver: ideal gate driver with both turn-on and turn-off resistor
- full H Bridge: H bridge plus designed LP filter on output stage

5.4.1 Gate Resistor Optimization

In order to implement the optimized gate resistor for the desired GaN transistor EPC2361 to obtain the best performance. The subtest schematic is shown below. To simulate the real situation to the maximum extent, real component' model of EPC2361 is here implemented, in the meanwhile the gate driver will use -1 V and 5 V for respectively turn off and turn on, to avoid False Turn On from ringing effect.

Try different combinations of gate resistors, measure the power loss crossing the transistor, then plot the result in fig. 5.11.

According to fig. 5.11, the optimized gate resistor based on a ideal in current topology is around: $R_{on} = 11 \Omega$, $R_{off} = 0.15 \Omega$. This conclusion will be applied in simulation in order to keep the

5 Simulation of Power Dissipation and Thermal Behaviour

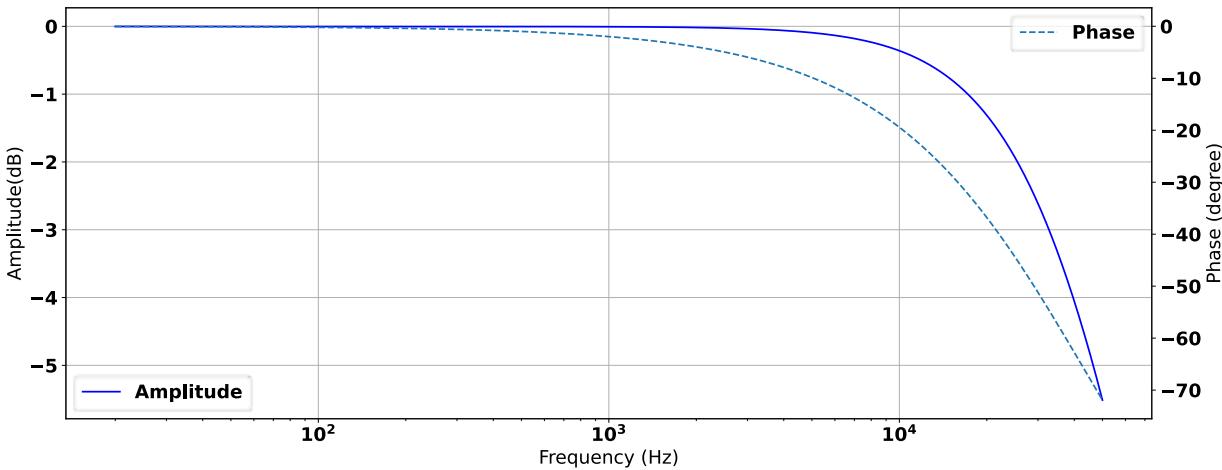


Figure 5.7: Bode diagram of LP filter without additional capacitors

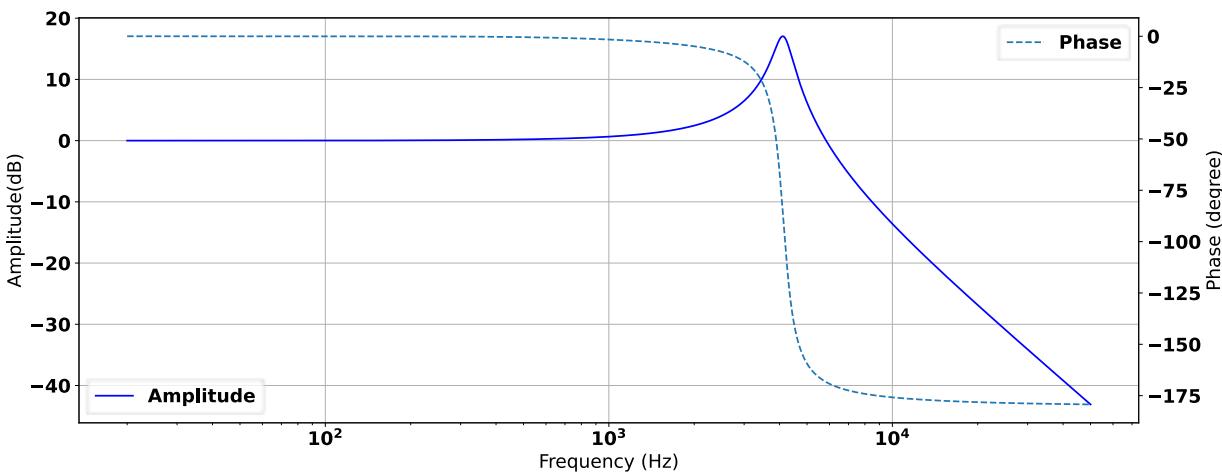


Figure 5.8: Bode diagram of LP filter with 66 μF capacitors

power loss minimal. However it is very clear that this topology neglects the parasitic components which exist definitely in real circuits. So normally the optimized gate resistor in real circuit is higher than this application to compensate the ringing effect caused by the parasitic capacitive components.

5.4.2 Wave generation and THD analysis

In fig. 5.12 and fig. 5.13, the simulation with given input as 200 Hz and 20 kHz are shown here as an example. The result between both modulation according to fig. 3.2 and fig. 3.1 are acceptable and seems there are no obvious difference with each other.

Furthermore to quantitatively analyse the output performance, THD could be a powerful tool.

The basic idea of THD is to calculate the sum of all the harmonics measured in output. A THD measurement sums all the distortion products by adding up the extra harmonic energy into a single value, expressed as either a percentage or as unit of dB, representing the proportion of the energy compared to the fundamental or desired signal. Here the THD will be represented as form of percentage. The formula of THD is:

$$THD = \frac{\sqrt{U_{f1}^2 + U_{f2}^2 + \dots + U_{fn}^2}}{U_{f1}} \quad (5.3)$$

Considering the sampling rate cannot reach to infinitely high, in the meanwhile in order to decrease the computational complexity, normally only harmonics up to 9 times the base frequency are taken into consideration.

Two modulation strategies according to fig. 3.2 and fig. 3.1 will be tested to compare their performance in terms of THD from 1 kHz to 20 kHz, totally 20 test frequency groups, each with the number of periods equals to 5 and $f_{PWM} = 1 \text{ MHz}$.

LTSpice provides a THD Analysis. However this process really takes a long time especially facing some low frequency signal while f_{PWM} is too high. A useful solution raised by this thesis is to take full advantage of personal computer (PC) and use the multi-processing simulation. It can take use of multiple cores in central processing unit (CPU) and all simulations in different test condition can be driven at the same time. The program's block diagram and simulation's result are respectively shown below in fig. 5.14 and fig. 5.15.

According to fig. 5.15, the performance of shifted phase Modulation is obviously better than the conventional modulation, especially at low frequency. In order to match the standard of THD equals to 0.1%, which ensures minimal distortion and maintains the purity of sound [15], shifted phase Modulation is chosen in practical implementation.

5 Simulation of Power Dissipation and Thermal Behaviour

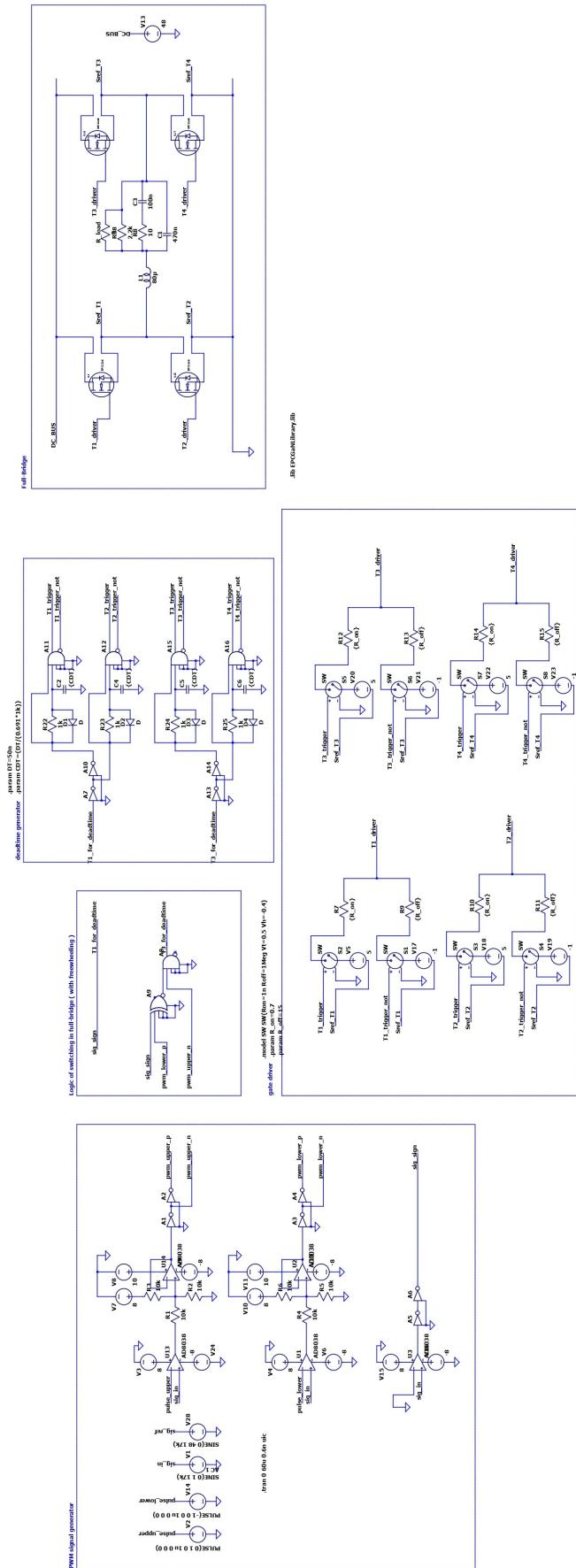


Figure 5.9: Schematic of H-Bridge in LTSpice

5.4 Simulation of H Bridge Amplifier in LTSpice

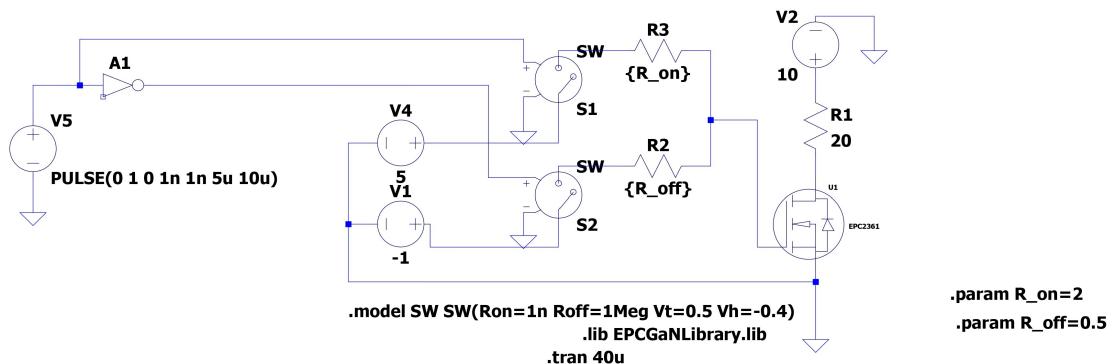


Figure 5.10: Schematic of gate resistor optimization

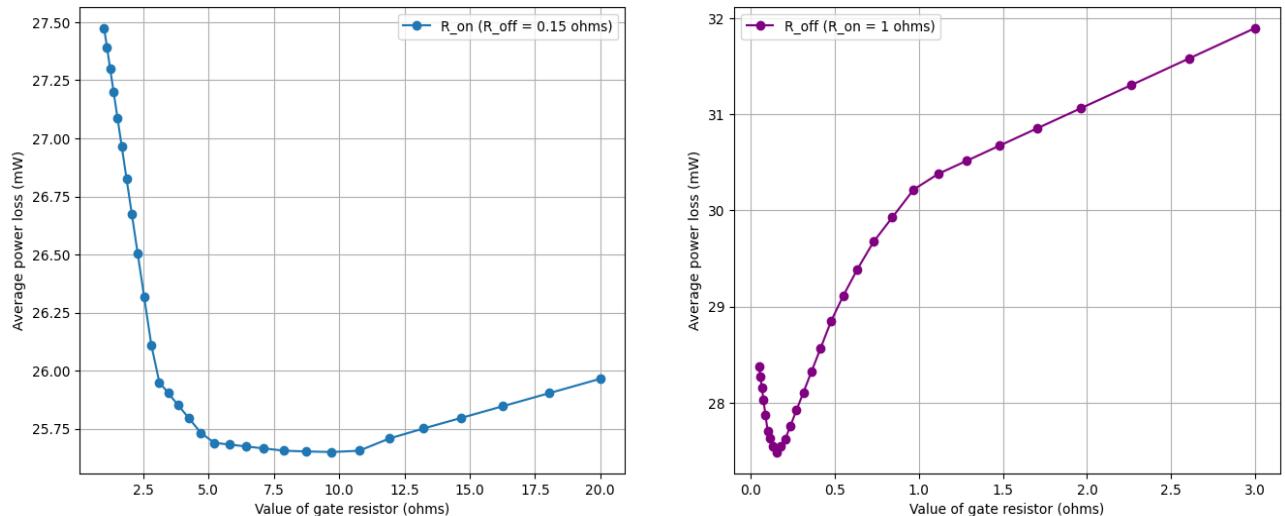


Figure 5.11: Power loss for different combinations of gate resistor

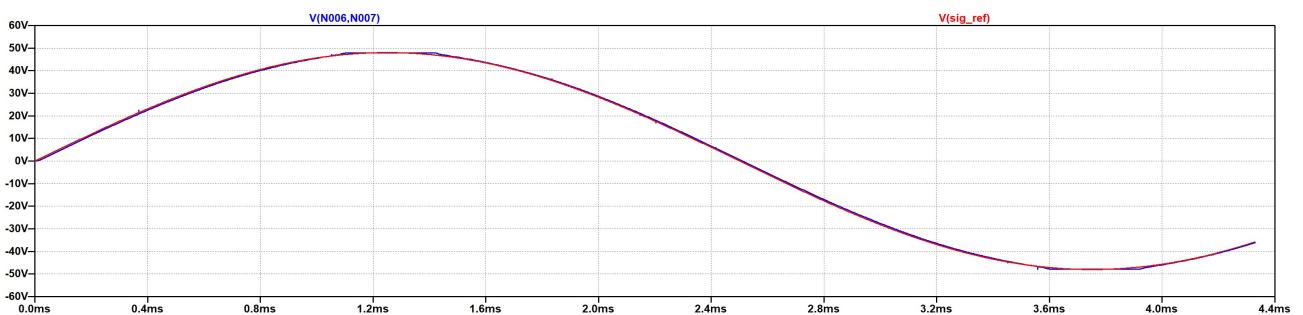


Figure 5.12: 200 Hz simulation of H amplifier

5 Simulation of Power Dissipation and Thermal Behaviour

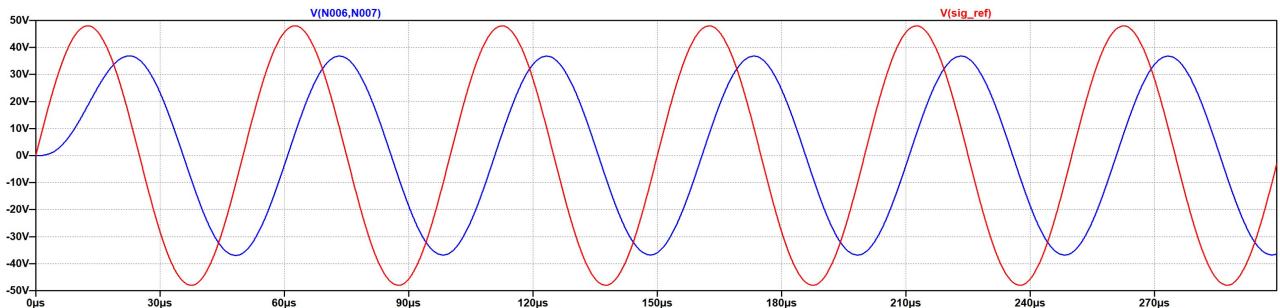


Figure 5.13: 20 kHz simulation of H amplifier

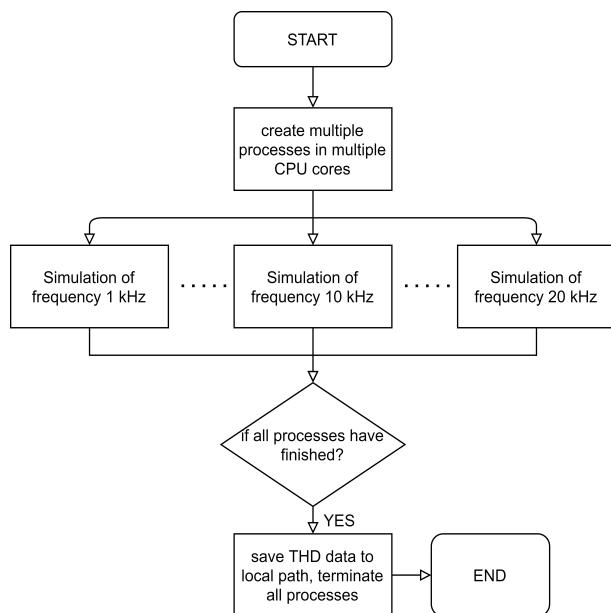


Figure 5.14: Block diagram of multi-processing THD simulation

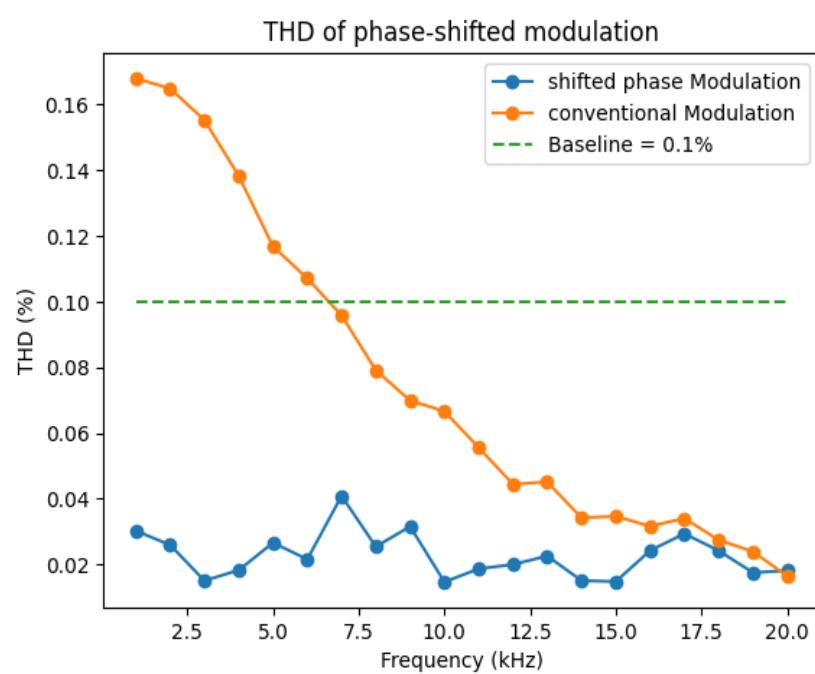


Figure 5.15: THD analysis of both modulation strategy

6 Implementation

6.1 Hardware Development

Based on fig. 1.10 in previous chapter, the hardware of this project will be divided into 3 sub-parts:

- PCB Main: on duty for audio signal preprocessing, function switch, 5 V power supply, connecting to the micro controller;
- PCB BOOST: contains physical signal acquisiter, Boost converter and relevant drivers.
- PCB Amplifier: contains H-Bridge amplifier and relevant drivers.

These three parts are designed in a modular manner, in order to test each sub-block individually. At the same time isolate the high power module (Boost Converter and H bridge amplifier) and low power module (central microcontroller and some preprocessing circuits) to ensure the safe operation of the whole system. The complete component list is shown in table .1 in appendix, and the details of each PCB will be discussed in following subsections. The 3D structure diagram of the whole project is shown in fig. 6.1 as a reference.

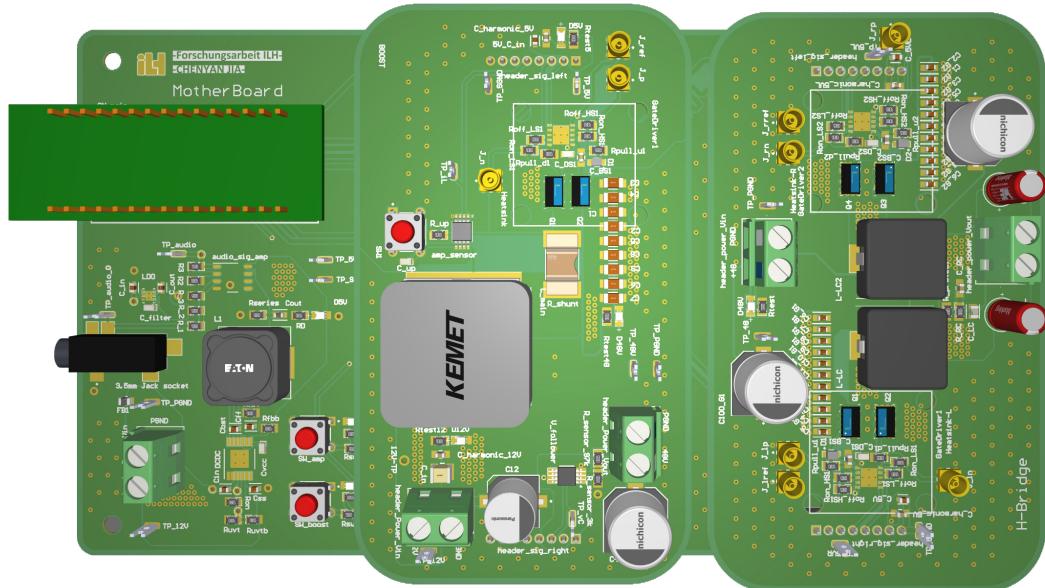


Figure 6.1: 3D structure diagram

6 Implementation

6.1.1 Sub-Board: Mother Board

The schematic and corresponding PCB Layout of mother board are shown respectively in fig. 6.2 and fig. 6.3.

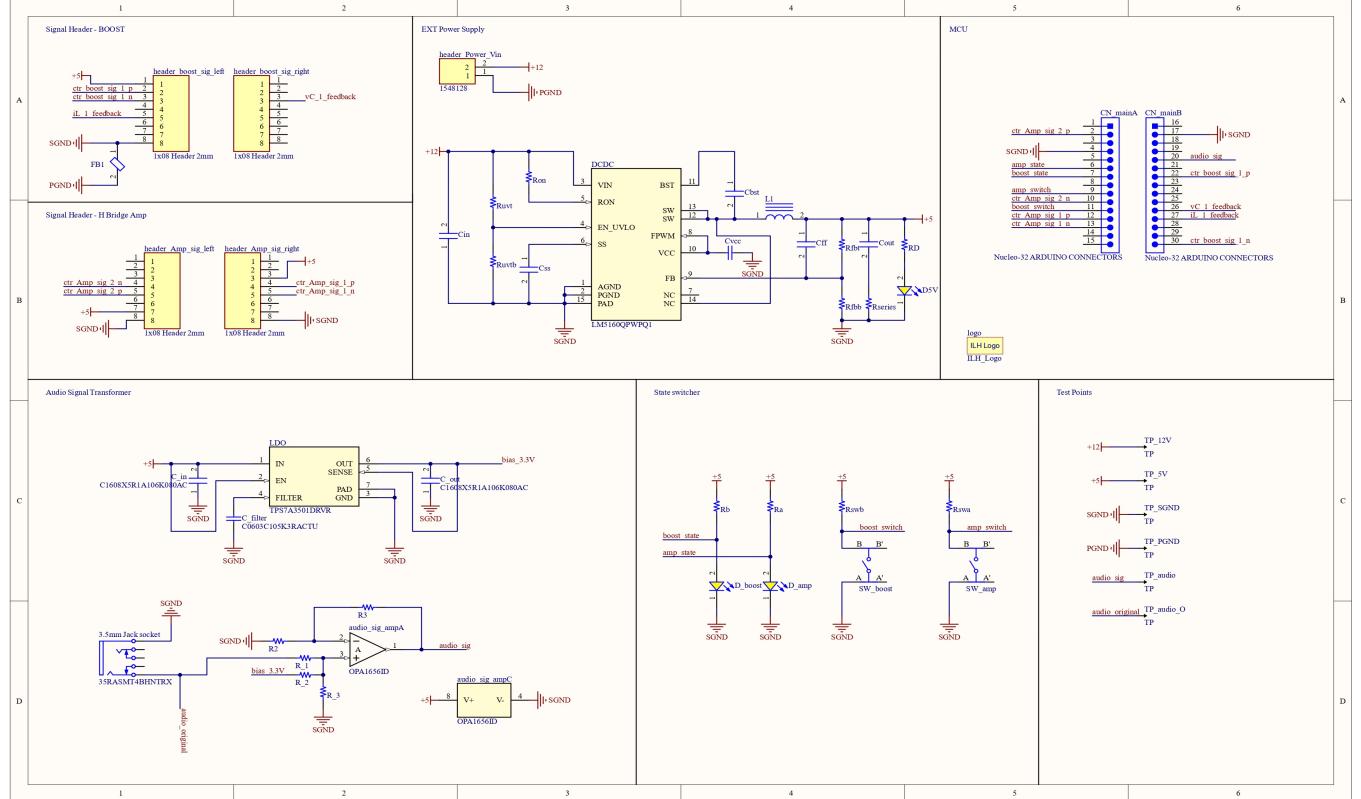


Figure 6.2: Schematic of mother board

The main board is designed as a 4 layer board, which from top to bottom are signal layer, 5 V power supply layer, signal ground layer and signal layer. Besides headers, test points , power supply check, switches and microcontroller, it contains two additional functional modules: 12 V to 5 V DCDC module and audio pre-processing module. It contains STM32G4 Nucleo-32 board as the controller platform and some other components according to table .1 for other functionalities.

Considering the input audio signal is AC signal, and that in microcontroller embedded analog-to-digital converter (ADC) is only capable for positive signal, this audio preprocessing operation is therefore necessary. The functional schematic of it is shown in fig. 6.4. Because the audio signal range is from -3.3 V to 3.3 V , so a LDO is applied to provide a 3.3 V bias, and a OPAMP is configurated as in fig. 6.5 to provide a fixed ratio to ensure the input signal is in the available range of ADC.

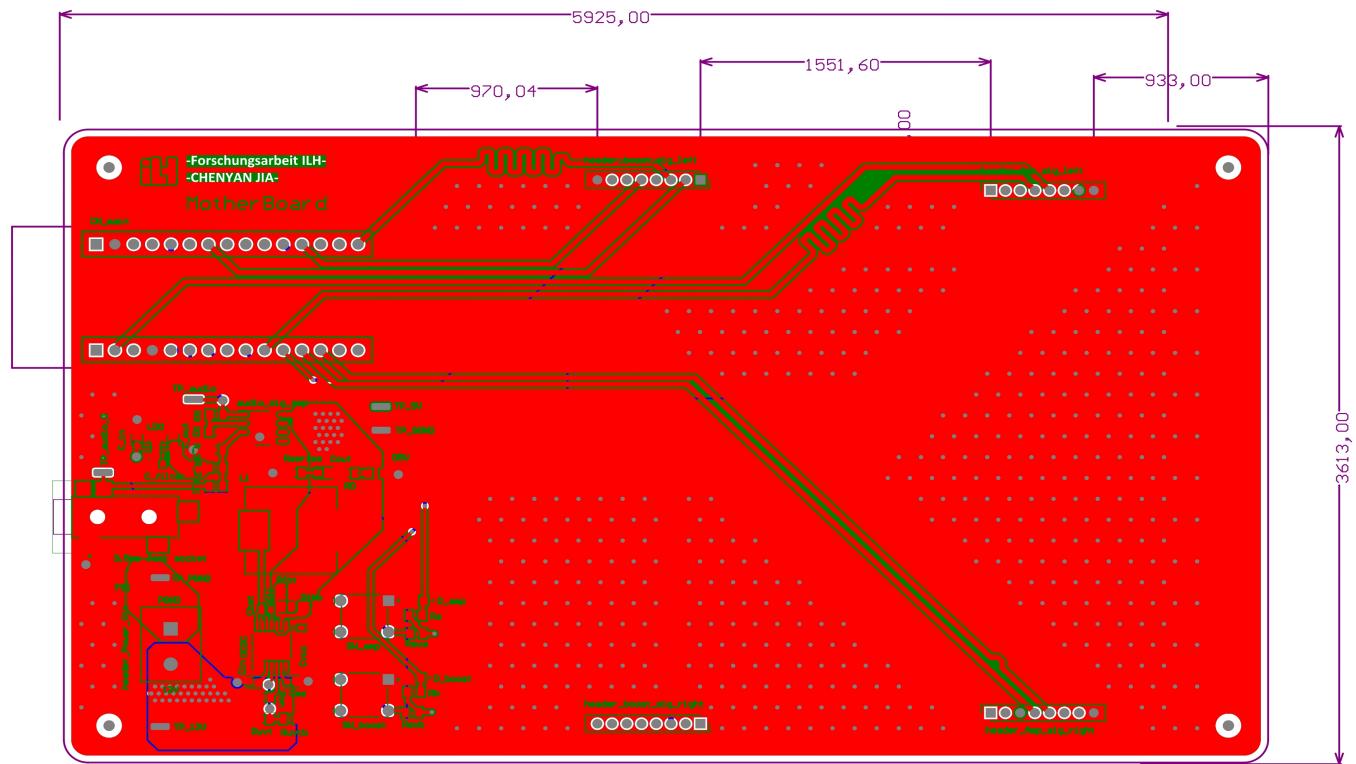


Figure 6.3: PCB Layout of mother board

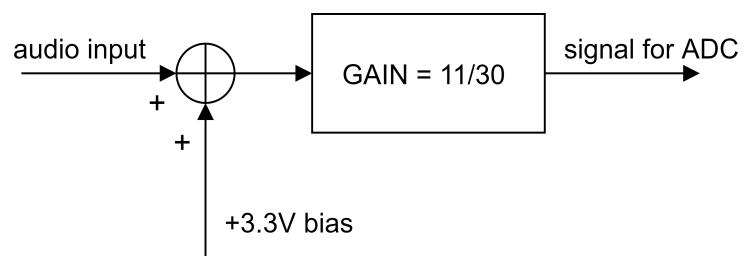


Figure 6.4: Functional schematic of audio pre-processing module

According to the fig. 6.5, the transformed audio signal equals to:

$$V_{out} = \frac{(V_{in} + V_{bias})(R_2 + R_3))}{3R_2} = (V_{in} + V_{bias}) \cdot \frac{11}{30} \quad (6.1)$$

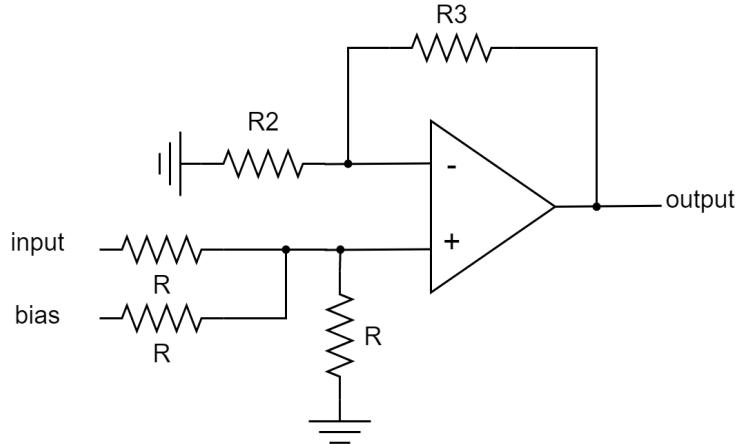


Figure 6.5: Topology of audio OPAMP

with the precondition:

$$R = R_2 = 10 \cdot R_3 \quad (6.2)$$

So that the range of the input signal will be transformed from $(-3.3V, 3.3V)$ to $(0.476V, 1.944V)$, which match the available input range of ADC limited in 2.048 V.

6.1.2 Sub-Board: Boost Converter

The PCB of boost converter is designed also as a 4 layer structure, which from top to bottom are signal layer, power ground layer, power signal layer and signal layer. The schematic (including external driver, boost synchronous half bridge, intermediate capacitor group) and corresponding PCB Layout of boost converter board are shown from fig. 6.6 to fig. 6.9.

The schematic design of boost bridge follows the theory above in chapter of Boost Converter, which is made of by 2 GaN transistors, one as switch, the other one as synchronous rectifier. Then two physical signal collector are taken into implementation:

- current feedback: use current sensor and shunt resistor to transform current signal to voltage signal;
- voltage feedback: use voltage divider, constructed by one big resistor and one relatively small resistor to transform high voltage into low voltage level with fixed ratio and small output current.

Besides, LED power detector and some other components are also taken into use for hardware debug.

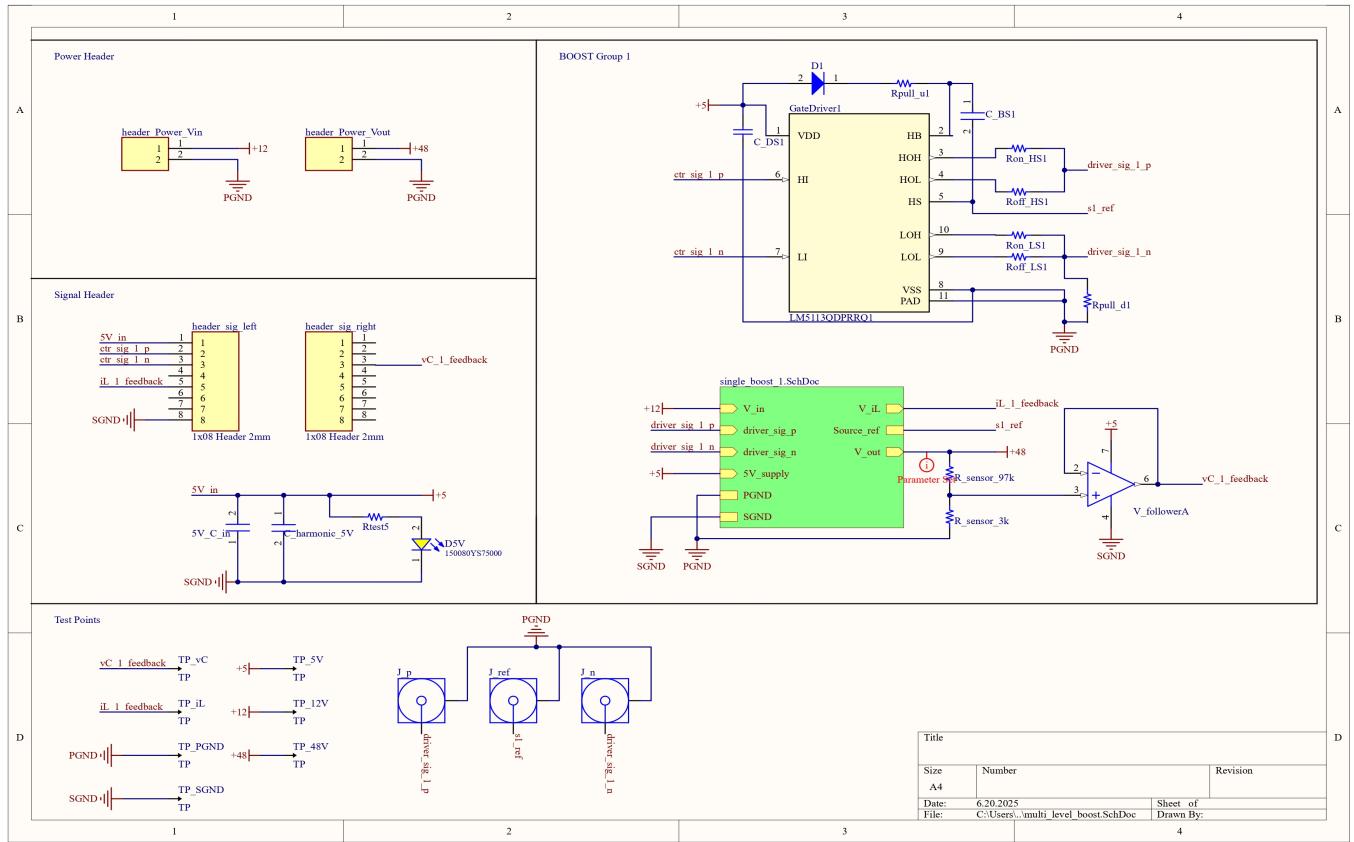


Figure 6.6: Schematic of external driver of boost converter board

6.1.3 Sub-Board: H Bridge Amplifier

The PCB of H Bridge amplifier is designed also as a 4 layer structure, which from top to bottom are signal layer, power ground layer, power signal layer and signal layer. The schematic and corresponding PCB Layout are shown in fig. 6.10 and fig. 6.11.

In order to decrease the noise and parasitic capacitive effect while measurement, the micro-miniature coaxial (MMCX) ports on board are placed as closely as possible to each gate signal termination.

6.2 Software Development

6.2.1 Software Framework - Parallel State Machine

According to the framework of this project in fig. 1.10, both functionality Boost converter and H Bridge amplifier are separate, which therefore can be regarded as two independent tasks, only

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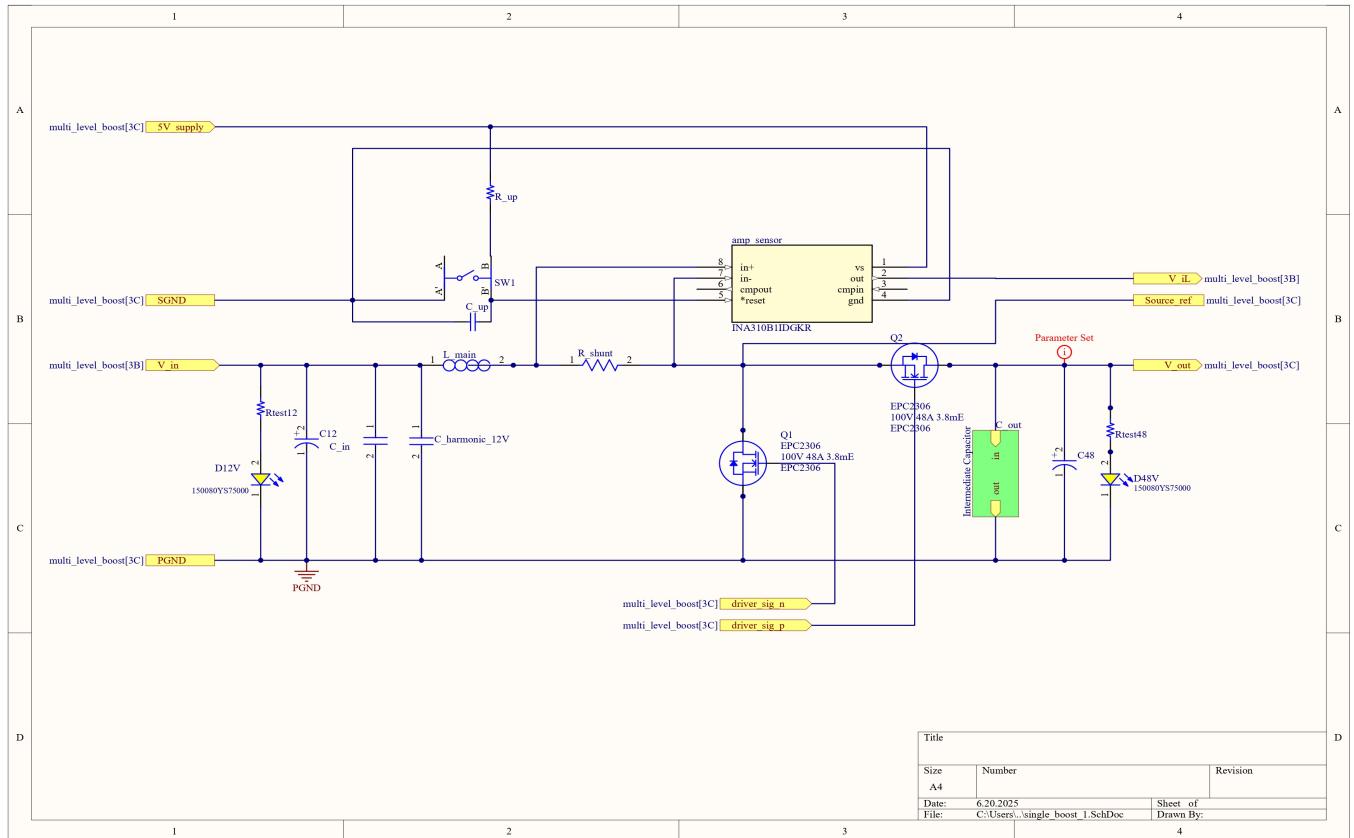


Figure 6.7: Schematic of synchronous bridge of boost converter board

communicate with microcontroller and share the 12 V DC power supply from the Boost converter. A parallel state machine architecture matches this requirement perfectly.

FreeRTOS is a real-time operating system kernel for embedded devices that has been ported to 40 microcontroller platforms [7]. It provides a powerful structure to build a real-time parallel state machine, which makes it possible that both boost and H Bridge amplifier task can run independently, with different, independent clock and would not be influenced by each other. The concrete software structure is shown below in fig. 6.12.

fig. 6.12 shows the states, transitions and events of 2 tasks as a way of state machine. Each task runs based on following process:

- starts from a entrance function in main.c;
- while not yet press the button, switch off, task stay in IDLE, which works as a pseudo state, task holds on;
- specific timer TIM16 and TIM17 provides a regular and cyclical hardware interrupt with fixed periode, which provides 2 fixed sampling time T_{s1} T_{s2} for different tasks;

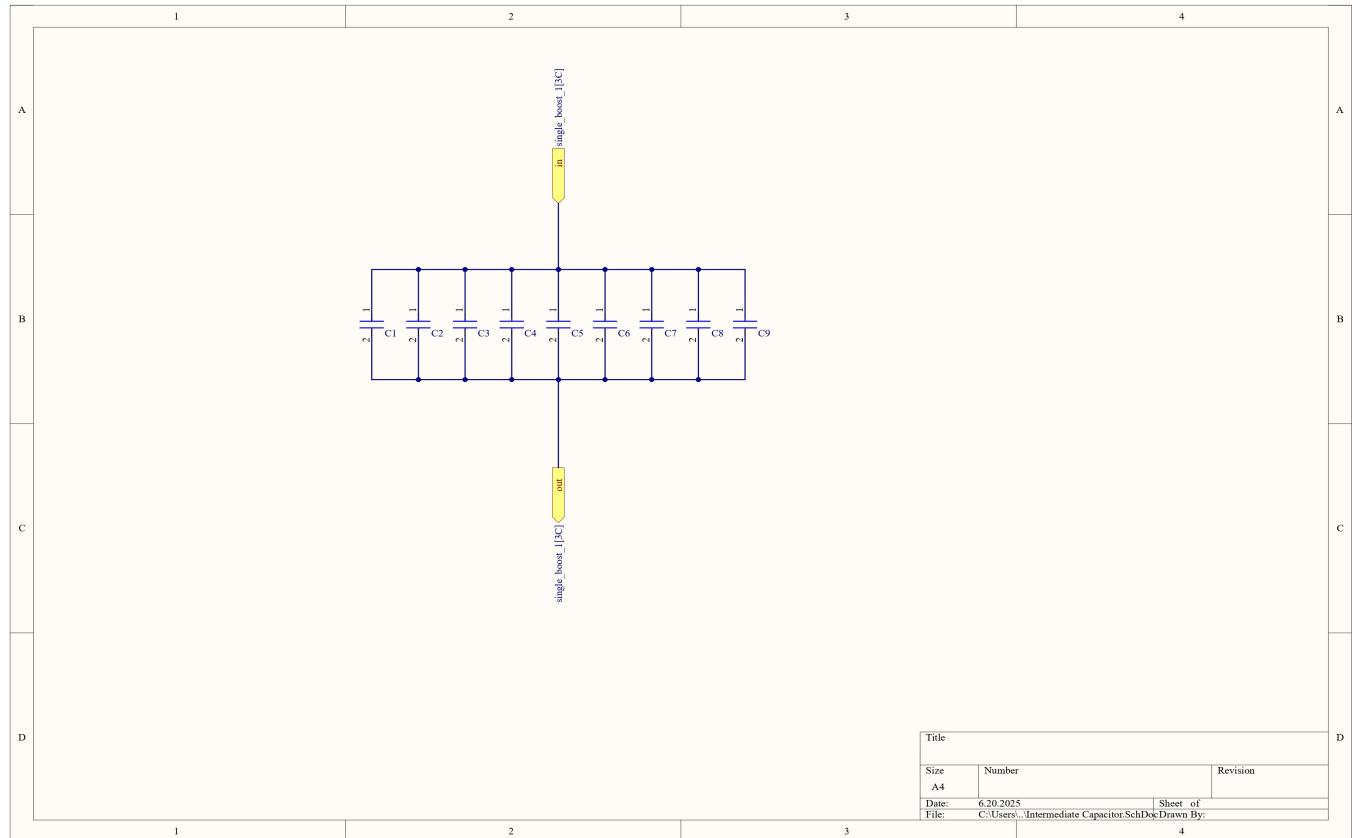


Figure 6.8: Schematic of intermediate capacitor group of boost converter board

- with both trigger from interrupt and switch on, task enters the task function called name_step() and runs;
- with calling the terminate function, tasks and the whole process terminate.

The details of resource allocation of software in microcontroller will be discussed in following sections.

6.2.2 Configuration of Microcontroller

In this project, STM32G4 works as microcontroller, locates on STM32G4 Nucleo-32 dev board which integrates STLINK and basic power supply circuit. The microcontroller is implemented in this project mostly as core controller for different tasks, PWM generator and ADC.

The PIN mapping and its corresponding description is shown in table .2 in appendix.

Beside the description in table .2:

- ADC1 is configurated in direct memory access (DMA) mode with 12-bit resolution with

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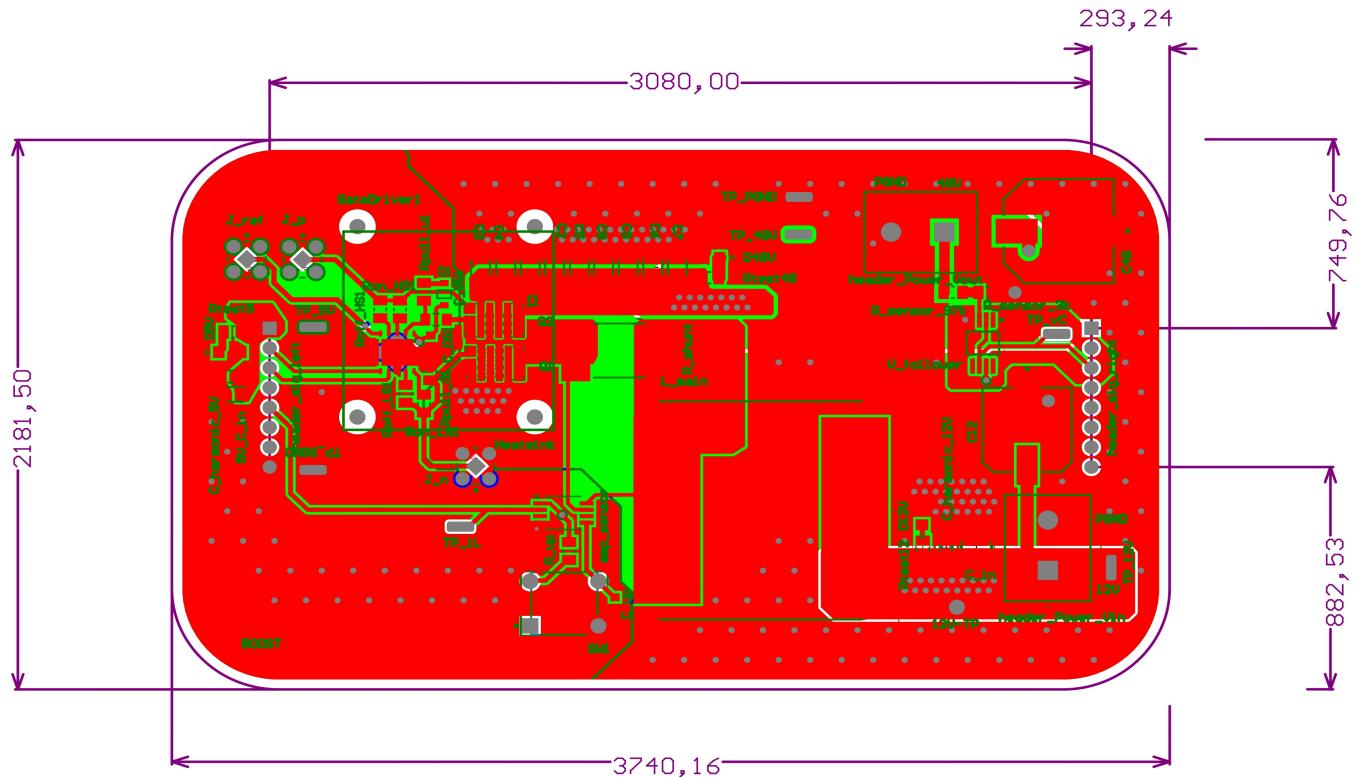


Figure 6.9: PCB layout of boost converter board

around 300 kHz sampling rate for 5 ranks: current feedback, voltage feedback, audio signal, 2 internal reference voltage;

- TIM16 and TIM17 are configurated as timer interrupt providing fixed sampling time for both boost task and H Bridge amplifier task, with respectively 50 kHz and 150 kHz.

In addition to these some other pins also work for state display connecting to LED.

6.2.3 Butterworth Digital Filter

Butterworth digital filter works as a very important component in both tasks, not only as a LP filter for feedback signal, but also as a band pass (BP) filter for audio signal, to increase specific frequency in order to make the frequency response of output signal closer to Harman curve [14].

The Butterworth filter is a type of signal processing filter designed to have a frequency response that is as flat as possible in the pass band, in the stop band it gradually decreases to zero. It is also referred to as a maximally flat magnitude filter.

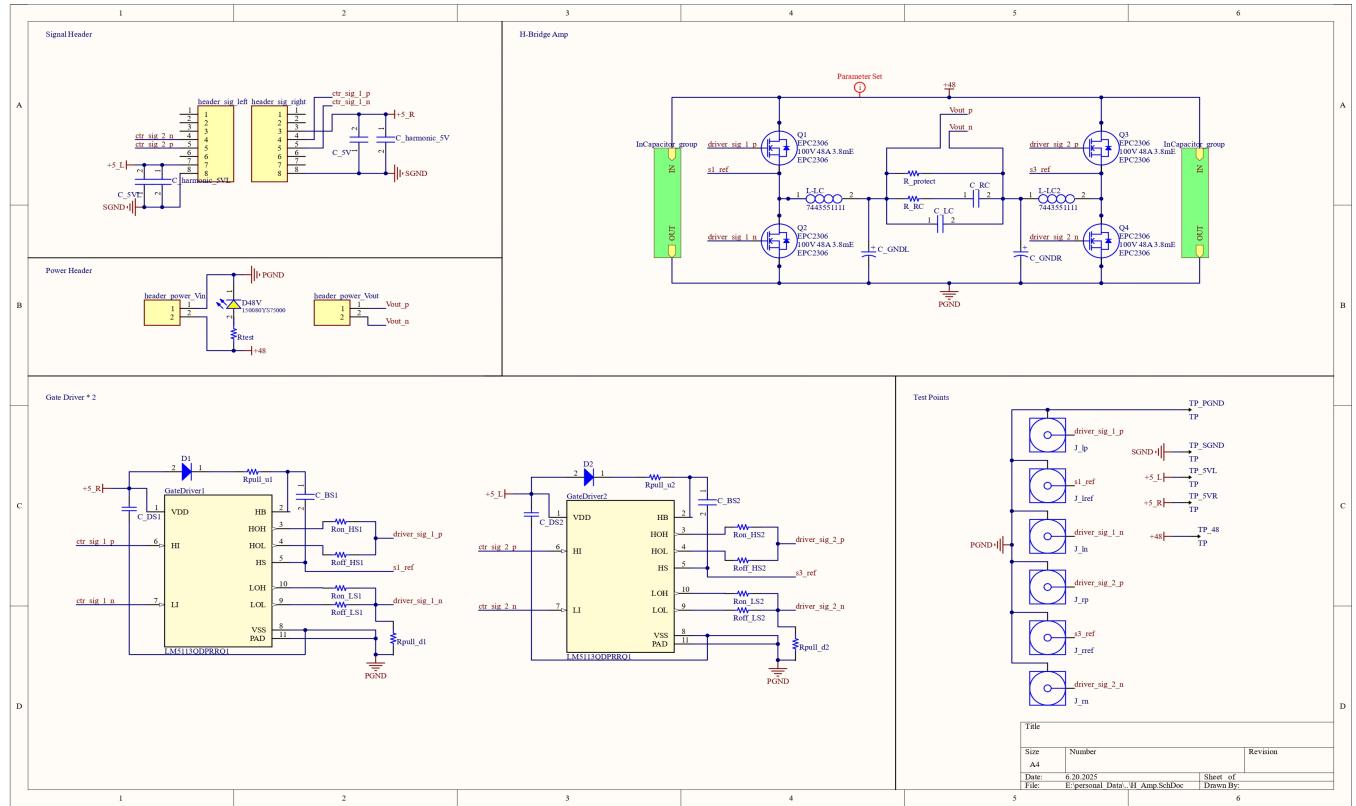


Figure 6.10: Schematic of H Bridge amplifier

6.2.3.1 LP Butterworth Filter

The original version of Butterworth filter corresponds to a LP filter. The gain $G(w)$ of an n th-order Butterworth LP filter is given in terms of the transfer function $H(s)$ as:

$$G^2(w) = |Hjw|^2 = \frac{G_0^2}{1 + \left(\frac{w}{w_c}\right)^{2n}} \quad (6.3)$$

where n is the order of filter, w_c is the cutoff frequency (approximately the -3 dB frequency), and G_0 is the DC gain.

It can be seen that as n approaches infinity, the gain becomes a rectangle function and frequencies below w_c will be passed with gain G_0 , while frequencies above w_c will be suppressed. For smaller n , the cutoff will be less sharp.

To determine the transfer function $H(s)$ where $s = \sigma + jw$ according to the Laplace transform. Because $|H(s)|^2 = H(s) \cdot \overline{H(s)}$ and as a general property of Laplace transforms at $s = jw$, the

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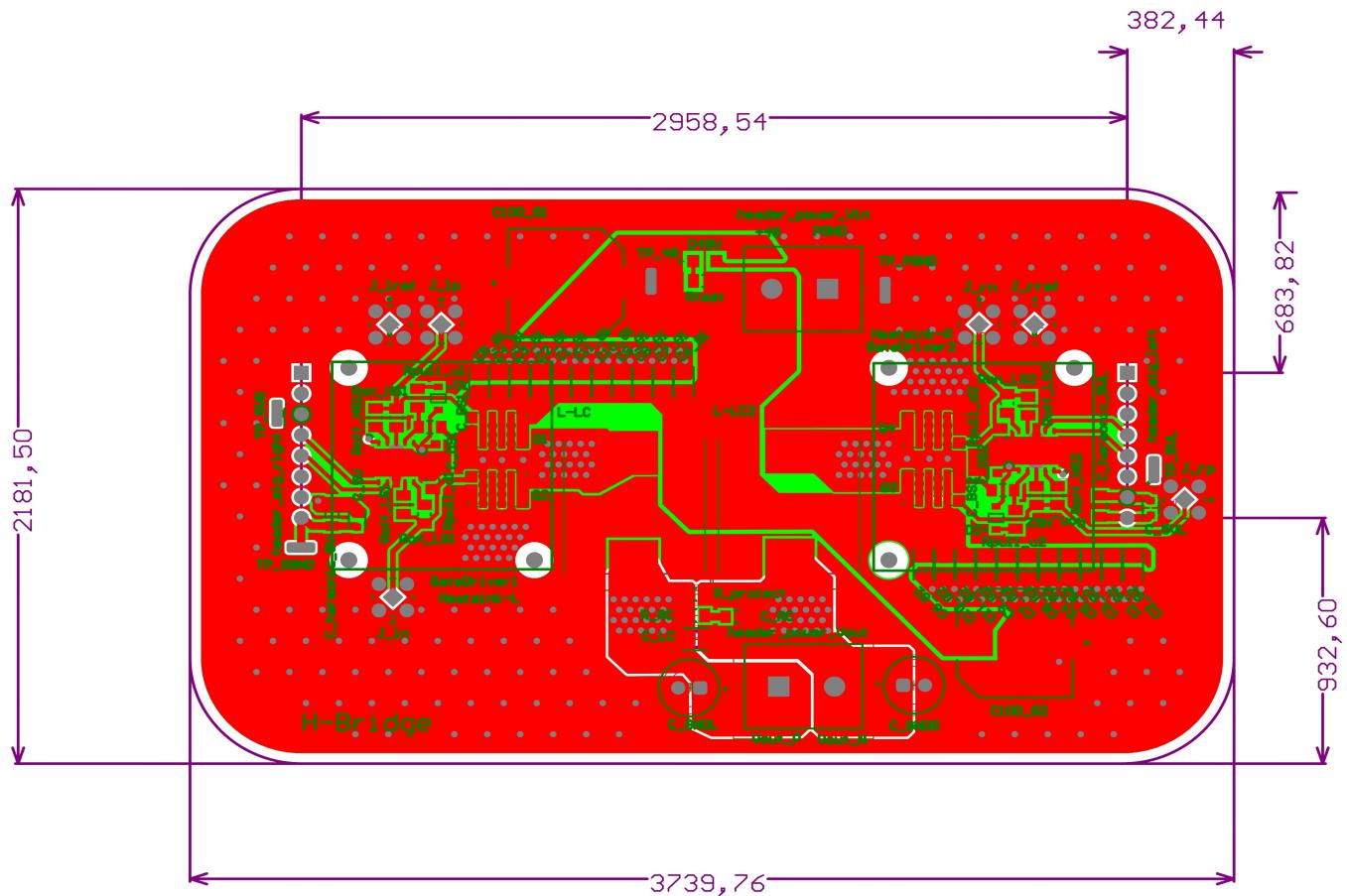


Figure 6.11: PCB layout of H Bridge amplifier

last equation can be replaced as:

$$H(s) \cdot \overline{H(s)} = H(s) \cdot H(-s) = \frac{G_0^2}{1 + \left(\frac{-s^2}{w_c^2}\right)^n} \quad (6.4)$$

The n poles of this expression occur on a circle of radius w_c at equally-spaced points, and symmetric around the negative real axis. For stability, the transfer function, $H(s)$ is therefore chosen such that it contains only the poles in the negative real half-plane of s . The k -th pole is specified by:

$$-\frac{s_k^2}{w_c^2} = (-1)^{\frac{1}{n}} = e^{\frac{j(2k-1)\pi}{n}} \quad (6.5)$$

with $k = 1, 2, 3, \dots, n$, hence:

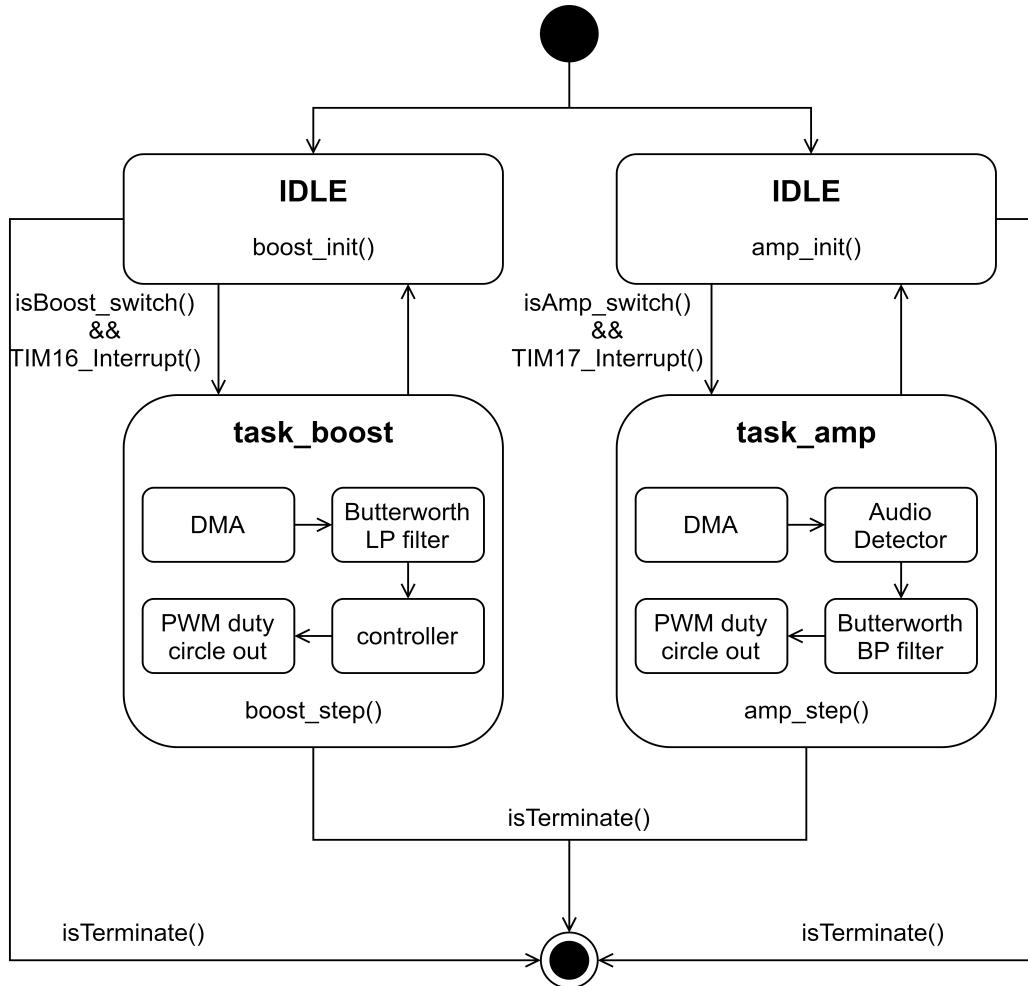


Figure 6.12: Software structure

$$s_k = w_c e^{\frac{j(2k+n-1)\pi}{2n}} \quad (6.6)$$

The transfer function can be written in terms of these poles as:

$$H(s) = G_0 \prod_{k=1}^n \frac{w_c}{s - s_k} = G_0 \prod_{k=1}^n \frac{w_c}{s - w_c e^{\frac{j(2k+n-1)\pi}{2n}}} \quad (6.7)$$

Then transform the complex form into real form with real coefficients:

$$B_n(s) = \prod_{k=1}^{\frac{n}{2}} [s^2 - 2s \cdot \cos\left(\frac{2k+n-1}{2n}\pi\right) + 1] \quad n = even \quad (6.8)$$

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$$B_n(s) = (s + 1) \prod_{k=1}^{\frac{n-1}{2}} [s^2 - 2s \cdot \cos(\frac{2k+n-1}{2n}\pi) + 1] \quad n = odd \quad (6.9)$$

Then use Bilinear Transform to map the continuous form into discrete form, which can be implemented into digital controller:

$$s = \frac{2}{T} \frac{z - 1}{z + 1} \quad (6.10)$$

6.2.3.2 HP and BP of Butterworth Filter

In order to get a high performance Butterowrth filter in terms of high pass (HP) or BP or other types, it's convenient to use the method of mapping in frequency domain.

The mapping from low frequency to high frequency bases on following equations:

$$s = \frac{w_c}{s} \quad (6.11)$$

and hence,

$$H_{HP}(s) = H_{LP}\left(\frac{w_c}{s}\right) \quad (6.12)$$

In terms of a BP filter, the mapping is:

$$s = \frac{s^2 + w_0^2}{B \cdot s} \quad (6.13)$$

where $w_0 = \sqrt{w_L w_H}$, w_L and w_H corresponds respectively to the lower and upper cutoff frequency of desired band. Hence,

$$H_{BP}(s) = H_{LP}\left(\frac{s^2 + w_0^2}{B \cdot s}\right) \quad (6.14)$$

Afterwards, apply eq. (6.10) to implement the filter into a digital platform.

6.2.4 Audio Detector

The input audio signal from this project is based on a 3.5mm Jack connector connecting directly with PC. When there is no audio signal generated from PC, the connector outputs a DC bias signal with multiple possible voltage level.

Because the speaker is a AC-sensitive component, the audio comes only from effective AC parts of the given signal. On the other hand, long time DC input could also damage the speaker and make some noise. So it's necessary to achieve an audio detector in order to get rid of the DC bias signal when there is no audio signal in.

The program diagram of the software audio detector is shown in fig. 6.13. The principle of this algorithm is a real-time updated shifted window.

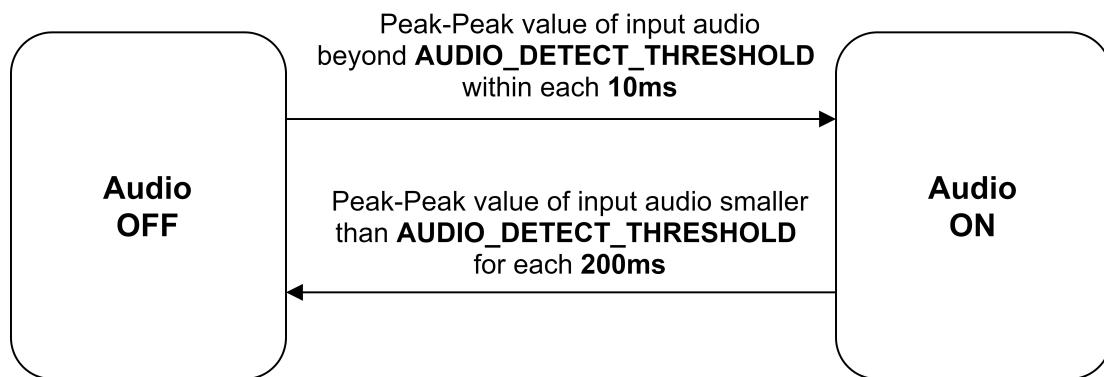


Figure 6.13: Program diagram of audio detector

This algorithm ensures that the audio play can start rapidly and stop carefully.

6.2.5 Class H: Adaptive Boost Output

Since the whole project is a Class D + H amplifier, the output of the boost converter is adaptive according to the amplitude of the input audio signal. This allows the boost converter to output a lower voltage when the input audio signal is small, thereby reducing system losses; whereas when the input audio signal is large, the boost module outputs a higher voltage, enabling the system to deliver greater output power.

The block in software is designed based on following principle:

- system initialization: $V_{DC} = 15V, K_{amp} = 0$;
- no audio detected: $V_{DC} = 13V, K_{amp} = 0$;
- $A_{audio} \in [V_{th}, 2] : V_{DC} = 15V, K_{amp} = 10$;

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- $A_{audio} \in [2, 3) : V_{DC} = 30V, K_{amp} = 5;$
- $A_{audio} \in [3, 4) : V_{DC} = 40V, K_{amp} = 3.75;$
- $A_{audio} \in [4, 6.6) : V_{DC} = 48V, K_{amp} = 3.125.$

where the V_{DC} , K_{amp} , A_{audio} refer to respectively the reference output amplitude of the boost converter, the H Bridge amplifier ratio, the amplitude of the input audio signal.

6.3 Parameter Optimization of the Experimental Setup

Based on the hardware design of previous chapters, print the Board and solder them together. The figure of the real Board is shown in fig. .1 in appendix.

The parameter optimization is related to both hardware part and software part, can be divided into following items:

- Dead time optimization
- PWM switching frequency optimization
- PID parameter optimization
- filter capacitor optimization

The selection of these parameters can greatly influence the performance of the whole system.

6.3.1 Dead Time Optimization

A suitable dead time for a complemented PWM output can avoid both long-duration and high-power-consuming body diode conduction (here for GaN is in fact a 3rd quadrant conduction) and the possibility of hazardous short circuits. Even though the theoretically optimized dead time is calculated in chapter 4, the practical PCB is not as perfect as a simulation model and therefore contain some parasitic components which could change some parameters, normally a larger gate capacitor.

In order to prevent excessive ringing caused by a larger gate capacitor during transistor turn-on and turn-off which could result in false turn-on or turn-off of the switch, a larger gate resistor needs to be matched to reduce the ripple. However, this slows down the switching speed, which consequently increases the optimal dead time.

This experimental procedure is to find the changed optimized dead time. STM32 series microcontroller only supports dead time that is an integer multiple of the system frequency 170 MHz, so the dead time here can only be $N \cdot 5.33$ (ns).

The selection of the optimized dead time based on both efficiency and temperature under switching frequency of 300 kHz, plot the result in fig. 6.14.

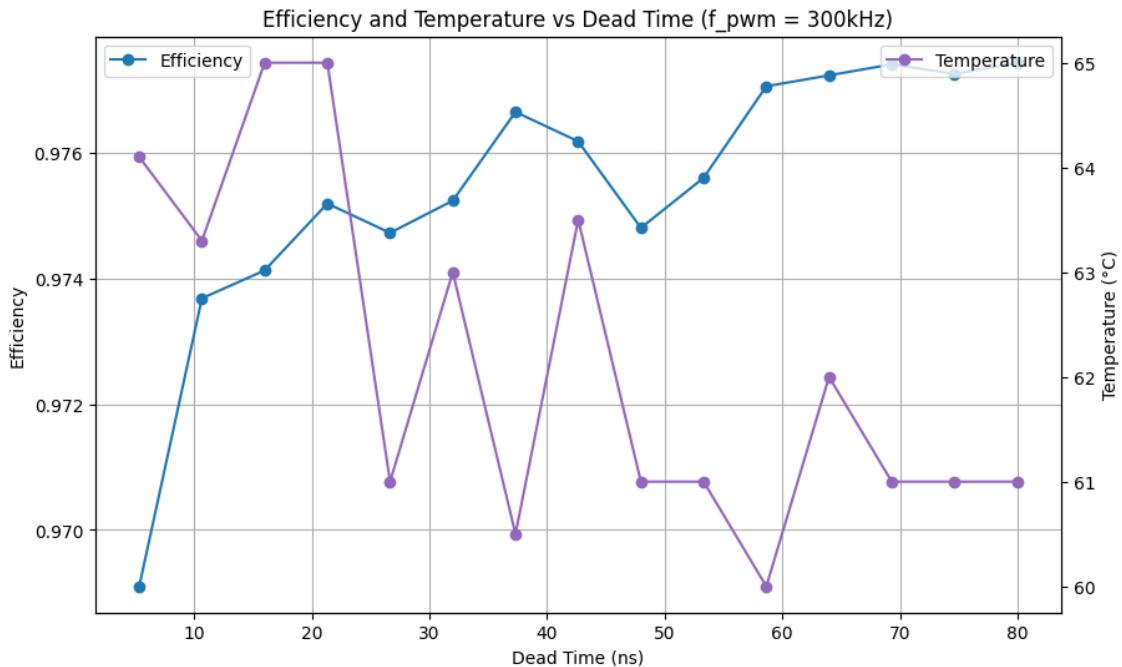


Figure 6.14: Parameter Optimization of Dead Time

In fig. 6.14 there is no obvious trend to find the optimized dead time with the highest efficiency. It could be because, parasitic components accounts for a significant proportion in the gate loop, bigger gate resistor is therefore needed in order to get rid of the huge ringing effect, which leads to however slower switching process, requiring a very long dead time to compensate. But longer dead time will also limit higher switching frequency, a compromise here is to choose a moderate dead time of 53.3 ns with acceptable efficiency.

6.3.2 PWM Switching Frequency Optimization

A switching frequency that is too low will lead to non-continuous conduction and thus high current ripples (under reasonable chosen inductance), but a higher switching frequency also increases switching losses. Therefore, it is necessary to find the optimal switching frequency that enables the system to achieve the highest efficiency and acceptable performance, the first item is tested in fig. 6.15.

The H Bridge amplifier works for high frequency audio signal of maximum 20 kHz, according to the Nyquist sampling theorem the sampling frequency and the PWM frequency must be at least two times of 20 kHz, namely 40 kHz, in order to reconstruct the audio signal. At practical using, it should be at least 8 - 10 times of that the higher, the better with lower THD. Since there is no

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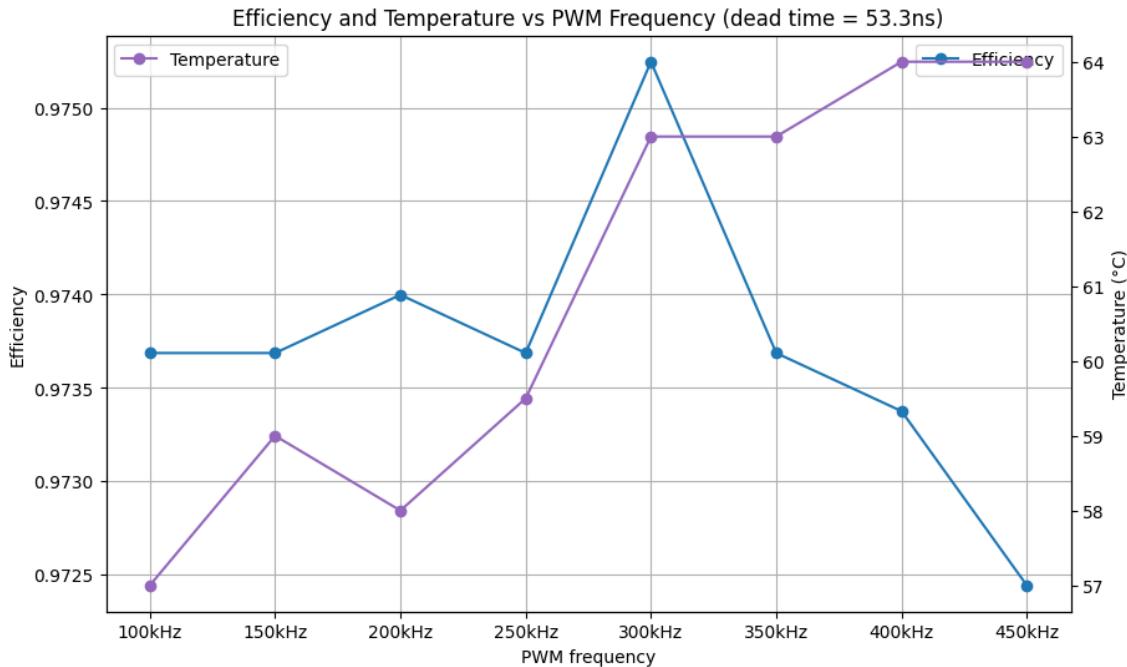


Figure 6.15: Parameter Optimization of PWM Frequency

feedback controller in H Bridge amplifier, the performance of it is from 300 kHz to 1 MHz tested and the output accuracy with the given input is tested. The result is illustrated as a Box Plot in fig. 6.16.

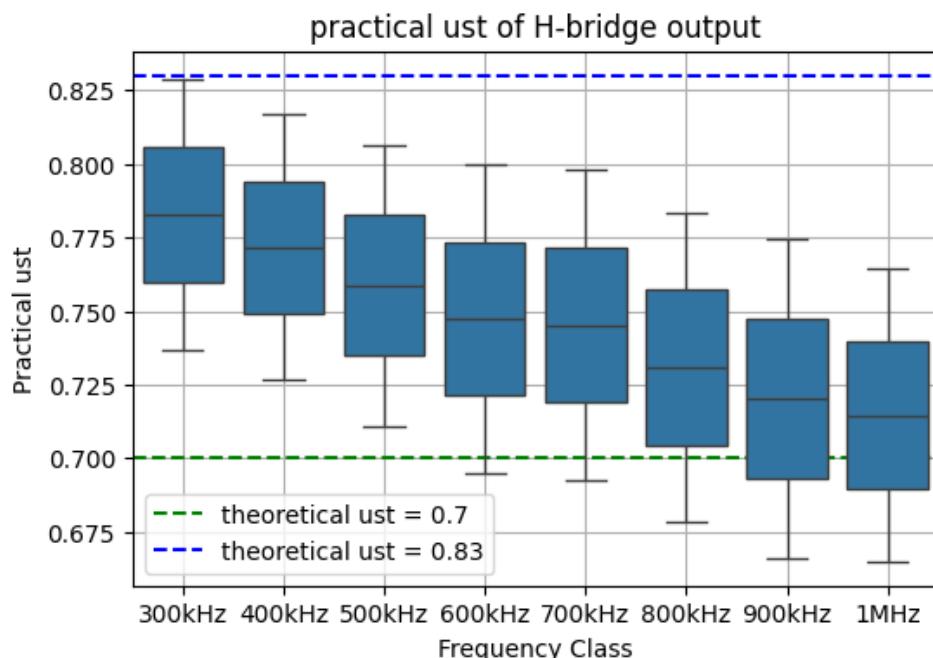


Figure 6.16: Parameter optimization of PWM frequency

Considering both fig. 6.15 and fig. 6.16, the optimized PWM Frequency is 300 kHz.

6.3.3 PID Parameter Optimization

In this subsection, the analytically calculated PID parameter for both current and voltage loop should be reconsidered once again to ensure the desired performance can be reached. Because the sampling time of the BOOST task is much higher than the desired response time, this system can be approximately regarded as a continuous system. Keep the parameters of the current controller invariant, adjust the parameters in voltage loop.

Ziegler–Nichols method is implemented here as a heuristic method of tuning a PID controller [21]. It is performed by setting the integral and derivative gains to zero. The proportional gain K_p is then increased from zero until it reaches the ultimate gain K_u , at which the output of the control loop has stable and consistent oscillations. K_u and the oscillation period T_u are then used to set the P, I, and D gains depending on the type of controller used and behaviour desired in table .3 listed in appendix.

6.3.4 Filter Capacitor Optimization

As what is shown in fig. 5.7 and fig. 5.8, 2 places of additional electrolytical capacitors are reserved in advance for further improvement of LP filter in H Bridge amplifier's output stage. Test the performance of H Bridge amplifier with different kinds of loads, with or without additional capacitors, then compare their performance to choose the best one.

A THD analyser for signal and THD analysis is set up. Its working principle is shown in fig. 6.17.

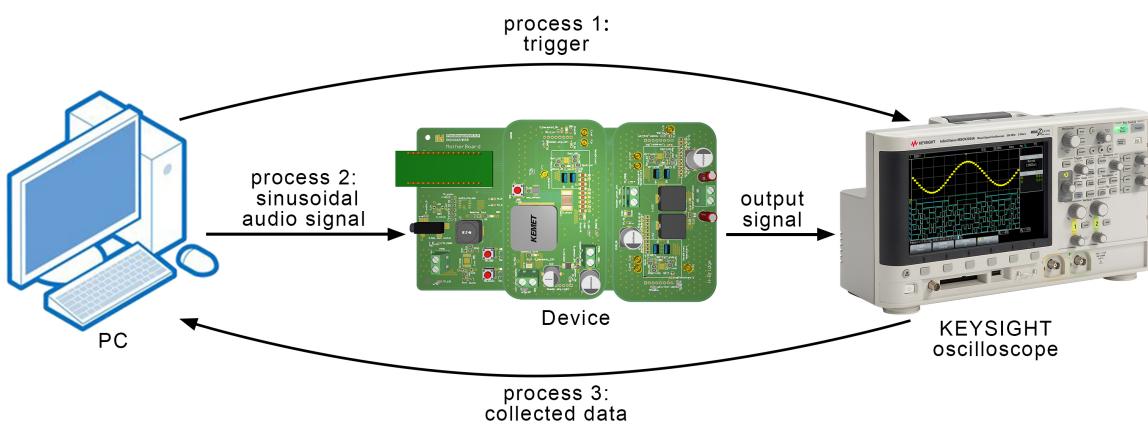


Figure 6.17: Principle of THD analyzer

Utilizing this THD analyser to fastly measure and analyze the responses towards input sinusoidal

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audio signal groups from 20 Hz to 20 kHz. Different output loads of 8 ohms pure resistor, 4 ohms pure resistor and real bass speaker with 4 ohms equivalent impedance, respectively with or without additional capacitors are tested. The result is illustrated in fig. 6.18.

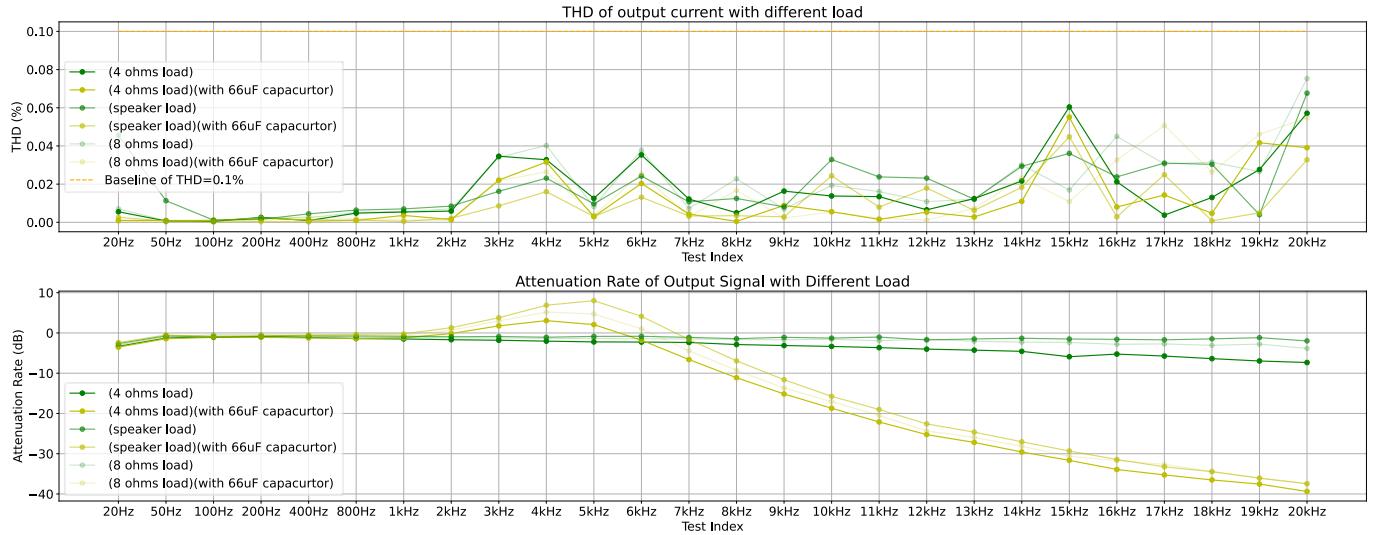


Figure 6.18: THD analysis for different configurations

According to this figure it's obvious, the system performance is greatly improved for both THD and damping ratio:

- in terms of THD, the additional capacitor reduce the THD of output signal and eliminates more high frequency noise;
- in terms of damping ratio, the additional capacitor improves the performance of the LP filter.

With fast fourier transform (FFT) analysis, this improvement can be better observed. The fig. 6.19 and fig. 6.20 represent the FFT analysis of both output voltage and output current compared with the 5 kHz sinusoidal input signal, both connecting to the bass speaker as load and respectively with or without additional capacitors.

While without additional capacitors, there is a very obvious harmony existing at both full frequency range and around 300 kHz, which is produced by the PWM frequency. While adding capacitors, the high frequency harmony is eliminated, and the whole spectrum is much cleaner than before.

Therefore the implementation of these additional capacitors as $66 \mu\text{F}$ is necessary for the performance of the LP filter at output stage.

6.3 Parameter Optimization of the Experimental Setup

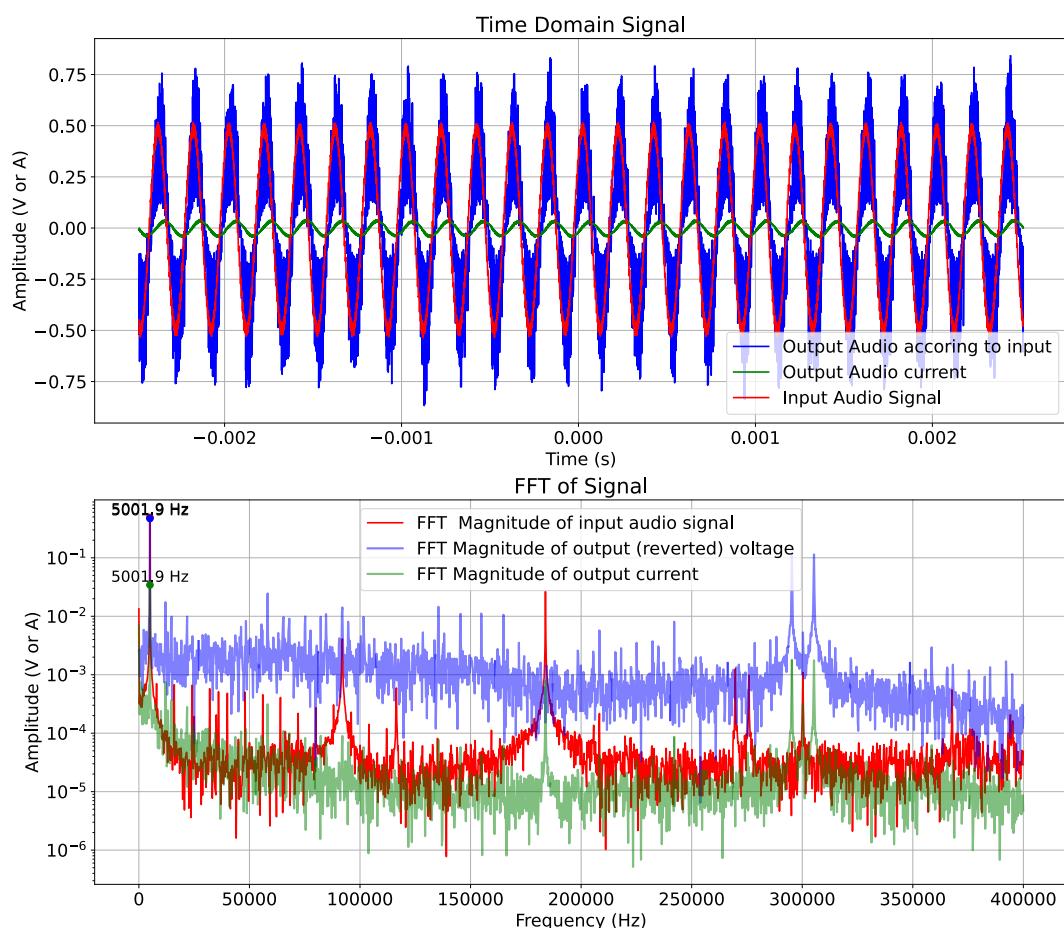


Figure 6.19: FFT analysis for 5 kHz input, without additional capacitors

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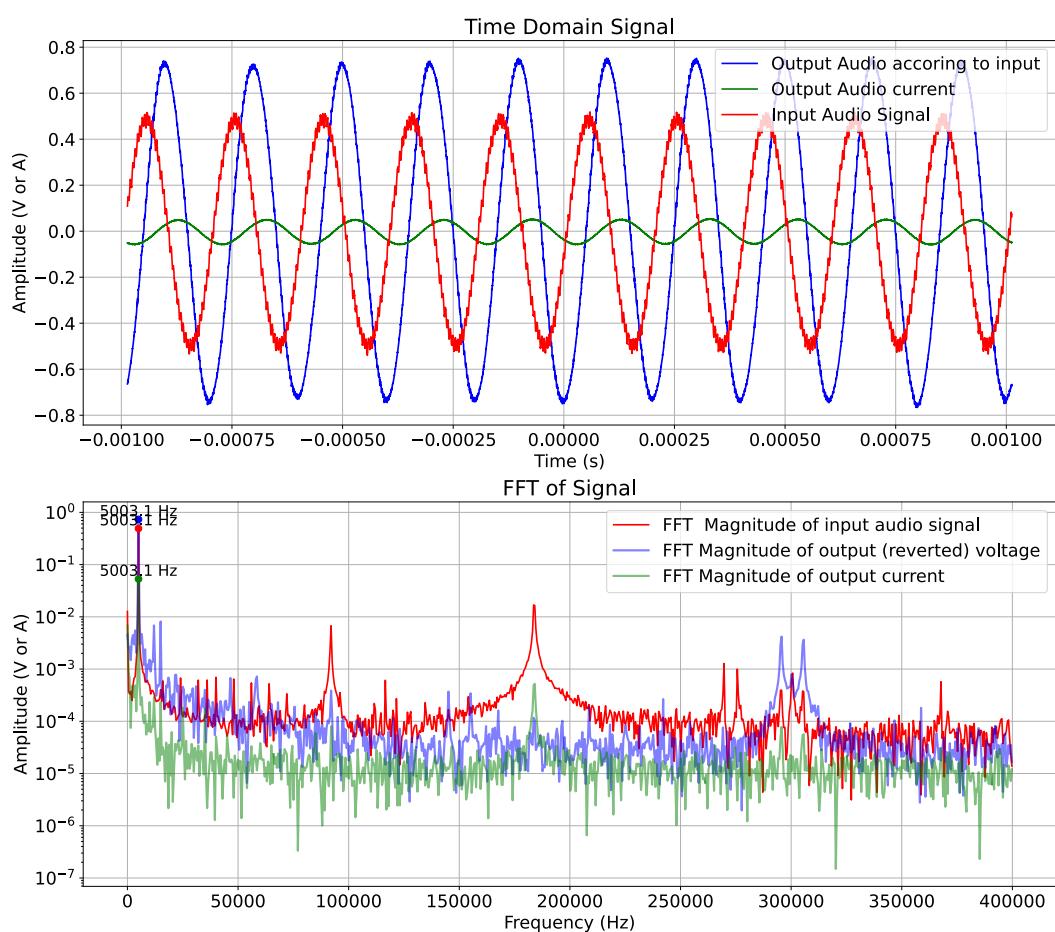


Figure 6.20: FFT analysis for 5 kHz input, with $66 \mu\text{F}$ capacitors

7 Performance Test And Audio Quality Improvement

7.1 Performance of Boost Converter

The performance of Boost converter is divided into several parts:

- dynamic performance: response time;
- steady-state performance: ripple;
- efficiency testing.

For the first and second item, the workflow is to measure the response time from 10 V (IDLE) to 48 V (maximum output voltage level), and the peak to peak value after it reaches 48 V. The result is illustrated in fig. 7.1. The response time of it is around 150 ms and the ripple at 48 V is around 0.3 V, which are acceptable.

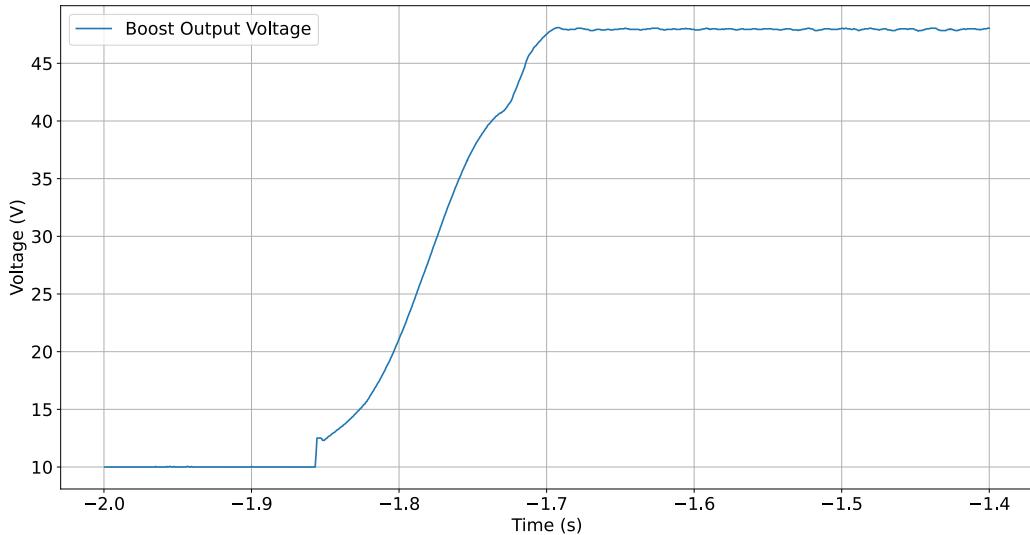


Figure 7.1: Boost converter output voltage

For the third item, connecting it to a pure resistive load and utilizing a power analyzer, the real-time output power is measured. At 120 W output power the converter reaches to 65 °C with an

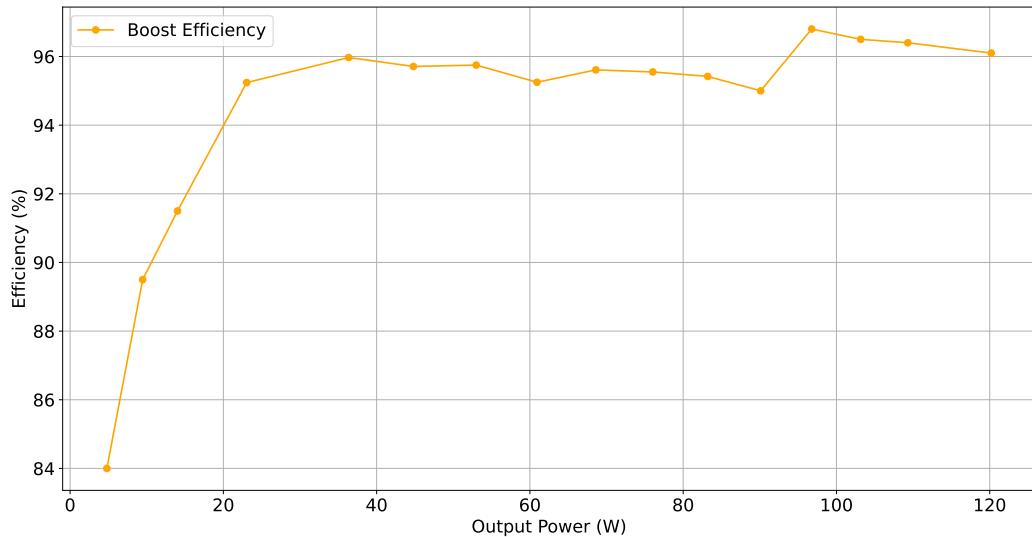


Figure 7.2: Boost converter efficiency

efficiency of $\eta_{\text{Boost}} = 96\%$.

7.2 Performance of Class H Amplifier and Boost Converter

According to the introduction of the logic of a class H amplifier, the performance of the output voltage of the boost converter with an audio input signal with varying amplitude is tested. Figure 7.3 shows that the voltage signal perfectly follows the amplitude variations of the audio signal.

It is important to ensure that variations in the current input volume are due to intentional user adjustments rather than a musical piece merely transitioning into a softer passage, as the latter might be very brief, even shorter than the boost converter's response time of around 140 ms, which is too slow to follow such short-term dynamics without potentially degrading audio quality. Therefore, the Class H volume detection incorporates a 1-second software delay to distinguish genuine volume changes, minimizing the risk of inappropriate DC voltage adjustments affecting the audio signal amplitude.

7.3 Audio Quality Improvement

The Harman curve, as an empirical curve, has long been used as one of the standards for evaluating the output quality of audio equipment. So one way to improve the performance of the H Bridge

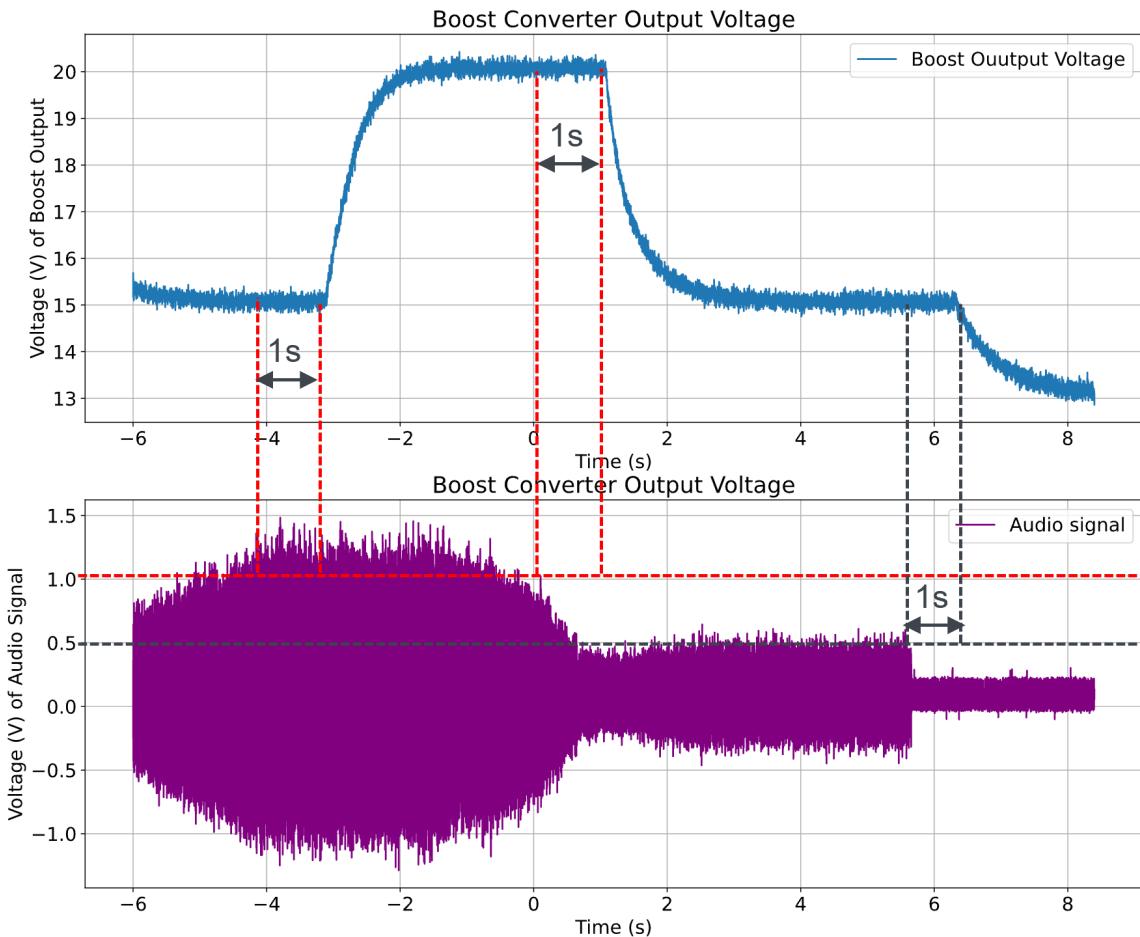


Figure 7.3: Performance of adaptive boost converter's output

amplifier is to make the output curve closer to the Harman curve.

The testing result in fig. 6.18 shows the current damping rate of the H Bridge Amplifier is much closer to a LP filter's property curve, which is consistent with the characteristics of low-frequency (Bass) speaker, attenuated at high frequencies. But according to the Harman curve, it should have a 10 dB gain in both low frequency and high frequency in order to better reproduce the true audio information.

Several different methods through adding different kinds of Butterworth filters are implemented here. The output signal is then equal to:

$$V_{out} = K_1 \cdot V_{in} + K_2 \cdot V_{filter} \quad (7.1)$$

where the V_{filter} is the audio signal after processing of the digital Butterworth filter. The result

7 Performance Test And Audio Quality Improvement

is illustrated in fig. 7.4. The Band Stop filer on the bottom right has the best performance with $K_1 = 1$ and $K_2 = 0.8$, which almost perfectly match the Harman curve, which corresponds to a good audio quality.

The output attenuation rate rises to 10 dB both from 20 Hz to 100 Hz and from 1 kHz to 10 kHz, at mid-frequency range keep around 0 dB. It exhibits stylized enhancement in the low-frequency range, aims to preserve the original characteristics of the audio as much as possible in the mid-frequency range, and boosts the high-frequency range to compensate for the natural attenuation that high-frequency audio signals tend to experience during propagation.

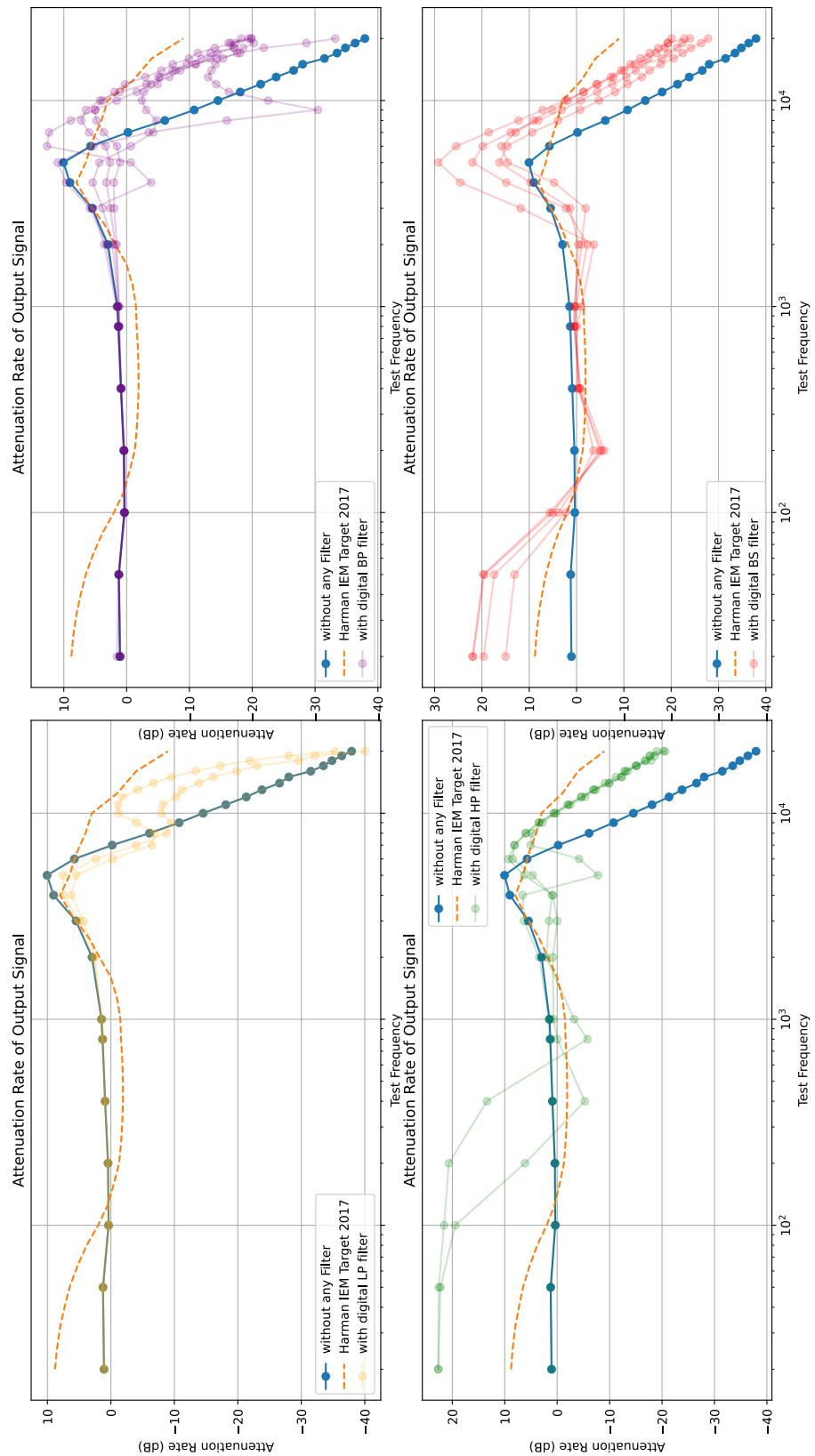


Figure 7.4: Improved audio signal with digital filter comparing with Harman curve

8 Conclusion and Outlook

8.1 Conclusion

Table 8.1: Performance comparison of different amplifier references

Parameter	Unit	This Thesis	EPC Ref.	Si Ref.	Class A/B Ref.
THD	%	0.03	0.005	0.05	0.001
Efficiency	%	96	96	90	60
Power Density	W/cm ³	6	5.83	4	0.3
Switching frequency	kHz	300	600	250	—
Max. Power	W	200	350	315	100

Table 8.1 presents a comparison between the Class D/H amplifier proposed in this work and several reference products based on common topologies, respectively the EPC2307 reference Board based on GaN transistors and class D strategy, the silicon based class D reference chip TPA3255 by Texas Instrument, and professional analog audio amplifier XA25 based on class A.

In terms of THD, traditional analog audio amplifiers still demonstrate superior performance, owing to the excellent linear characteristics of analog topologies such as Class A. Regarding efficiency, both this work and the EPC reference board achieve the highest levels, attributable to the lower on-resistance and reduced switching losses of GaN devices.

For power density, this work achieves the highest figures of 6 W/cm³; however, this comes at the cost of lower rated voltages for smaller SMT component sizes, thereby limiting the maximum achievable output power. As for switching frequency, significant parasitic capacitance in the gate loop of the PCB layout necessitates larger gate resistors to mitigate the ringing effect, which reduces switching speed and ultimately results in a lower optimal switching frequency. Compared to the EPC reference board, there remains considerable room for improvement.

This work also introduces several improvements in terms of architecture, parameter optimization, and software implementation.

In terms of parameter optimization, this work leverages the characteristics of GaN switches, including the absence of a body diode, low conduction losses, and low driving losses, enabling both the Boost converter and the H-Bridge amplifier to maintain an efficiency of around 96% at 120 W output power. This significantly reduces the switching losses of the system, thereby

8 Conclusion and Outlook

improving overall system performance.

Meanwhile, the introduction of the Class H functionality further enhances the system's capability for adaptive output voltage control. This allows the system to use a lower output voltage when handling small audio signal amplitudes and a higher output voltage when processing large audio signal amplitudes, thereby further improving overall system efficiency.

In addition, on the software side, the design of the Audio Signal Detector prevents the system from outputting a DC signal for extended periods when there is no audio input, thereby protecting the speaker from damage. The application of real-time operating system (RTOS) for parallel processes enables independent operation of multiple tasks with different periods. The implementation of filter anti-aliasing achieves improved audio output quality, bringing the output curve very close to the Harman curve.

8.2 Outlook

This project has achieved encouraging results by implementing a digital Class D audio amplifier based on GaN devices, delivering high system efficiency and power density. Additionally, various software-level features have been integrated, such as Class H adaptive voltage control, audio signal detection, and RTOS based multitasking management. However, there remain several areas for further optimization. Future work can focus on the following aspects:

- Higher-Performance Audio Sampling and Processing
 - Introducing dedicated high-resolution, high-speed ADC chips to replace the internal ADC of the STM microcontroller, thereby improving audio sampling precision and signal-to-noise ratio.
 - Considering the adoption of higher-performance digital signal processor (DSP)s or field-programmable gate array (FPGA)s as the control core to support more complex audio processing algorithms and higher sampling rates.
- Optimizing PCB Layout Design
 - Enhancing simulation and optimization of high-speed circuit PCB layout in future designs to minimize the impact of parasitic inductance and capacitance, reducing reliance on large gate resistors.
 - Simplifying unnecessary vias and inter-layer connections to improve manufacturability and reduce risks associated with soldering and debugging.
- Improving System Dynamic Response
 - Optimizing the control algorithms of the Boost converter and H-Bridge to enhance

dynamic response speed, enabling the system to better handle rapid transient dynamics within audio signals.

- Exploring more advanced control strategies, such as feedforward control or adaptive control, to further reduce dead time and lower system losses.
- Enhancing Audio Quality
 - Further improving digital filter design to reduce aliasing distortion and more precisely match the Harman curve, thereby enhancing auditory experience.
 - Considering the integration of more intelligent audio analysis modules in the algorithms to enable personalized optimization for different music styles or usage scenarios.
- Enhancing System Intelligence and Interactivity
 - Integrating richer communication interfaces (such as Bluetooth, WiFi, Ethernet) to enable remote monitoring and dynamic adjustment of amplifier parameters.
 - Incorporating AI algorithms for audio content recognition and dynamic tuning to further enhance the user experience.

Overall, digital Class D audio amplifiers combined with GaN technology offer significant potential for development in the audio electronics field. Through ongoing hardware and software iterations, this system has the potential to achieve further breakthroughs in power density, efficiency, audio quality, and intelligence, making it suitable for a wide range of applications, from high-fidelity audio systems to portable devices.

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Appendix

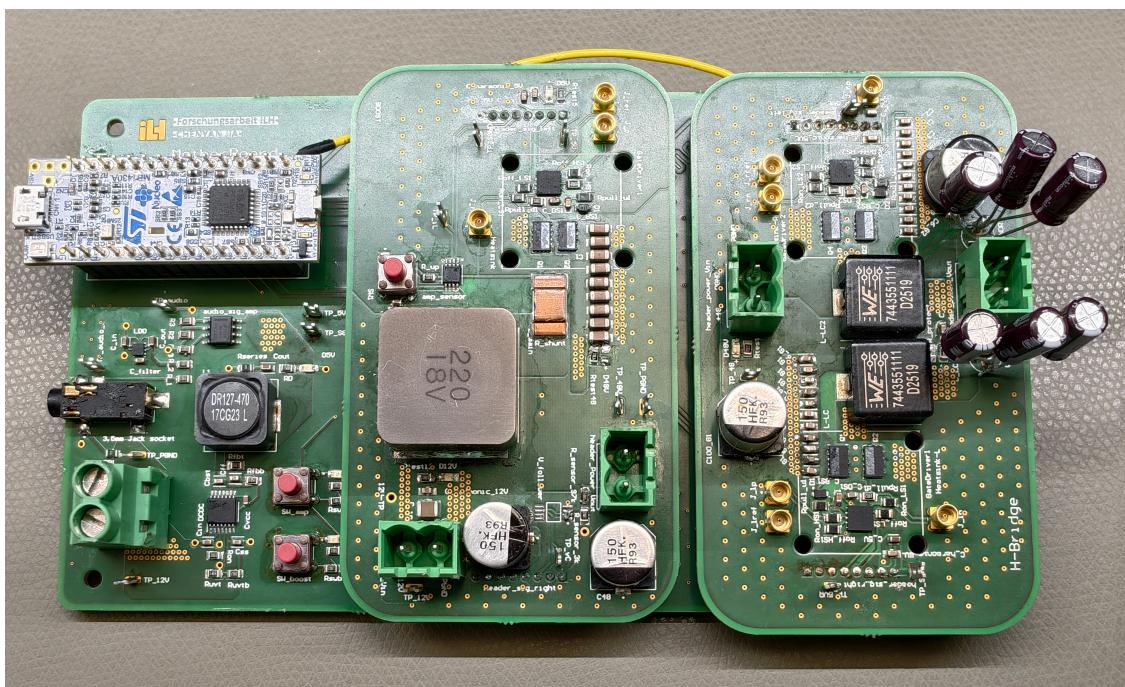


Figure .1: Real PCB

Appendix

Table .1: Component list

Resource List					
Board	Sub Group	Block	Function	Component	Description
Mother Board	Headers	signal header	control/sensor signal in/out	1x08 Header 2mm	header boost sig left
				1x08 Header 2mm	header boost sig right
				1x08 Header 2mm	header Amp sig left
		power header	Provide ext +5V	1x08 Header 2mm	header Amp sig right
				Ferrite bead	MPZ2012S601AT000
	Nucleo-32 ARDUINO CONNECTORS	Connecting MCU	12V > 5V	1548128 Phenox header	header Power Vin
				R filter	100ohms, SMD
				C0603C105K3RACTU	1uF, 0603
				LM5160QPWPQ1	DCDC chip
				C1608X5R1C335K080AC	Cin, 3.3uF, 0603
Daughter Board Boost Converter	DCDC	12V > 5V	Functional control and check	06033C223KAT2A * 2	Css, Cff, 22nF, 0603
				06033C103KAT2A	Cbst, 10nF, 0603
				C0603C105K3RACTU	Cvc, 1uF, 0603
				GRM188R604J76ME15D	Cout, 47uF, 0603
				DR127-470-R	L1, 47uH
	Audio Signal Transformer	audio_sig_amp	Make sure the audio input signal is always positive and in range (0.476V , 1.944V)	SMD*7	
				150080YS75000	LED
				150080YS75000 * 2	LED
				SMD*4	
				EVQ-PAG05R * 2	switch
Daughter Board H-Bridge	Boost Converter	Gate Driver	Generate a 3.3V bias for connecting amp	TPS7A3501DRV	LDO, 5.35V-3.3V, TI
				C1608X5R1A106K080AC	C LDO in, 10uF, 0603
				C1608X5R1A104K080AA	C LDO out, 10uF, 0603
				C0603C105K3RACTU	1uF, 0603
				OPA1656ID	opamp, TI
	H Bridge Amplifier	GaN Bridge	One group of full Boost converter	35RASMD4BHNTRX	3.5mm jack socket
				SMD 100 ohms * 1	
				SMD 1k ohms * 4	
				150080YS75000	LED
				LM5113QDPRRQ1	Gate driver, TI

Table .2: PIN mapping of microcontroller

PIN Name	PIN Location	Functionality	GPIO
iL_1_feedback	PA0	current feedback signal of boost converter	ADC1_IN1
vC_1_feedback	PA1	output voltage feedback signal of boost converter	ADC1_IN2
audio_sig	PA2	modified audio signal	ADC1_IN3
boost_state	PB7	on/off of boost converter	GPIO_Output
boost_switch	PF1	switch of boost converter	GPIO_EXTI1
amp_state	PB0	on/off of bridge amplifier	GPIO_Output
amp_switch	PB6	switch of H amp	GPIO_EXTI6
ctr_boost_sig_1_p	PA15	PWM sig of HS	TIM8_CH1
ctr_boost_sig_1_n	PA7	PWM sig of LS	TIM8_CH1N
ctr_amp_sig_1_p	PA8	PWM sig of HS left arm	TIM1_CH1
ctr_amp_sig_1_n	PA11	PWM sig of LS left arm	TIM1_CH1N
ctr_amp_sig_2_p	PA10	PWM sig of HS right arm	TIM1_CH3
ctr_amp_sig_2_n	PF0	PWM sig of LS right arm	TIM1_CH3N

Appendix

Table .3: Ziegler-Nichols tuning rules for different controllers

Control Type	K_p	T_i	T_d	K_i	K_d
P	$0.5K_u$	—	—	—	—
PI	$0.45K_u$	$0.83T_u$	—	$0.54K_u/T_u$	—
PD	$0.8K_u$	—	$0.125T_u$	—	$0.10K_uT_u$
classic PID	$0.6K_u$	$0.5T_u$	$0.125T_u$	$1.2K_u/T_u$	$0.075K_uT_u$
Pessen Integral Rule	$0.7K_u$	$0.4T_u$	$0.15T_u$	$1.75K_u/T_u$	$0.105K_uT_u$
some overshoot	$0.33K_u$	$0.50T_u$	$0.33T_u$	$0.66K_u/T_u$	$0.11K_uT_u$
no overshoot	$0.20K_u$	$0.50T_u$	$0.33T_u$	$0.40K_u/T_u$	$0.066K_uT_u$