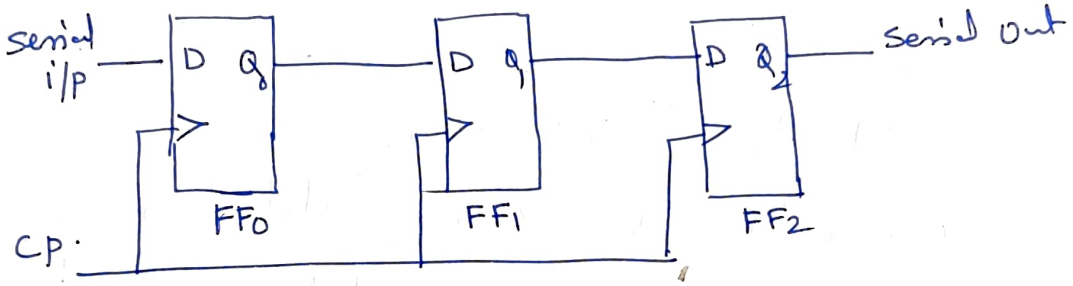
Shift Registers

* shift registers are capable of moving or shifting the data stored in their flip flops in either direction
* shift registers use D f/fs in cascade.

I Serial in serial out shift register

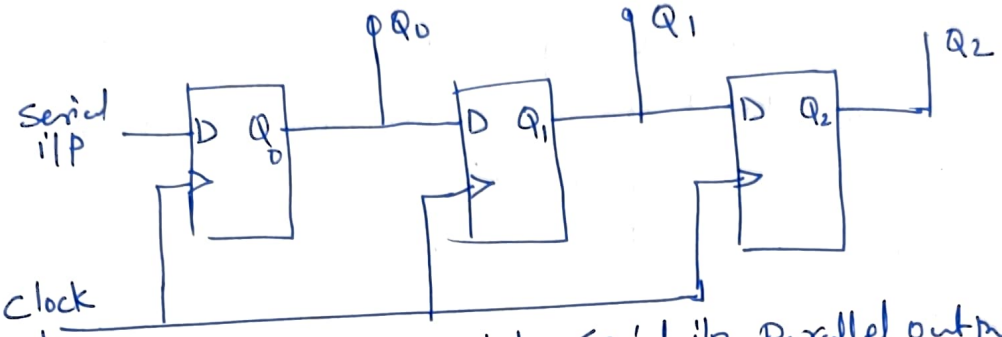


* 3bit SISO shift register.

* 3 f/f are cascaded, clock pulse applied to all f/fs simultaneously.
* at each clock pulse serial i/p data enters in FF0 (First D f/f), i/p data shift to o/p by all F/Fs
* at every clock pulse o/p of each FF shift to next stage and, out put taken serially from FF2. (Q_2).

serial i/p.	o/p. Q_0 Q_1 Q_2	CP	serial Output Q_2.
1	1 0 0	1	0
1	1 1 0	2	0
1	1 1 1	3	1
0	0 1 1	4	1
0	0 0 1	5	1
0	0 0 0	6	0

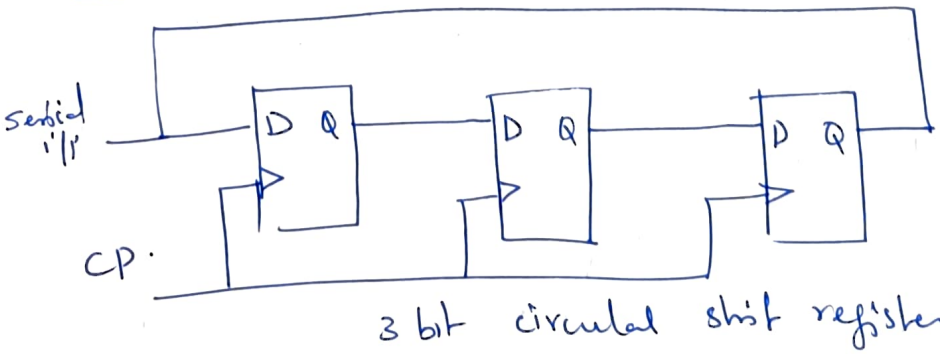
Serial i/p Parallel output shift register



3 bit Serial i/p Parallel output shift register.

* 3 D F/F's are cascaded to form 3 bit SIPO shift register
* Serial i/p given to FF0.
* Out puts are taken parallel from Q_0 Q_1 Q_2
* at every clock pulse data entered from serial i/p to FF_0 and shift to FF_1 & FF_2 consecutively.

serial i/p	clock pulse	o/p's Q_0	Q_1	Q_2
1	0	0	0	0
1	1	1	0	0
0	2	0	1	0
1	3	1	0	1
1	4	1	1	0



3 bit circular shift register.

Counters

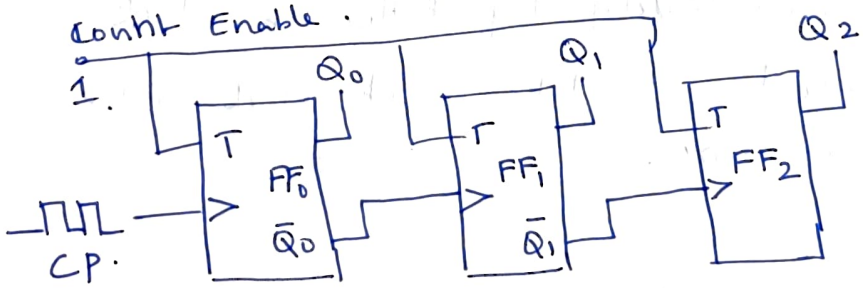
* Counter is a cascade of f/f configured to output a specific sequence on applications of a clock.
* Each output of the sequence is depends on the contents of a F/F called a State of the counter.
* out put of a counter is binary sequence.
* A cascade of F/Fs can be used to configure a counter upto Modulus of 2^n.

Two types of counters

1) Synchronous Counter
2) Assynchronous counter. (Ripple counter)

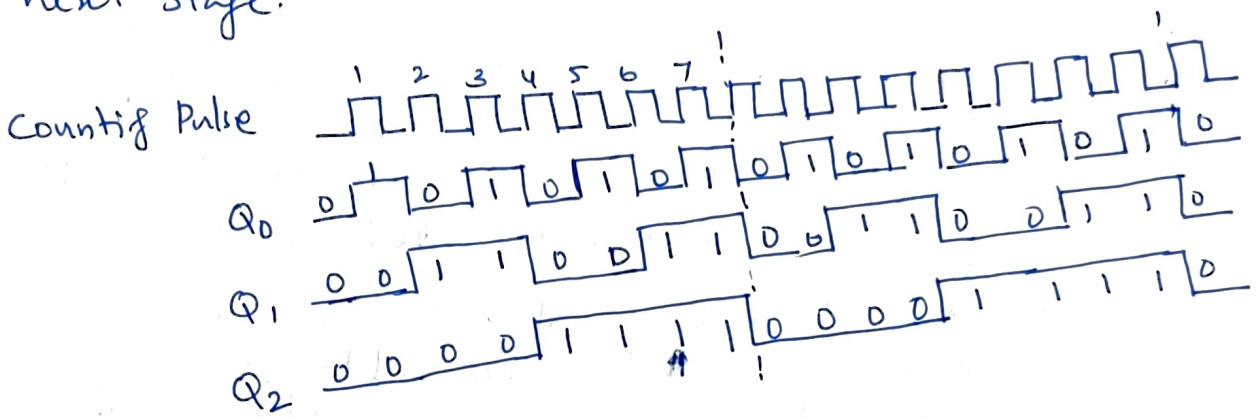
Assynchronous Counter. (Ripple counter)

Modulo 8 or Modulus 8 counter.



* Modulo 8 counter uses 3 flip flops in cascade.
* Its 3 bit binary counter produce out put from 000 to 111 in sequence.
* All T i/ps are connected to high for enabling toggle condition
* O/p is takes from $Q_0 Q_1$ & Q_2 terminals.
* Counter enabled by T=1. out put of each flip flop toggles for every transition of its clock i/p (0 to 1 change)

* $\bar{Q}$ of every flip flop connected to clock i/p of the next stage.

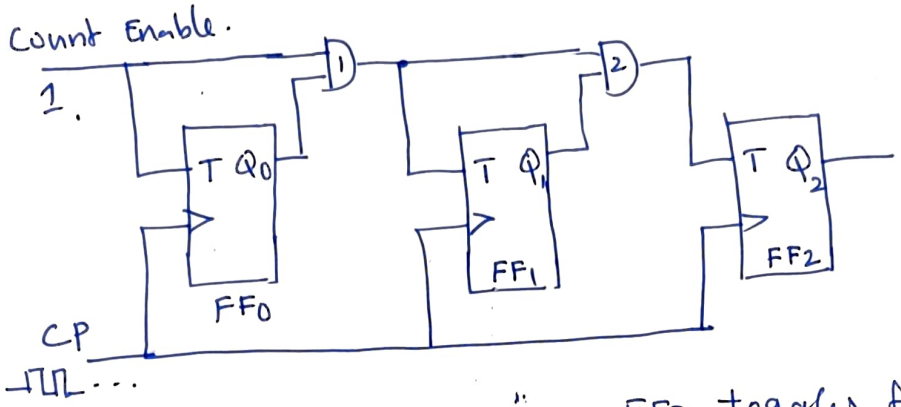


* FF_0 toggles at every positive edge of every clock i/p.
* $\bar{Q}_0$ is connected to CP of FF_1 so falling edge of Q_0 toggles Q_1
* $\bar{Q}_1$ is connected to CP of FF_2, falling edge of Q_1 toggles Q_2.
* out put is taken from Q_0, Q_1 & Q_2 so it starts with 000 from first clock pulse and continues up to 111 consecutively by following clock pulses.
* once count reaches to 111 next clock pulse makes all out put to 000.

Synchronous Binary Counter

* clock pulses are connected together & applied simultaneously to all flip flops in cascade.
* It reduces the effect of Propagation delay.
* Propagation delay is not cumulative like in Ripple counter but delay is equal to delay of 1 f/f and connecting gates.

Modulo 8 synchronous counter



FF0 toggles from 0 to 1,

* If count Enable line is 1. AND, gate o/p place a 1 at T i/p of FF_0, and
* First clock pulse makes Q_0 toggles and AND, o/p goes 1.
* second flip flop toggles at second clock pulse, AND_2 goes 1
* Third flip flop toggles at Third clock pulse. and next clock pulse automaticall Q o/p's resets.
* This counter produces o/p sequences from 000 to 111
* synchronous counter has minimum propagation delay.