

OPERATING SYSTEM

Multilevel Paging

Why Multilevel Paging is Needed

In simple paging, **each process has a single page table**.

For large address spaces (e.g., 32-bit or 64-bit systems), this page table becomes **very large** and wastes memory.

👉 Multilevel paging solves this problem by breaking the page table into smaller tables.

Definition

Multilevel paging is a memory management technique in which the **page table itself is divided into multiple levels**, and address translation is done through a **hierarchy of page tables**.

Only the required page tables are kept in memory, reducing memory overhead.

Basic Idea (Simple Explanation)

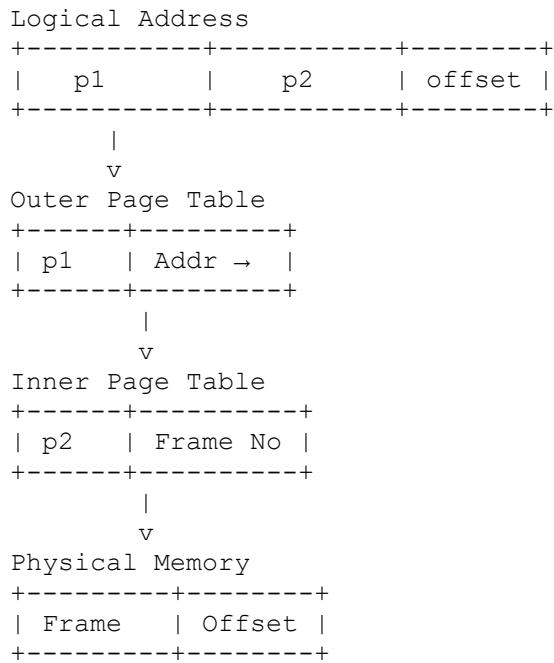
- Logical address is divided into **multiple parts**
- Each part indexes a **level of page table**
- Final level gives the **frame number**
- Offset remains unchanged

Logical Address Format (Example: Two-Level Paging)

+-----+	+-----+	+-----+	+-----+
Page No 1	Page No 2	Offset	
+-----+	+-----+	+-----+	+-----+

- **Page No 1** → Index to outer page table
- **Page No 2** → Index to inner page table
- **Offset** → Position inside the page

Multilevel Paging Diagram (Two-Level Paging)



Step-by-Step Address Translation

1. CPU generates a **logical address**
2. **p1** indexes the **outer page table**
3. Outer table gives address of an **inner page table**
4. **p2** indexes the inner page table
5. Inner table gives the **frame number**
6. Frame number + offset → **physical address**

Advantages of Multilevel Paging

- Reduces memory used by page tables
- Supports very large address spaces
- Only required page tables are loaded
- Efficient memory utilization

Disadvantages of Multilevel Paging

- Slower memory access (multiple table lookups)
- More complex address translation
- Requires hardware support (TLB)

Role of TLB in Multilevel Paging

- TLB stores **recent address translations**

- Reduces number of memory accesses
- Improves performance significantly

Multilevel paging is a memory management technique where the page table is divided into multiple levels. Logical address is split into multiple page numbers and an offset. Address translation is done step-by-step through these page tables, reducing memory overhead and supporting large address spaces.

One-Line Summary

 *Multilevel paging breaks a large page table into smaller tables to save memory and efficiently manage large address spaces.*