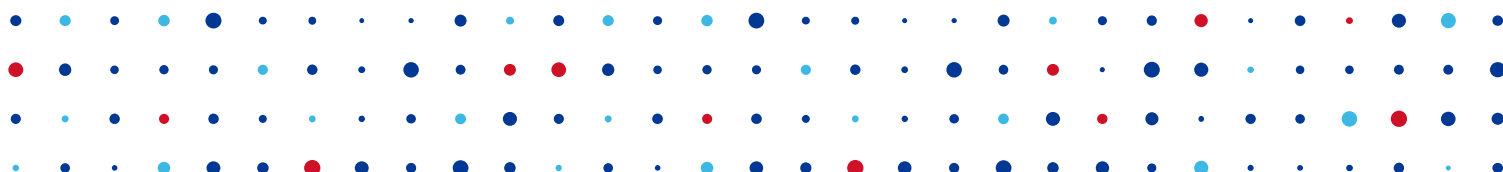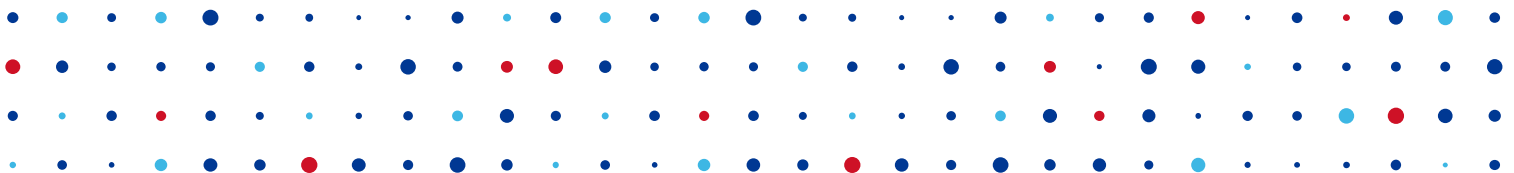# Router TURRIS
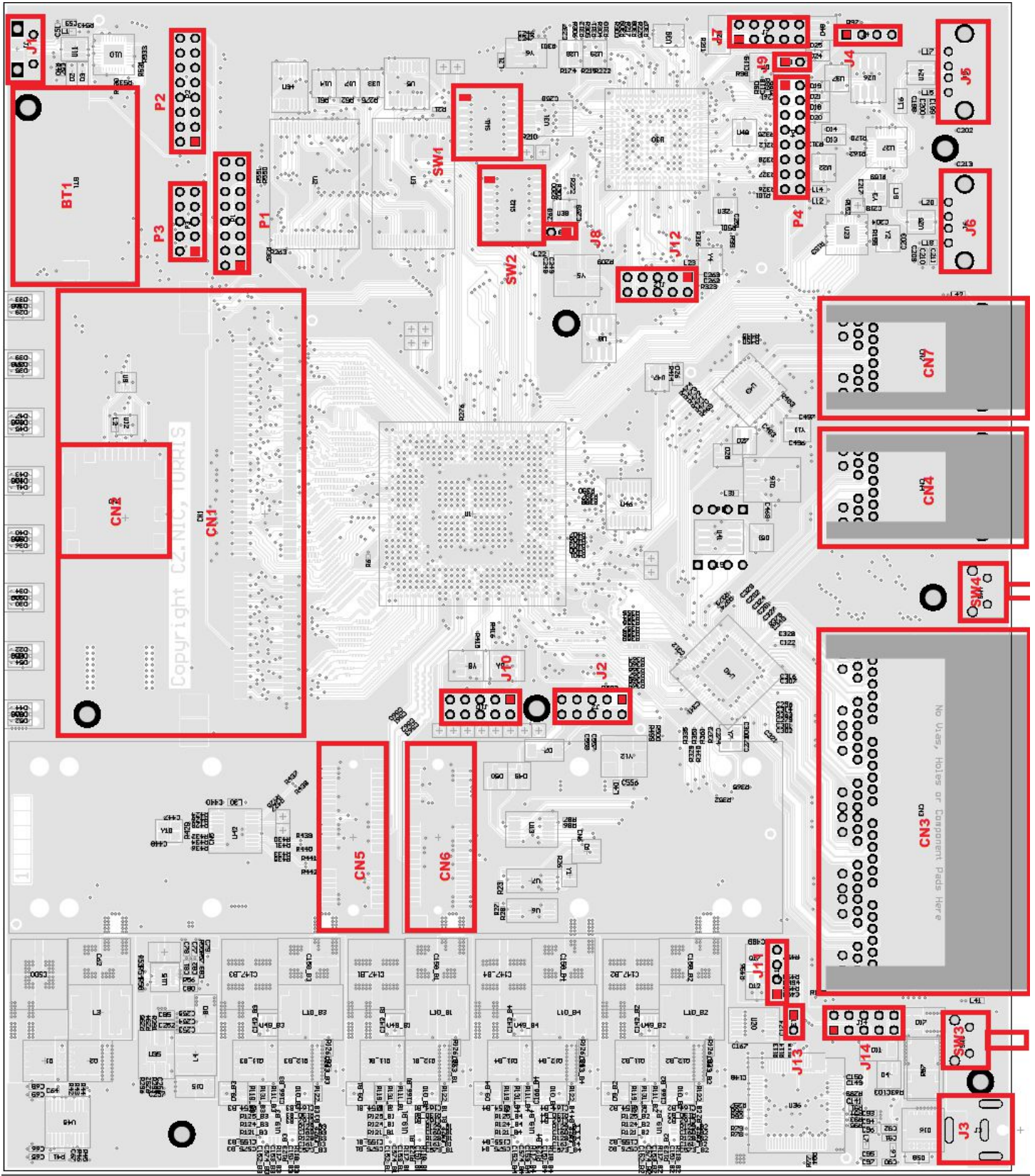
Description of connectors and DIP switches

Tomas Rykl v1.2 9.6.2014

1. PCB layout
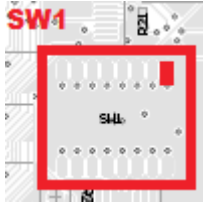
2. Connectors and DIP switches

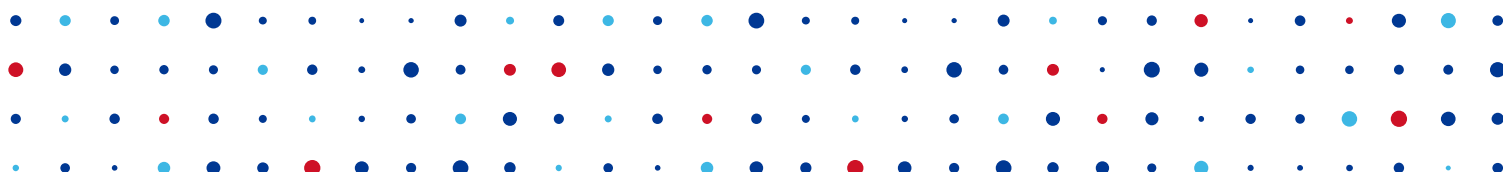| BT1	battery holder CR2032

CN1	DDR3 SODIMM

CN2	micro SD card

CN3	Ethernet LAN ports 2 to 5

CN4	Ethernet LAN port 1

CN5	mini PCIe

CN6	mini PCIe

CN7	Ethernet WAN port

J1	micro USB debug console

J3	Power supply 7,5V
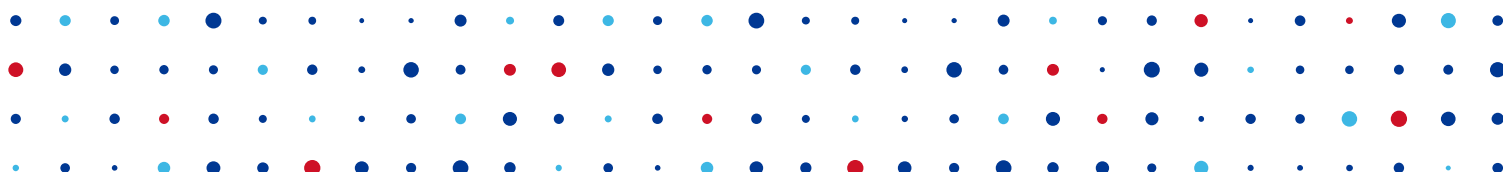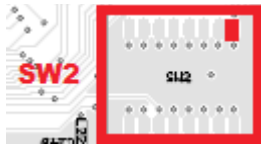
J5	USB2

J6	USB1
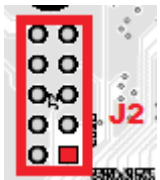
SW1	FREQUENCY AND BOOT LOCATION

SW1[1:6]	CPU FREQ.	PLATFORM FREQ.	DDR FREQ.	BOOT
011110	800	400	667	NOR
101110	800	400	800	NOR
001110	1000	500	667	NOR
110110	1000	500	800	NOR
100110	1200	600	667	NOR
000110	1200	600	667	SD/MMC
111010	1200	600	800	NAND
011010	1200	600	800	SD/MMC
101010	1200	600	800	PCIE2
001010	1200	600	800	SPI
110010	1200	600	800	NOR

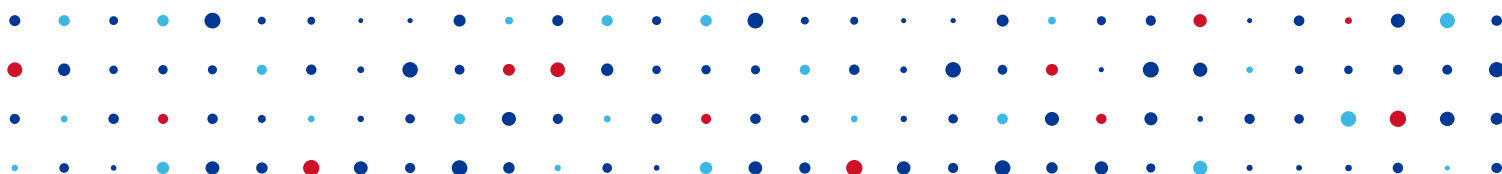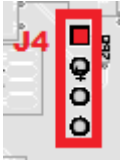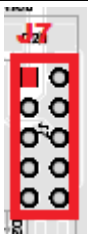| SW1[7]	LGPL (CFG_BOOT_SEQ[1])	Indicates wheather the boot sequencer is enabled during boot=up	OFF: Enables boot sequencer and information loaded from I2C ROM ON: Disables boot sequencer
SW1[8]	FBANK_SELECT	Indicates which NOR bank is selected	OFF: Uses upper 4 sectors for booting ON: Uses middle 4 sectors for booting

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SW2		Configuration options			
	SW2[1]	CFG_WIDTH	Not used		
	SW2[2]	LA18 (cfg_host_agt[1])	Controls the setting of the cfg_host_agt[1] pin	ON: cfg_host_agt[1] = 1 OFF: cfg_host_agt[1] = 0	
	SW2[3]	DMA1_DACK_N		Must be set ON for P2020	
	SW2[4]	LA19 (cfg_host_agt[2])	Controls the setting of the cfg_host_agt[2] pin	ON: cfg_host_agt[2] = 1 OFF: cfg_host_agt[2] = 0	
	SW2[5]	USB1_STP		Must be set ON for P2020	
	SW2[6]	TEST_SEL	TEST mode selection	ON: Normal operation OFF: TEST mode	
	SW2[7]	PCIE_SEL	Not used		
	SW2[8]	LWE1_N (cfg_host_agt[0])	Controls the setting of the cfg_host_agt[0] pin	ON: cfg_host_agt[0] = 1 OFF: cfg_host_agt[0] = 0	

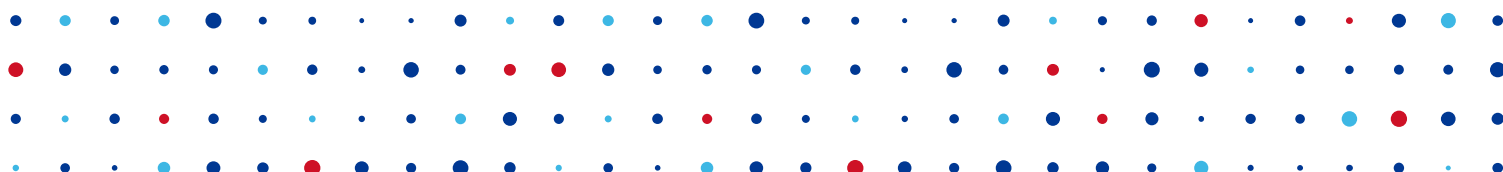| SW3	RESET push button

SW4	LED INTENSITY push button

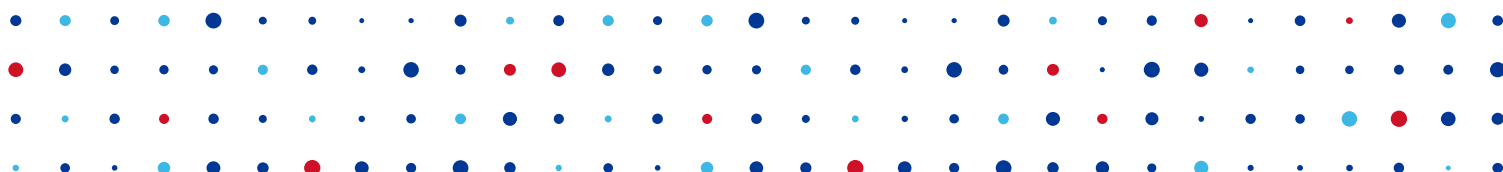| J2	I2C1 PROGRAMMING CONNECTOR
	1 I2C1_SCL 2 GND 3 PMB_CNTRL 4 GND 5 I2C1_SDA 6 3V30 CPLD 7 GPIO9/PMB_ALERTn 8 GND 9 EXTERNAL I2C1 DISCONNECT

	10 3V30 CPLD DIODE

J4	CPU FAN
	1 Power supply (7,5V) 2 TACHO 3 PWM 4 GND

J7	CPLD JTAG interface
	1 TCK 2 GND 3 TMS 4 GND 5 TDI 6 3V30_CPLD 7 TDO 8 GND 9 - 10 3V30_CPLD DIODE

J8	RESET BUTTON JUMPER
	1 GND 2 RESET

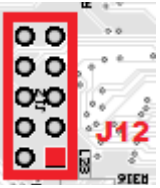| J9	Bypass
	1 C_P_BPS_OUT0 2 C_BPS_OUT0

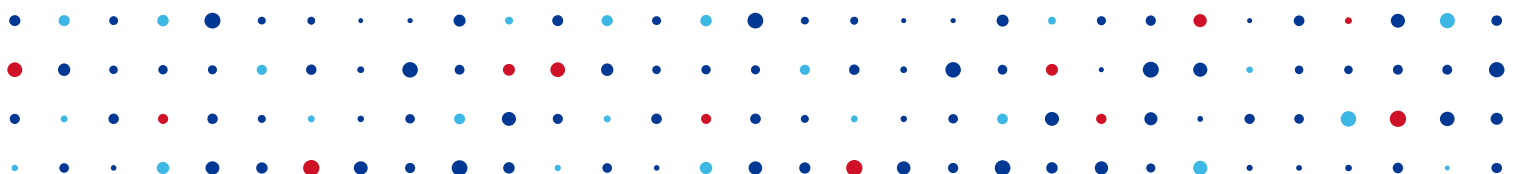| J10	CPU 1588
	1 - 2 GND 3 CPU_1588_CLK_IN 4 CPU_1588_PULSE_OUT2 5 CPU_1588_PULSE_OUT1 6 CPU_1588_CLK_OUT 7 CPU_1588_TRIGIN2 8 CPU_1588_ALARM_OUT1 9 CPU_1588_TRIGIN1 10 CPU_1588_ALARM_OUT2

J11	POWER SUPPLY FAN
	1 POWER SUPPLY (7,5V) 2 TACHO 3 PWM 4 GND

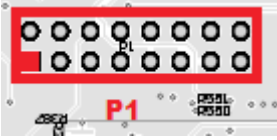| J12	CPLD not used signals
	1 3V30 CPLD 2 X2JTAG TCK 3 CFG_STROBE2 4 X2JTAG TMS 5 CFG_STROBE2A 6 X2JTAG TRST 7 X2JTAG TDI 8 XRESET# 9 X2JTAG TDO 10 GND

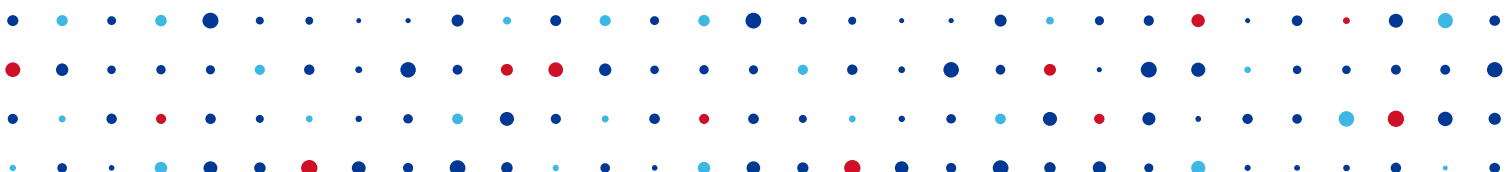| J13	POWER SUPPLY JTAG ENABLE
	1 GND 2 PM_ADDSENS0

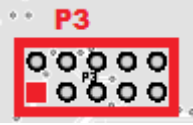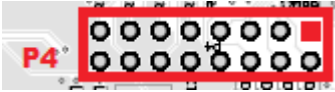| J14	POWER SUPPLY JTAG
	1 TCK 2 GND 3 TMS 4 GND 5 TDI 6 3V30 PMB 7 TDO 8 GND 9 TRCK 10 3V30 PMB DIODE

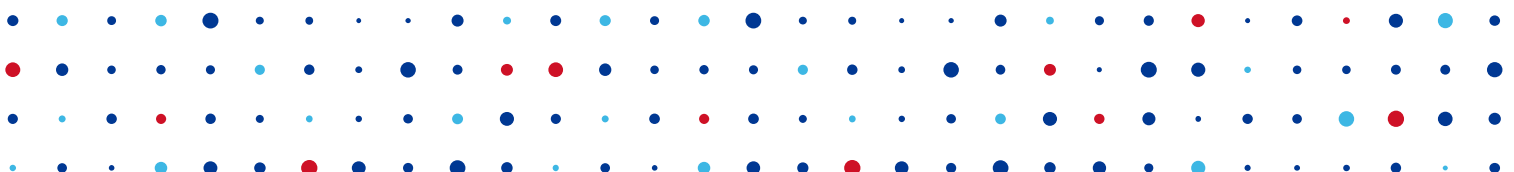| P1	UART1, SPI, I2C2
	1 3V30 PE 2 CPU_SPI_MOSI 3 CPU_UART1_SIN 4 CPU_SPI_MISO 5 CPU_UART1_SOUT 6 CPU_SPI_CLK 7 CPU_UART1_CTSn 8 CPU_SPI_CSN0_N 9 CPU_UART1_RTSn 10 CPU_SPI_CSN1_N 11 CPU_I2C2_SDA 12 CPU_SPI_CSN2_N 13 CPU_I2C2_SCL 14 CPU_SPI_CSN3_N 15 SDWIDTH 16 GND

P2	CPU JTAG
	1 CPU_TDO 2 3 CPU_TDI 4 COP_TRST_N 5 PE_COP_RUNSTOP 6 PE_COP_VSENSE 7 CPU_TCLK 8 CKSTP_IN_N

| 9 CPU_TMS |
| 10 - |
| 11 COP_SRST_N |
| 12 GND |
| 13 COP_HRST_N |
| 14 - |
| 15 CKSTPOUT_N |
| 16 GND |

P3	GPIO SIGNALS
	1 3V30 PE 2 GPIO15 3 GPIO0 4 GPIO6 5 GPIO1 6 GPIO5 7 GPIO2 resistor 8 GPIO4 9 GPIO3 10 GND

P4	CPLD not used signals
	1 3V30 CPLD 2 C_TDM_CLK_SLIC1 3 C_TDM_LA# 4 C_TDM_CLK_SLIC2 5 C_CFG_CPU_VDD0

	6 C_PCIE_SEL 7 C_CFG_CPU_VDD1 8 C_RGMII_RST# 9 C_IIC2CTL1 10 C_BPSOUT0 11 C_IIC2CTL2 12 C_QESPI IIC2# 13 C_IIC2CTL3 14 C_TDM0 UART1# 15 C_IIC2CTL4 16 GND