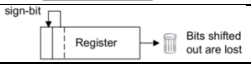
Assembly instructions - ARM V8a (simplified)

Category	Instruction	Mnemonic	Meaning	Set Flags?
Arithmetic	ADD	ADD{S} rd, rn, op2	rd = rn + op2	Yes
	CMN	CMN rd, op2	rd + op2	Yes
	CMP	CMP rd, op2	rd – op2	Yes
	NEG	*NEG{S}* rd, op2	rd = –op2	Yes*
	NGC	*NGC{S}* rd, rm	rd = –rm – ~C	Yes*
	SUB	SUB{S} rd, rn, op2	rd = rn - op2	Yes*
Logical and Mov	AND	AND{S} rd, rn, op2	rd = rn & op2	Yes*
	BIC	BIC{S} rd, rn, op2	rd = rn & ~op2	Yes*
	EON	EON rd, rn, op2	rd = rn ⊕ ~op2	
	EOR	EOR rd, rn, op2	rd = rn ⊕ op2	
	LSL	LSL rd, rn, op2		
	LSR	LSR rd, rn, rm		
	ASR	ASR rd, rn, op2		
	MOV	*MOV* rd, op2	rd = op2	Yes
	MVN	*MVN* rd, op2	rd = ~op2	
	ORN	ORN rd, rn, op2	rd = rn | ~op2	
	ORR	ORR rd, rn, op2	rd = rn | op2	
	ROR	*ROR* rd, rn, op2		
	TST	*TST* rn, op2	rn & op2	Yes
Branch	B	B{cc} target	If (cc) jump to target	
	CBNZ	CBNZ rd, target	if (rd≠0) jump to target	
	CBZ	CBZ target	if (rd=0) jump to target	
Load and Store	LDR	LDR rt, [addr]	rt = Mem[addr]	
	STR	STR	Mem[addr] = rt	

Notes:

- {S} is the set bit. If present, Flags will be set.
- op2: register or immediate
- rd, rn, rm: W or X registers

Condition code (cc)) suffixes					
Suffix	**Flags**	**Meaning**	**Suffix**	**Flags**	**Meaning**
EQ	Z = 1	Equal	VC	V = 0	No overflow
NE	Z = 0	Not equal	HI	C = 1 and Z = 0	Higher, unsigned
CS or HS	C = 1	Higher or same, unsigned	LS	C = 0 or Z = 1	Lower or same, unsigned
CC or LO	C = 0	Lower, unsigned	GE	N = V	Greater than or equal, signed
MI	N = 1	Negative	LT	N != V	Less than, signed
PL	N = 0	Positive or zero	GT	Z = 0 and N = V	Greater than, signed
VS	V = 1	Overflow	LE	Z = 1 and N != V	Less than or equal, signed

The condition flags	
Name	**Behavior**
N	Set to 1 when the result of the operation was negative, cleared to 0 otherwise.
Z	Set to 1 when the result of the operation was zero, cleared to 0 otherwise.
C	Set to 1 when the operation resulted in a carry, cleared to 0 otherwise.
V	Set to 1 when the operation caused overflow, cleared to 0 otherwise.