CPE301 – SPRING 2025

Design Assignment 3

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Primary Github address: <https://github.com/CaFu0320>

Directory: <https://github.com/CaFu0320/submission_da/tree/main/DesignAssignments/DA3>

Video Playlist: <https://youtube.com/playlist?list=PLa3xS6s509hiDecTLktQ7m7s623c5CIqA&si=bn_1aSdc2Qvaoy2E>

Submit the following for all Labs:

1. In the document, for each task submit the modified or included code (only) with highlights and justifications of the modifications. Also, include the comments.
2. Use the previously create a Github repository with a random name (no CPE/301, Lastname, Firstname). Place all labs under the root folder ESD301/DA, sub-folder named LABXX, with one document and one video link file for each lab, place modified asm/c files named as LabXX-TYY.asm/c.
3. If multiple asm/c files or other libraries are used, create a folder LabXX-TYY and place these files inside the folder.
4. The folder should have a) Word document (see template), b) source code file(s) and other include files, c) text file with youtube video links (see template).

1. **COMPONENTS LIST AND CONNECTION BLOCK DIAGRAM w/ PINS**

* ATMEGA328PB MINI BOARD
* 3 FEMALE TO FEMALE CABLE
* LOGIC ANALYZER
* ARDUINO SHIELD

1. **C CODE TASK 1 a, b and c TOGETHER**

/\*

\* DA3allofthecodescombined.c

\*

\* Created: 3/26/2025 8:21:33 PM

\* Author : Carlos Funes

\*/

#define *F\_CPU* 8000000UL

#include <avr/io.h>

#include <avr/interrupt.h>

volatile *uint16\_t* timer3\_counter = 0; //counter for Timer3 interrupts

volatile *uint16\_t* timer4\_counter = 0; //counter for Timer4 interrupts

int main(void) {

//configuring Timer0 for 0.125ms delay

DDRB |= (1 << PB5); //PB5 as output

TCCR0A = 0; //normal mode

TCNT0 = 0x83; //initial value for 125us overflow

TCCR0B |= (1 << CS01); //prescaler 8

*uint16\_t* timer0\_counter = 0; //software counter for overflows

//configuring Timer3 for 0.25ms interrupts

DDRB |= (1 << PB4); //PB4 as output

TCCR3A = 0; //normal port

TCCR3B = (1 << WGM32) | (1 << CS31) | (1 << CS30); //CTC mode, prescaler 64

OCR3A = 30; //compare match value for ~0.248ms

TIMSK3 |= (1 << OCIE3A); //enable compare match interrupt

//configuring Timer4 for 0.1ms interrupts (Normal mode, PB3 LED)

DDRB |= (1 << PB3); //PB3 as output

TCNT4 = 0xFF9C; //preload for 100us overflow (65436)

TCCR4A = 0; //normal mode

TCCR4B = (1 << CS41); //prescaler 8

TIMSK4 |= (1 << TOIE4); //enable overflow interrupt

sei(); //global interrupts

while (1) {

//polling Timer0 overflow flag

if (TIFR0 & (1 << TOV0)) { //checking overflow flag

TIFR0 = (1 << TOV0); //clearing flag

timer0\_counter++;

if (timer0\_counter >= 12000) {

PORTB ^= (1 << PB5); //toggling PB5 every 1.5s

timer0\_counter = 0; //reseting counter

}

}

}

}

//Timer3 toggling PB4 every 2 seconds

ISR(TIMER3\_COMPA\_vect) {

timer3\_counter++;

if (timer3\_counter >= 16128) { //this works 2 seconds

PORTB ^= (1 << PB4); //toggling PB4

timer3\_counter = 0; //reseting counter

}

}

//Timer4 toggling PB3 every 1 second

ISR(TIMER4\_OVF\_vect) {

TCNT4 = 0xFF9C; //reloading preload value

timer4\_counter++;

if (timer4\_counter >= 20000) { //this works 1 second

PORTB ^= (1 << PB3); //toggling PB3

timer4\_counter = 0; //reseting counter

}

}

**A screenshot of a computer

AI-generated content may be incorrect.**

1. **SCHEMATIC**

**A computer screen shot of a circuit board

AI-generated content may be incorrect.**

1. **SCREENSHOTS OF EACH TASK OUTPUT (LOGIC ANALYZER)**

**PB5:**

**A screenshot of a video game

AI-generated content may be incorrect.**

**PB4:**

**A screenshot of a computer

AI-generated content may be incorrect.**

**PB3:**

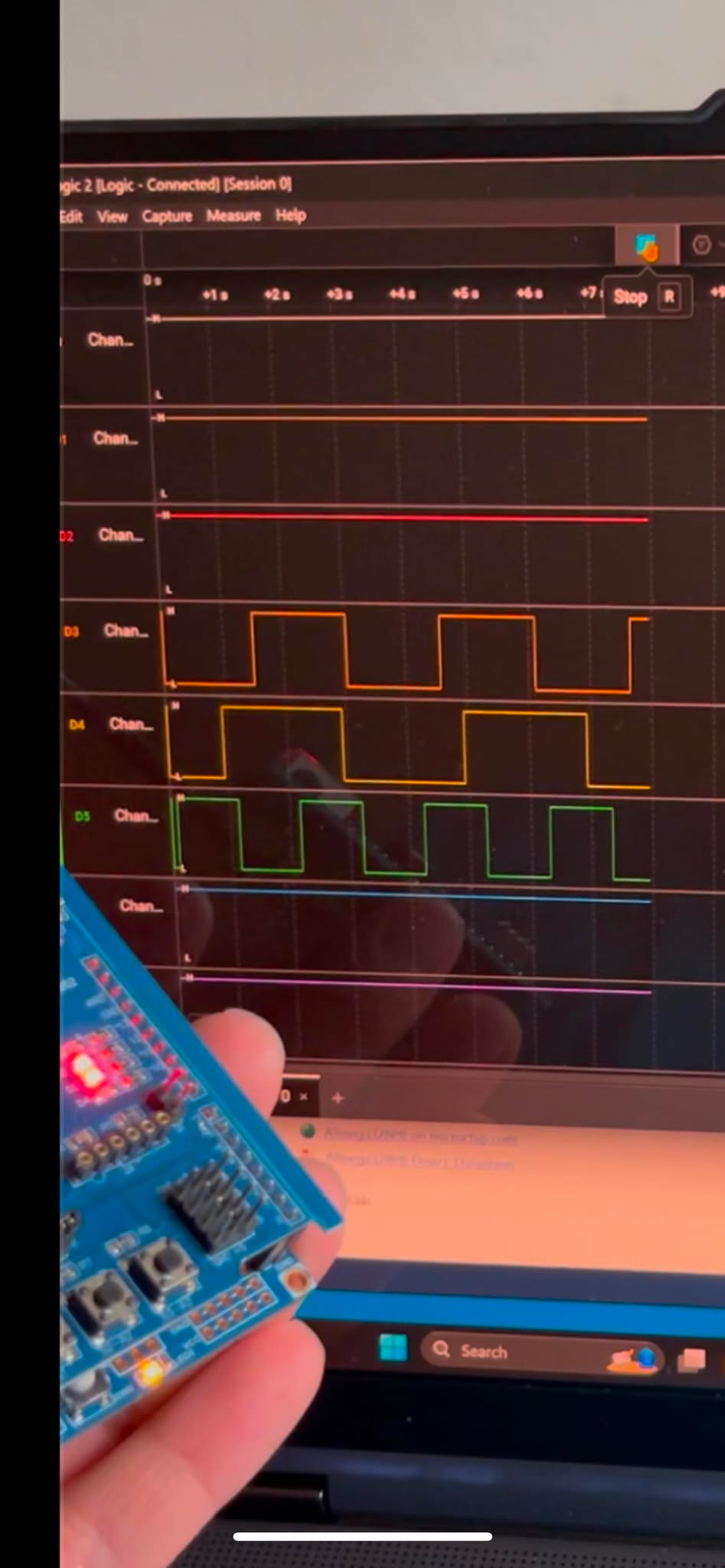
A screenshot of a computer

AI-generated content may be incorrect.

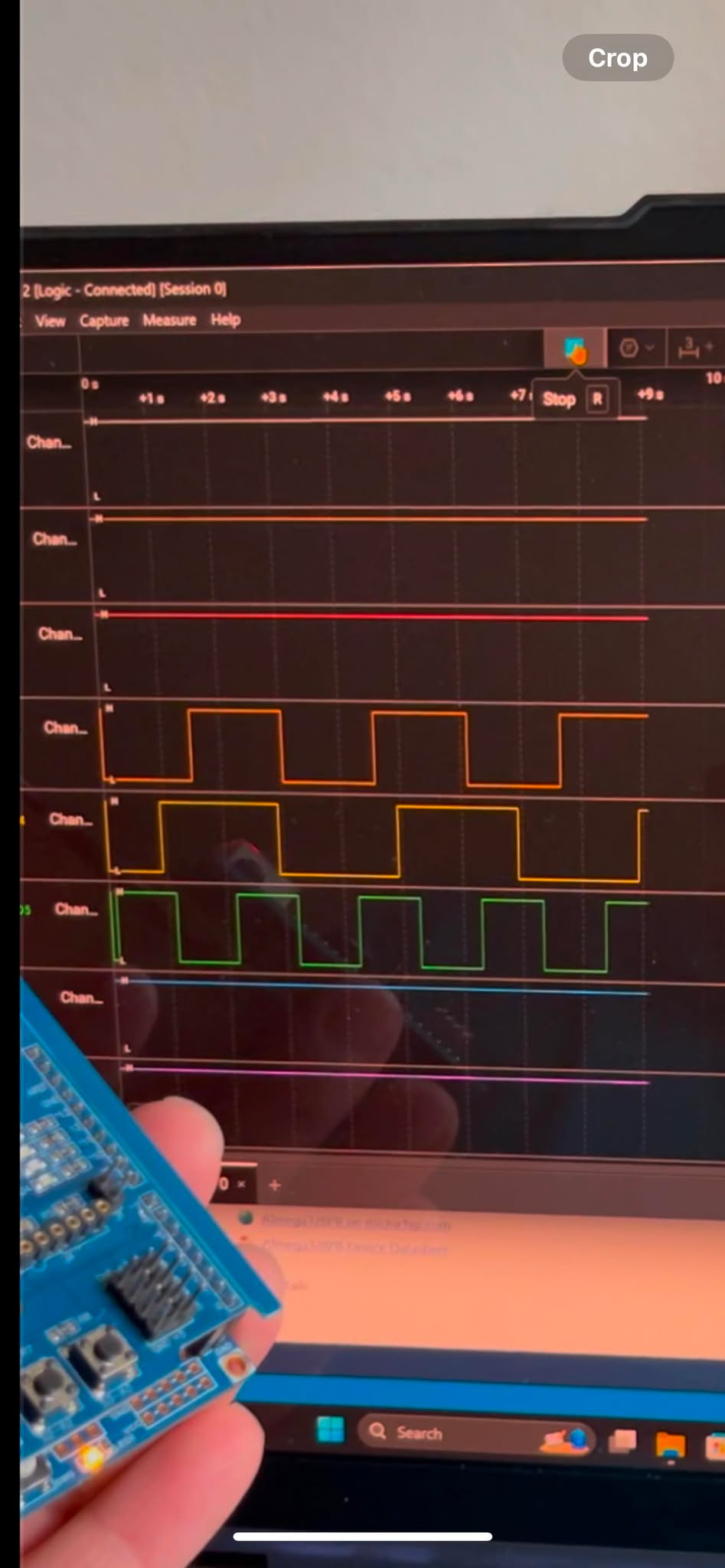
1. **SCREENSHOT OF EACH DEMO (BOARD SETUP)**

**Board Setup**

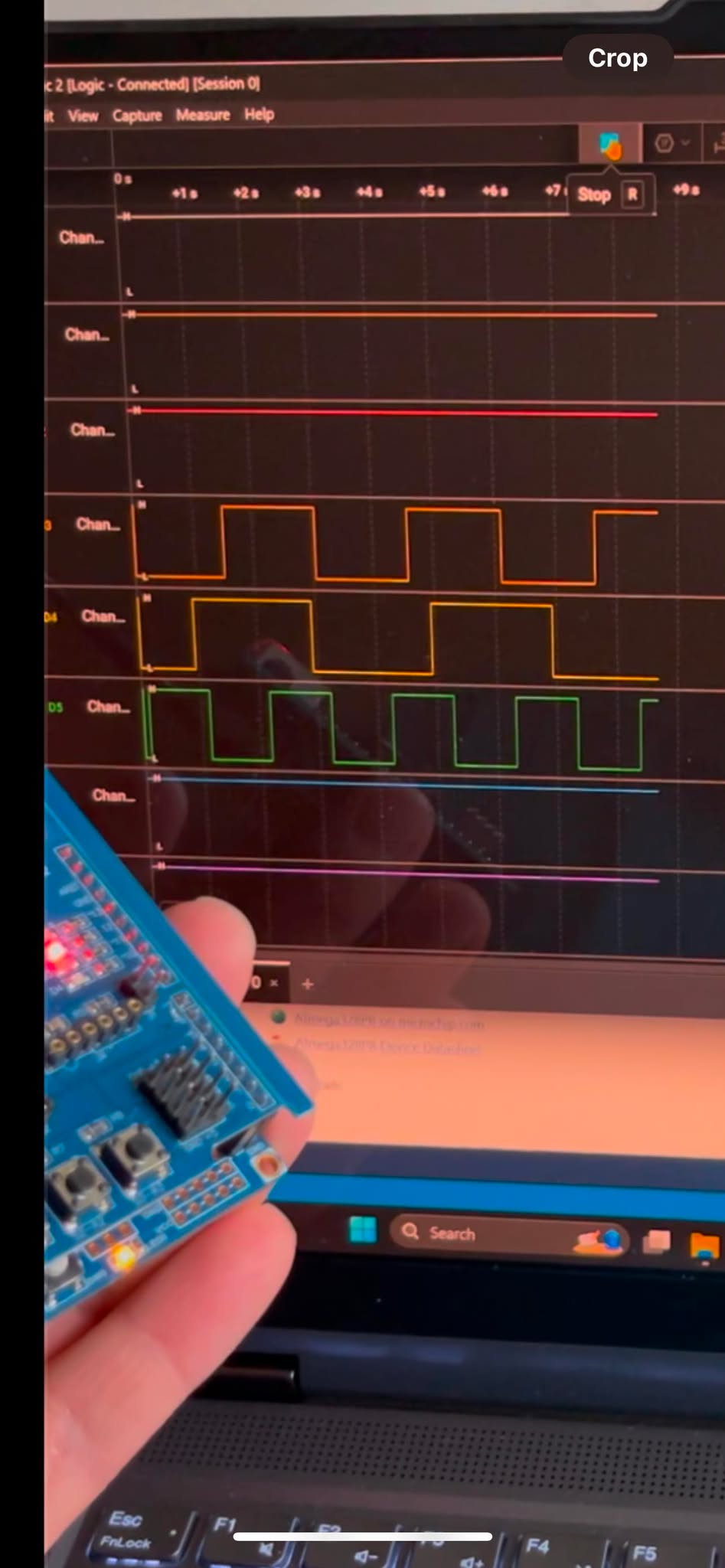
**Task 1a) PB5**



**Task 1b) PB4**



**Task 1c) PB3**



1. **VIDEO LINK FOR DEMO**

Tasks:

[**https://youtu.be/kQ49667VZCI**](https://youtu.be/kQ49667VZCI)

1. **GITHUB LINK OF THIS DA**

Tasks c code: <https://github.com/CaFu0320/submission_da/tree/main/DesignAssignments/DA3/DA3allofthecodescombined>

**Student Academic Misconduct Policy**

<http://studentconduct.unlv.edu/misconduct/policy.html>

“This assignment submission is my own, original work”.

Carlos Funes