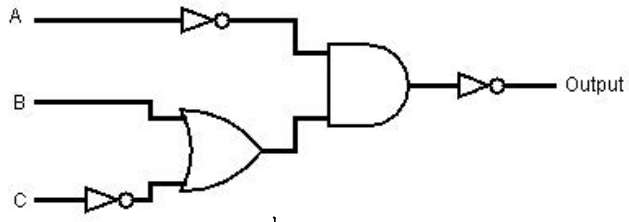
Computer Architecture Homework 4

Spring 2019, March

1 Synchronous Finite State Digital Machine Systems

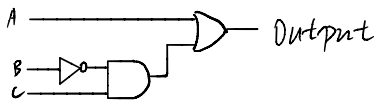
a. The circuit shown below can be simplified. Write a Boolean expression that represents the function of the simplified circuit using the minimum number of AND, OR, and NOT gate.



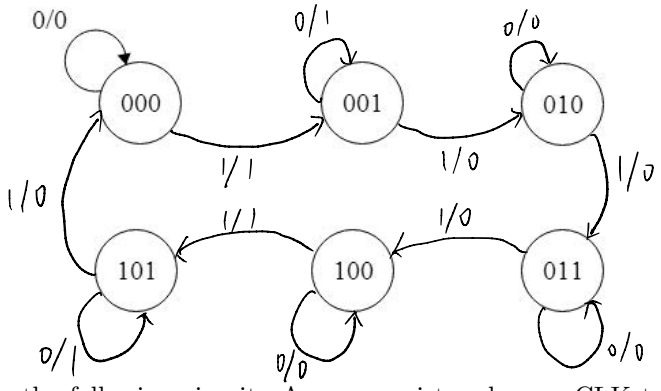
The circuit is equivalent to:

$$\overline{\bar{A}(B+\bar{C})} = A+\overline{(B+\bar{C})} = A+\bar{B}C$$

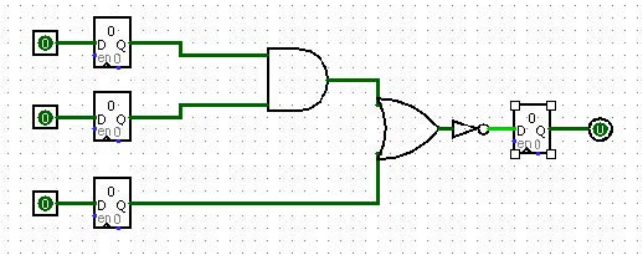
This boolean expression only uses three AND, OR, NOT gates.
i.e. the corresponding circuit diagram below



b. Consider the finite state machine below which has 6 states and a single input that can take on the value of 0 and 1. The finite state machine should output 1 IF AND ONLY IF 6 + sum of all the input values is not divisible by 2 or 3. One transition has been provided; complete the remainder of the diagram. (Hint: If the sum of the inputs is a multiple of 6, then we have 6 + sum of the inputs = 6n for some n. As 6n is divisible by 2, 6n cannot be prime.)



c. Consider the following circuit. Assume registers have a CLK to Q time of 60ps, a setup time of 40ps, and a hold time of 30ps. Assuming that all gates have the same propagation delay, what is the maximum propagation delay each individual gate could have to achieve a clock rate of 1 GHz.



Since digital signals can propagate simultaneously, the propagation delay on the critical path is the maximum delay.

Consider the path where three gates are passed through.

$60ps + 40ps + 3t = 1/1GHz$

$t = 300PS$

2 Boolean Logic

1. Simplify each Boolean expression to one of the following ten expressions:
$0, 1, A, B, AB, A + B, \overline{A}\ \overline{B}, \overline{A} + \overline{B}, A\overline{B}, \overline{A}B$
Each answer may be used as many times as necessary.

a. $A(A + \overline{A}) + B$

$A(A+\bar{A})+B = AA + A\bar{A} + B = A + 0 + B = A+B$

b. $(A + B)(\overline{A} + B)\overline{B}$

$(A+B)(\bar{A}+B)\bar{B} = (A\bar{A} + \bar{A}B + AB + BB)\bar{B} = (\bar{A}B + AB + B)\bar{B}$

$= (\bar{A} + A + 1)\bar{B}B = 0$

c. $\overline{\overline{A} + \overline{B}}$

$\overline{\bar{A}+\bar{B}} = \bar{\bar{A}}\,\bar{\bar{B}} = AB$ (By DeMorgan's Law)

2. Simplify the following expression step by step (as simple as possible):

a. Standard: $(A + B)(A + \overline{B})C$

$(A+B)(A+\bar{B})C = (AA + AB + A\bar{B} + B\bar{B})C = (A + AB + A\bar{B})C$

$= AC + AC(B + \bar{B}) = AC$

b. Grouping & Extra Terms: $\overline{A}\ \overline{B}\ \overline{C} + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}\ \overline{C} + ABC + A\overline{B}C$

$(\bar{A}\bar{B} + \bar{A}B + AB + A\bar{B})\bar{C} + (AB + A\bar{B})C$

$= [\bar{A}(\bar{B}+B) + A(B+\bar{B})]\bar{C} + AC(B+\bar{B})$

$= (\bar{A}+A)\bar{C} + AC = \bar{C} + AC = A + \bar{C}$

c. DeMorgan's: $\overline{A(\overline{B}\ \overline{C} + BC)}$

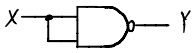
$\overline{A(\bar{B}\bar{C} + BC)} = \bar{A} + \overline{(\bar{B}\bar{C} + BC)} = \bar{A} + (\overline{\bar{B}\bar{C}}\ \overline{BC})$

$= \bar{A} + [(B+C)(\bar{B}+\bar{C})] = \bar{A} + (B\bar{B} + C\bar{B} + B\bar{C} + \bar{C}\bar{C})$

$= \bar{A} + \bar{B}C + \bar{C}B$

3 Logic Gates

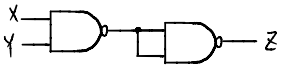
a. Create a NOT gate using only NAND gates.



X	Y
0	1
1	0

b. Create an AND gate using only NAND gates. (Hint: use a)

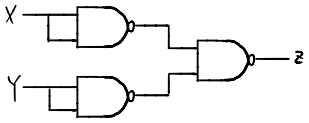
$$XY = \overline{\overline{XY}}$$



X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

c. Create an OR gate using only NAND gates.

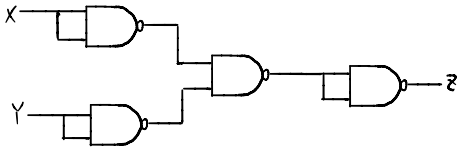
$$X + Y = \overline{\overline{X}\,\overline{Y}}$$



X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

d. Create a NOR gate using only NAND gates. (Hint: use a & c)

$$\overline{X+Y} = \overline{\overline{X}\,\overline{Y}}$$



X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0