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Computer Architecture Homework 6

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Instructions:

Homework 6 is due in May. 6, covers the content of caches and float-points, please refer to the lecture slides. You can print it out and write on it, and scan it into a pdf, or you can take photos or write Latex if you want, just remember: you must create a **PDF** and upload to the **Gradescope**, please assign the questions properly on Gradescope, otherwise you will lose 25% of points.

Tell us your feeling after finish it. Thank you!

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Question Set 1. Direct Mapped Cache

[30 points] In a 16-bit byte-addresses machine, the clock frequency is 3GHz. We have a cache with properties as follows:

1. Cache size is 64 Bytes;
2. Block size is 4 Bytes;
3. Cache hit time is 2 cycles;
4. Cache miss penalty is 100 cycles;

1-A. What the width of each field of following address bit assignment:

TAG: 10	Set index: 4	Block offset: 2

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

① offset: 2 bits. 4-Byte block requires 2 bit to locate each byte.

② Index: 4 bits. There are 64/4=16 cache blocks. Due to the directed mapped cache, the number of sets is 16, which requires 4 bits to index.

③ TAG: the rest 10 bits.

1-B. We will access the data of addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.)

(Apply LRU replace policy)

Addresses (serially access)	Tag/Index	Hit, Compulsory or Replace
0x0000	0 / 0	Compulsory
0x0004	0 / 1	Compulsory
0x0008	0 / 2	Compulsory
0x000c	0 / 3	Compulsory
0x1000	64 / 0	Replace
0x1004	64 / 1	Replace
0x1008	64 / 2	Replace
0x100c	64 / 3	Replace
0x0000	0 / 0	Replace
0x0004	0 / 1	Replace

1-C. Calculations. (Step-by-step, worth 50% pts)
1-C-i: Miss rate: (4 pt.)

100%. No hit at all.

1-C-ii: AMAT (ns): (3 pt.)

$(2 + 100\% \times 100) \times \frac{1}{3\text{GHz}} = 34\ \text{ns}$

1-C-iii: AMAT if we don't have this cache (ns): (3 pt.)

$100 \times \frac{1}{3\text{GHz}} = 33.3\ \text{ns}$

(No hit time)

Question Set 2. Two-Way Set Associative Cache

From QS 1. We change the block size to 8 Bytes and implemented a two-way set associative cache. The parameters are shown as follows:

1. Cache size is 64 Bytes;
2. 16-bit byte-addresses machine;
3. Block size is 2 words;

2-A. What is the width of each field of following address bit assignment? :

TAG: 11	Set index: 2	Block offset: 3

Please show the procedure that your solutions derive from.
Answer 6pt + Analysis 4pt

① offset : 3 bits. 8-Byte cache block requires 3 bits to locate each byte.
② Index : 2 bits. There are 64/8 = 8 cache blocks. Due to the associativity is 2, there are 4 sets, and 2 bits are required to index
③ TAG: the rest 11 bits.

2-B. We will access the data of the addresses as follows. Fill in the blanks. It is about the index, tag (in decimal) and whether there is a hit or miss. If there is a miss, then give what type is the miss (either compulsory or replace). (Here we define replace as either conflict or capacity that causes a miss.) (Apply LRU replace policy)

Addresses (serially access)	Tag/Index	Hit, Compulsory or Replace
0x0000	0 / 0	Compulsory
0x0004	0 / 0	Hit
0x0008	0 / 1	Compulsory
0x000c	0 / 1	Hit
0x1000	128 / 0	Compulsory
0x1004	128 / 0	Hit
0x0000	0 / 0	Hit
0x0100	8 / 0	Replace
0x0000	0 / 0	Hit
0x1004	128 / 0	Replace

2-C. Calculations.
2-C-i. Miss rate: (5 pt.)

$5/10 = 50\%$

2-C-ii. Assume the new cache miss time is 200 cycles and hit time is 3 cycles. Calculate the AMAT in ns. Round to the nearest tenth. (5 pt.)

$\frac{1}{3\text{GHz}}(3 + 200 \times 50\%) = 34.3\ ns$

Question Set 3. Floating Point Numbers

We consider the IEEE 32-bit floating point representation except with a 7-bit exponent (bias of 63) and a denorm implicit exponent of -62.
3-A. Convert `-95.2` to that form. In hexadecimal.

$95 \Rightarrow (1011111)_2$ $0.2 \Rightarrow (0.0011\ 0011\ 0011\ 0011\ 00)_2$
$\therefore 95.2 \Rightarrow (1.0111110011\ 0011\ 0011\ 0011\ 00)_2 \times 2^{(110)_2}$
$\therefore$ exponent : $(63+6) = 69 \Rightarrow (1000101)_2$ $\therefore$

1	1000101	01111100110011001100
sign	exponent	significand

$\therefore$ 0xC57CCCCC

3-B. Convert `0x4a23a000` into a floating point number, specify infinities as `+inf` and `-inf`, and not a number as `NaN`.

0	100 1010	0010 0011 1010 0000 0000 0000
sign	exponent	significand

∴ exponent = 74 − 63 = 11

$(1001000111010.0000\,0000\,0000)_2 \Rightarrow 2333$

3-C. What is the smallest non-infinite positive integer it CANNOT represent? (an integer is `XX.0000`). Please explain why.

Let significand is $K=(k_{24}\ k_{23}\ \cdots\ k_1)_2$, exponent is E, then
$(K+1)/2^{24}\cdot 2^E - K/2^{24}\cdot 2^E > 1$, then $E \geq 25$.
Considering the minimum case, $K=(1000\cdots0)_2$, $E=25$. The integer between numbers of significand K and K+1 cannot be represented, i.e. $2^{25}+1$

3-D. What's the smallest positive value it can represent that is not a denorm? Leave your answer as a power of 2. Please explain why.

① The exponent should be $1-63=-62$ because it's normalized.
② Putting the significand all zero minimizes the number
③ The smallest positive value which is not a denorm is 2^{-62}

3-E. What's the smallest positive value it can represent? Leave your answer as a power of 2. Please explain why.

① Leaving exponent zero, use denorms to denote small floats.
The factual exponent turns out to be $1-63=-62$
② Putting significand to $1000\cdots01_b$ minimizes the value.
③ The smallest positive value is $2^{-24}\cdot 2^{-62}=2^{-86}$