



THE CYPRUS
INSTITUTE

RESEARCH • TECHNOLOGY • INNOVATION

National Competence
Center in HPC - Cyprus

C EURO

Introduction High-Performance Computing - Dr. S. Bacchio



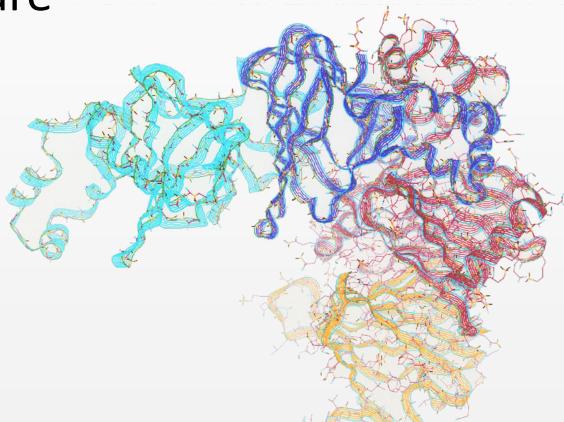
In today's talk

Introduction to High-Performance Computing

- Supercomputers in Europe, present and future
- The TOP500 list, analysis of the trends
- Co-processors: CPU vs GPU architecture
- Parallel computing



EuroHPC
Joint Undertaking



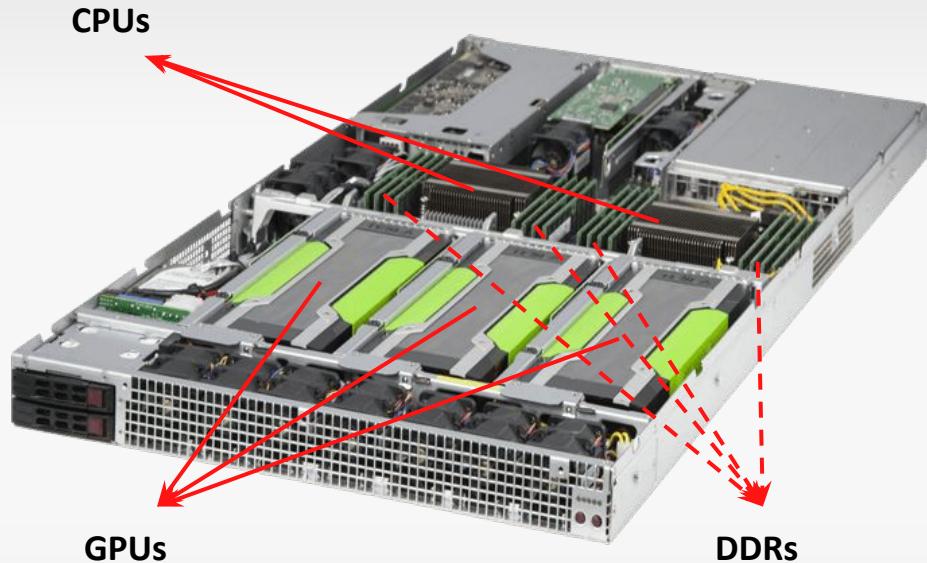
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Inside a supercomputers

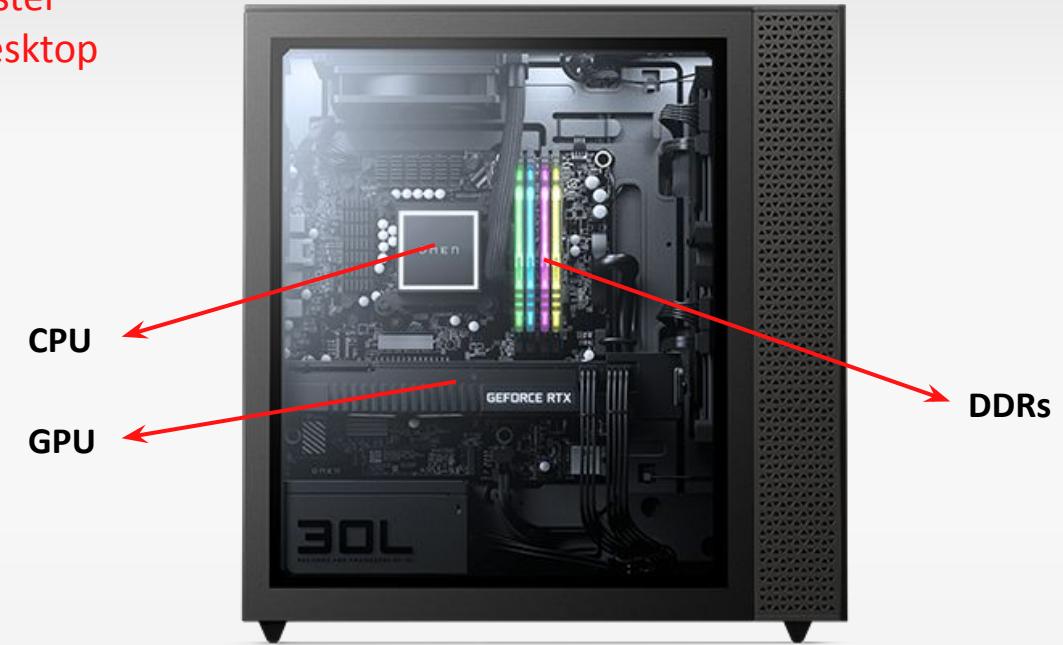
Computing Node



VS

Desktop

A node is
~5x faster
than a desktop



X no hard-drive and **X** no voltage convertor

Centralized long-term storage and power supply



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Inside a supercomputers

Computing Node



Rack



Supercomputer



- + Network
- + Storage
- + Power supply
- + Cooling



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Supercomputers in Europe



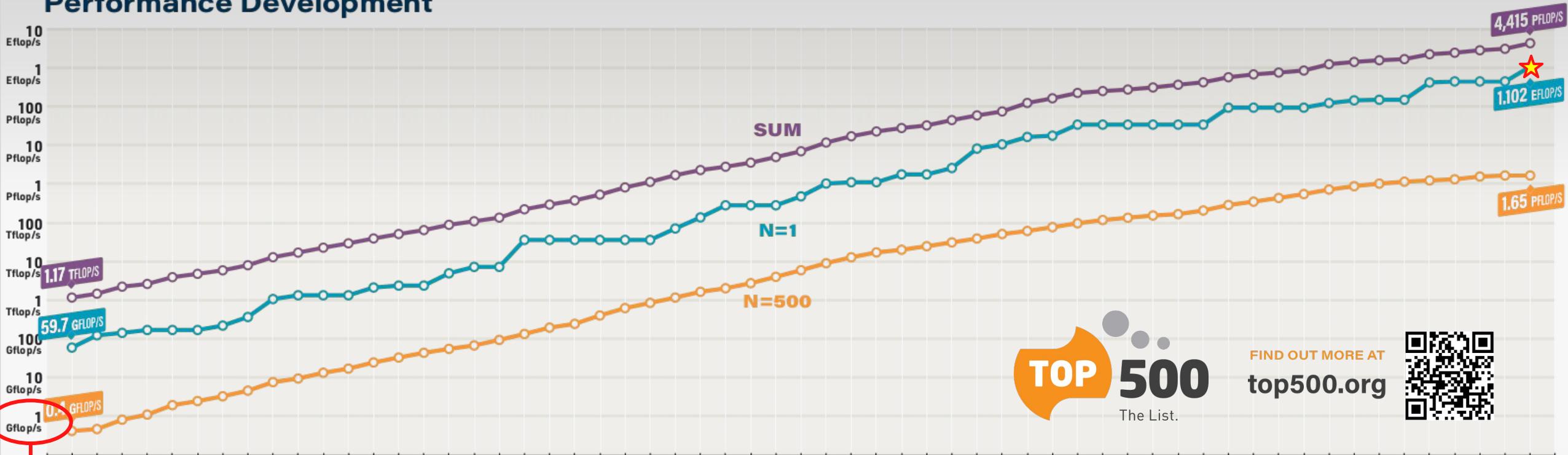


Supercomputers in Europe



TOP 500 - The List.

Performance Development



FIND OUT MORE AT
top500.org

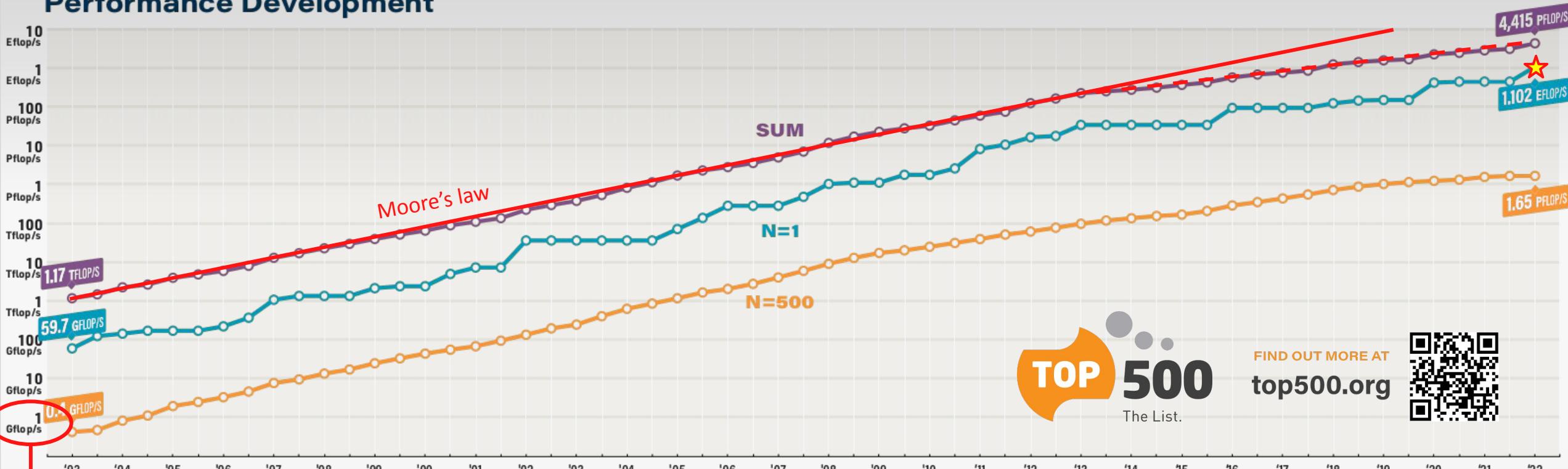


→ FLOP/s = Floating Point Operations per Second
(in double precision)

A Standard PC does about 50 Gflops (CPU) and
1 Tflops (GPU).

TOP 500 - The List.

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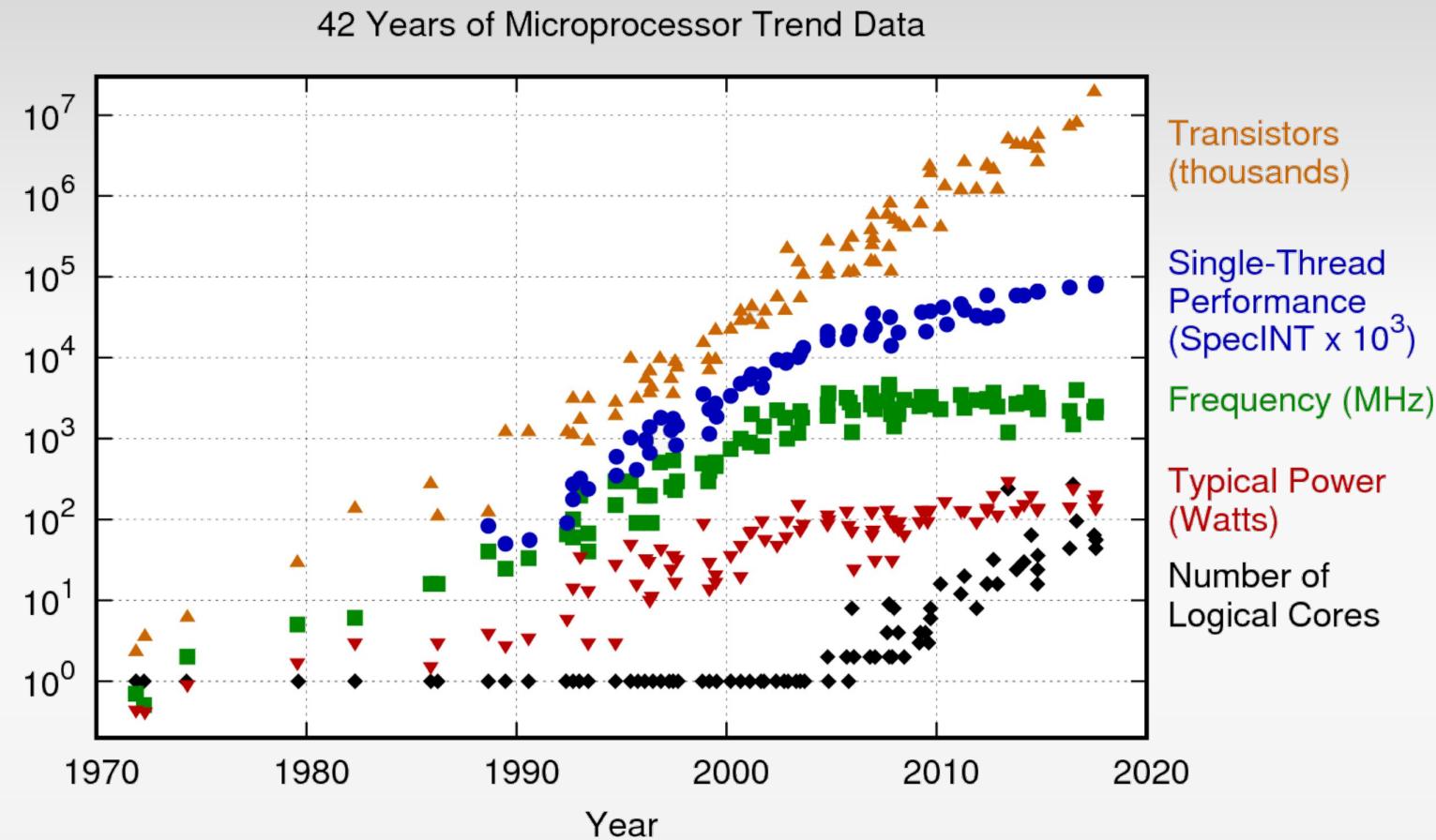


FIND OUT MORE AT
top500.org



Evolution of technology

- Exascale is a milestone in HPC since 2008:
 - DARPA, US (2008), “ExaScale Computing Study: Technology Challenges in Achieving Exascale Systems”
 - Exascale systems predicted for 2015
- It has revealed to be not only an iconic milestone but a **real challenge!**

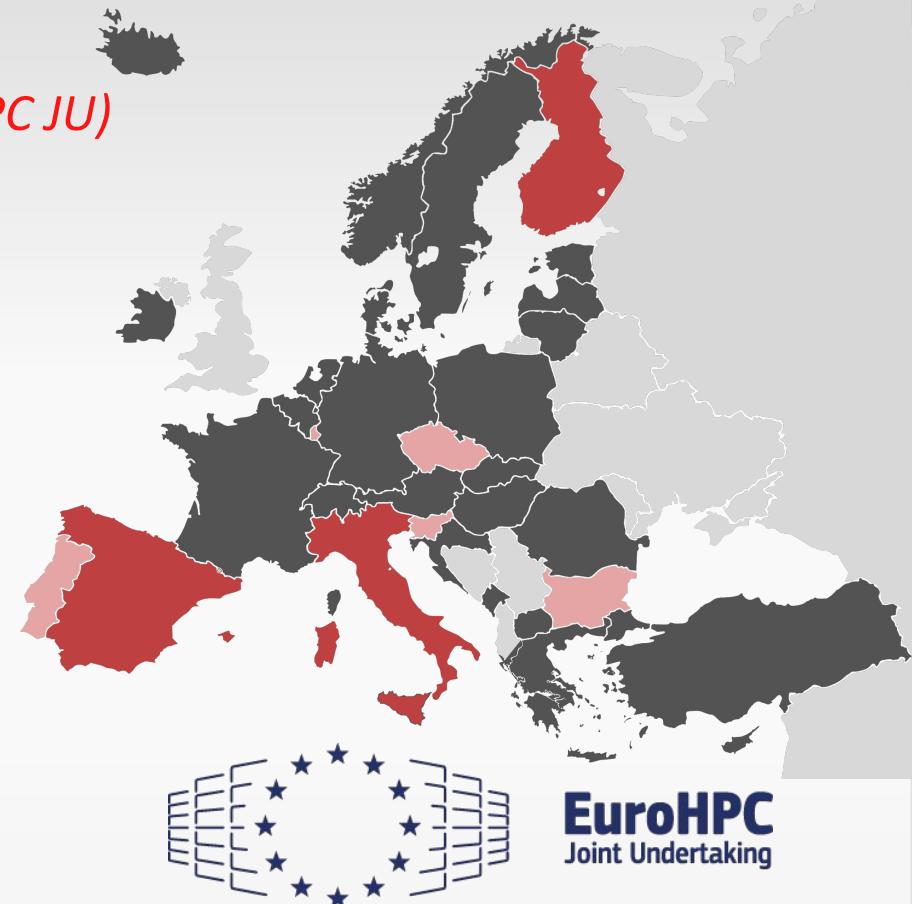


EuroHPC Joint Undertaking

The European High Performance Computing Joint Undertaking (EuroHPC JU) is pooling European resources to buy and deploy top-of-the-range supercomputers and develop innovative exascale supercomputing technologies and applications.

The JU is currently supporting two main activities:

- Developing a pan-European supercomputing infrastructure:
 - **5 PetaFlop machines** in Bulgaria, Czech, Luxembourg, Slovenia, Portugal
 - **3 Pre-Exascale machines** with over 200 PetaFlops: Lumi in Finland, Leonardo in Italy and Marenostrum 5 in Spain
 - **2 Exascale machines:** JSC in Germany, TBD



Upcoming Budget (2021 - 2033): 8 billion Euro

TOP HPC systems

JUNE 2022	SYSTEM	SPECS	SITE	COUNTRY	CORES	R _{MAX} PFLOPS	POWER MW
1	Frontier	HPE Cray EX235a, AMD Opt 3rd Gen EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-10	DOE/SC/ORNL	USA	8,730,112	1,102.0	21.3
2	Fugaku	Fujitsu A64FX (48C, 2.2GHz), Tofu Interconnect D	RIKEN R-CCS	Japan	7,630,848	442.0	29.9
3	LUMI	HPE Cray EX235a, AMD Opt 3rd Gen EPYC 64C 2GHz, AMD Instinct MI250X, Slingshot-10	EuroHPC/CSC	Finland	1,268,736	151.9	2.94
4	Summit	IBM POWER9 (22C, 3.07GHz), NVIDIA Volta GV100 (80C), Dual-Rail Mellanox EDR Infiniband	DOE/SC/ORNL	USA	2,414,592	148.6	10.1
5	Sierra	IBM POWER9 (22C, 3.1GHz), NVIDIA Tesla V100 (80C), Dual-Rail Mellanox EDR Infiniband	DOE/NNSA/LLNL	USA	1,572,480	94.6	7.44

Top European systems:

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10	Adastra	AMD EPYC (64C 2GHz), AMD Instinct MI250X, Slingshot-11	GENCI	France	319,072	46.1	0.9
11	JUWELS Booster	AMD EPYC 7402 (24C 2.8GHZ), NVIDIA A100, Mellanox HDR Infiniband	Juelich	Germany	449,280	44.1	1.8
21	Marconi-100	IBM POWER9 (16C, 3GHz), NVIDIA V100, Mellanox EDR Infiniband	Cineca	Italy	347,776	21.6	1.4
23	Piz-daint	Xeon E5-2690v3 (12C 2.6GHz), NVIDIA P100, Cray/HPE	CSCS	Switz	387,872	21.2	2.4

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Future Systems

Upcoming European systems:

			SITE	COUNTRY	PFLOP/S
2024	Jupiter	TBD (GPU-based system, NVIDIA or AMD)	JSC	Germany	1500
2023	MareNostrum5	Intel Xeon CPUs, NVIDIA Ampere A100	BSC	Spain	314
2023	Leonardo	Intel Xeon CPUs, NVIDIA Ampere A100	Cineca	Italy	250

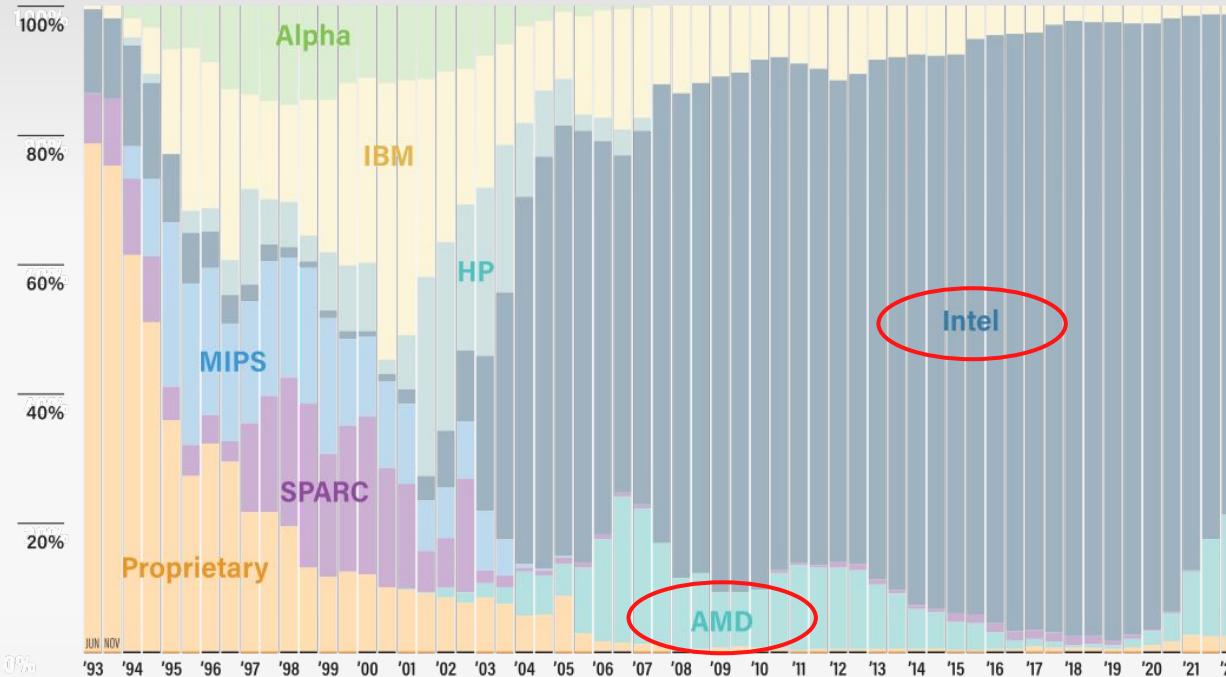
Upcoming USA systems:

			SITE	COUNTRY	PFLOP/S
2023	El Capitan	AMD Epyc CPUs, AMD Instinct GPUs	NNSA	USA	2000
2022	Aurora	Intel Xeon CPUs, Intel Xe GPUs	ALCF	USA	1000

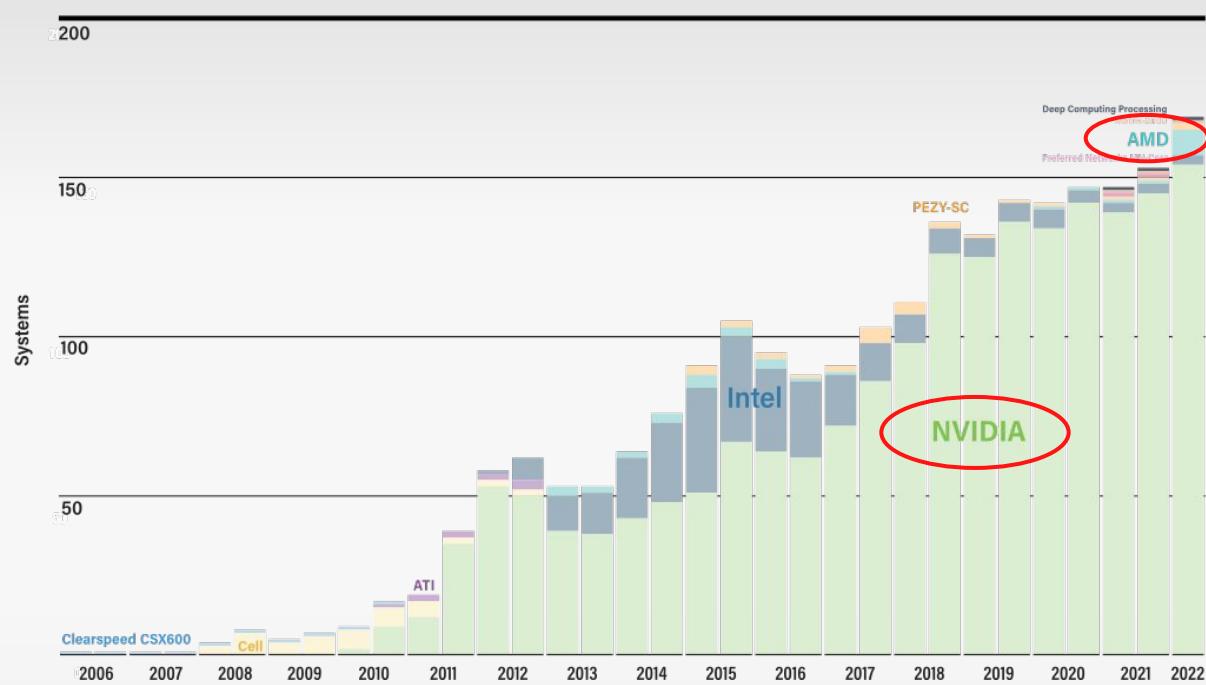
AMD and **Intel** have started only recently in producing GPUs for HPC systems
NVIDIA has dominated the market for more than 10 years

Hardware Vendors

Chip Technology



Accelerators/Co-processors



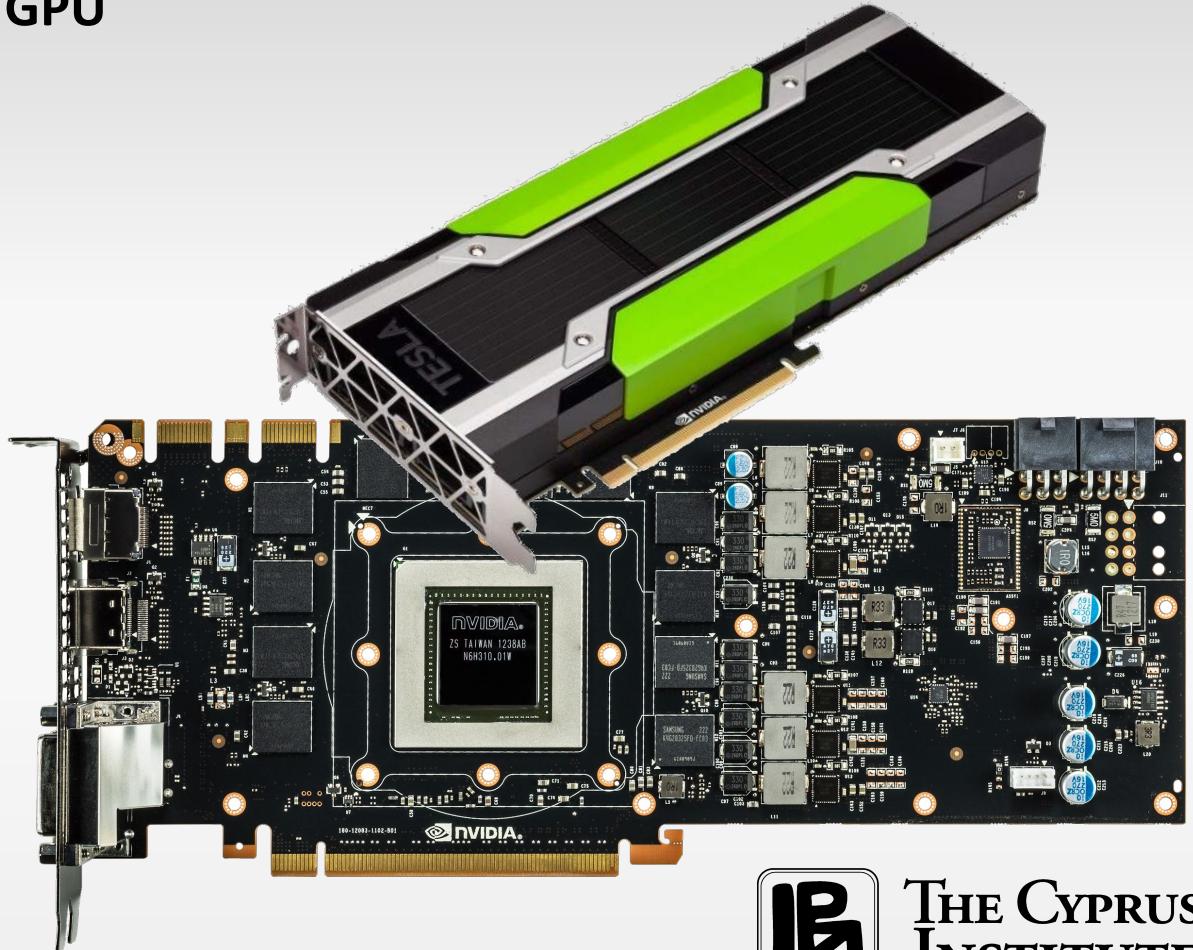


CPUs vs GPUs

CPU



GPU



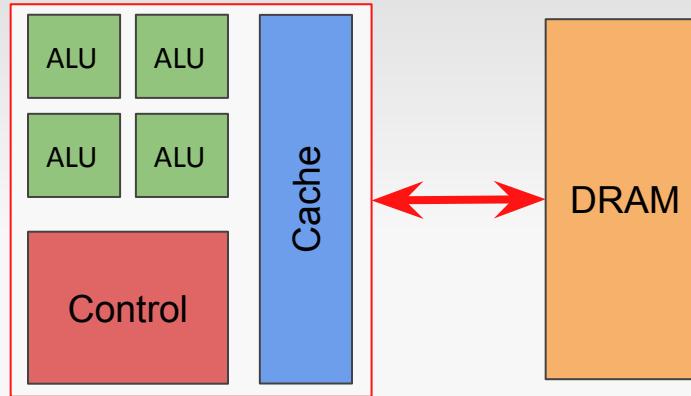
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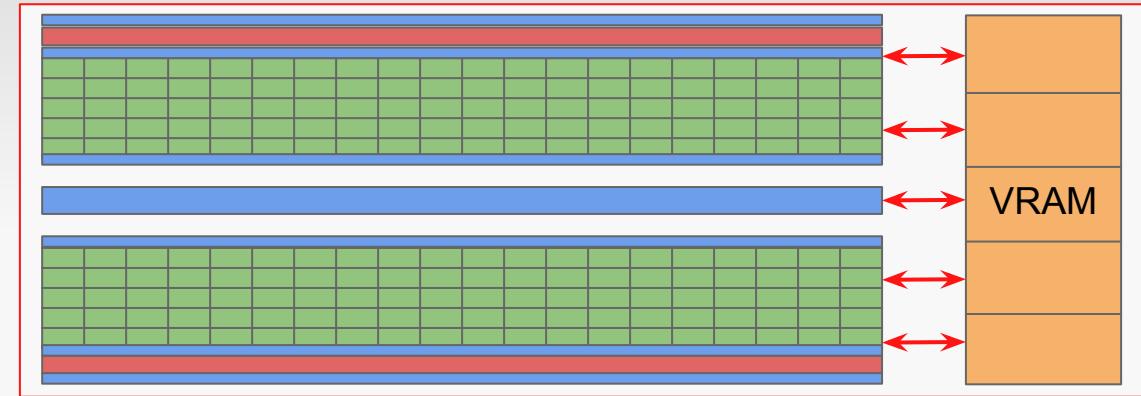


Low latency or High-throughput?

CPU



GPU

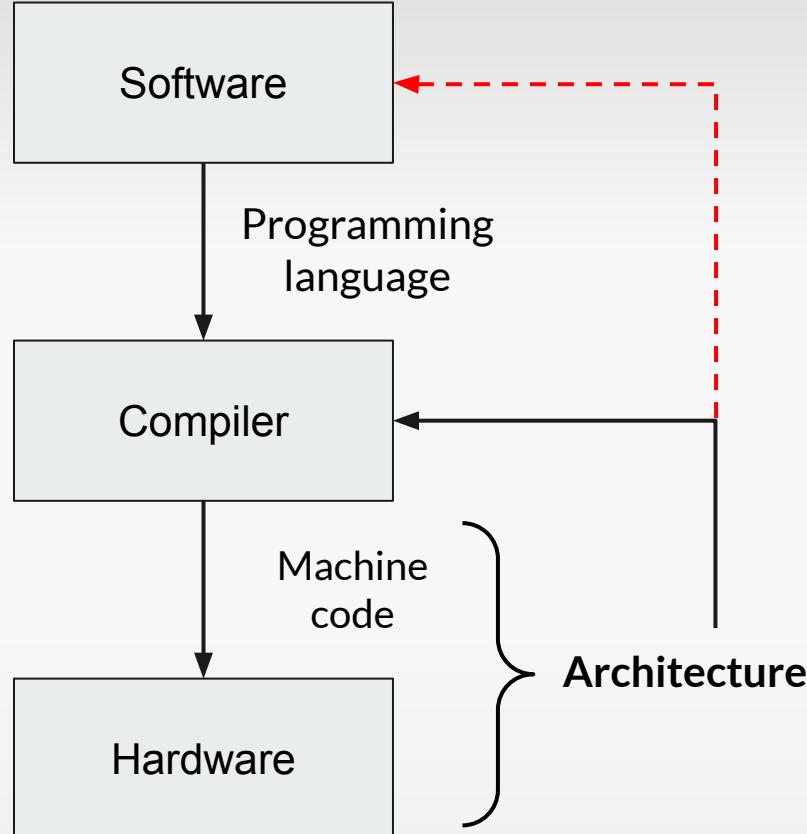


- Optimized for **low-latency access** to cached data
- Complex control logic (thousands of instructions available)
- Large caches (L1, L2, etc.)
- Optimized for serial operations
- Shallow pipelines (< 30 stages)
- Newer CPUs have more parallelism (**becoming more GPU-like**)

- Optimized for **data-parallel throughput** computation
- High latency tolerance
- High compute density per memory access
- High throughput
- Deep pipelines (hundreds of stages)
- Newer GPUs have better control logic (**becoming more CPU-like**)



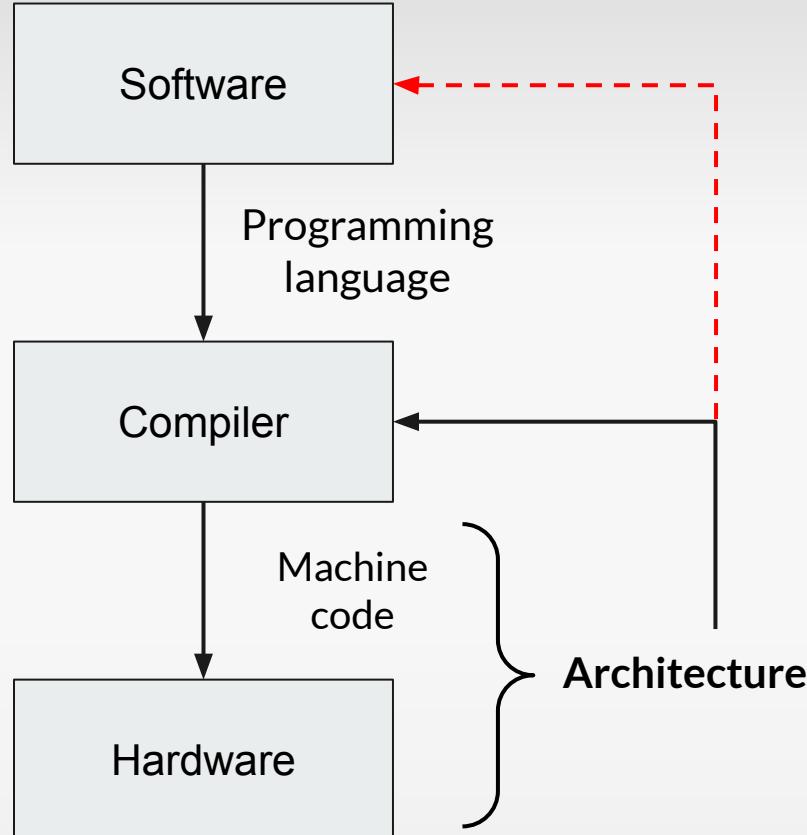
Why is the architecture important?



The architecture **affects the design of HPC software**:

- Memory bandwidth
- Cache memory size
- Frequency
- Number of cores
- Instruction set:
 - Floating point operations (e.g. $y = a x + b$)
 - Single Instruction Multiple Data (SIMD)
- Architecture-specific features

Why is the architecture important?



The architecture **affects how we program the software**:

- Intrinsic functions in C/C++ that are architecture-dependent
- Architecture-dependent extension of the programming lang:
 - CUDA for NVIDIA GPUs -> nvcc compiler
 - HIP for AMD GPUs -> hipcc compiler

All in one solution (CPUs, GPUs, FPGAs):

- OpenCL: open-source framework in C/C++
- OneAPI and DPC++: developed by Intel, C/C++ framework and extension of the programming language

Other alternatives? Standard libraries

- Standard Software Libraries define formal APIs to be implemented and optimized on specific architectures. Examples are
 - **BLAS**: Basic Linear Algebra Subroutines
 - **LAPACK**: Linear Algebra Package
 - ...
- These then have different implementations for various architectures:
 - **OpenBLAS**: Open-source library of BLAS
 - **Intel MKL**: Intel's implementation of BLAS and LAPACK
 - **cuBLAS**: NVIDIA's implementation of BLAS
 - **hipBLAS**: AMD's implementation of BLAS
- For reference see e.g.
 - [shorturl.at/aOPY6](https://software.intel.com/content/www/us/en/develop/tools/oneapi/components/math-kernel-library.html) →

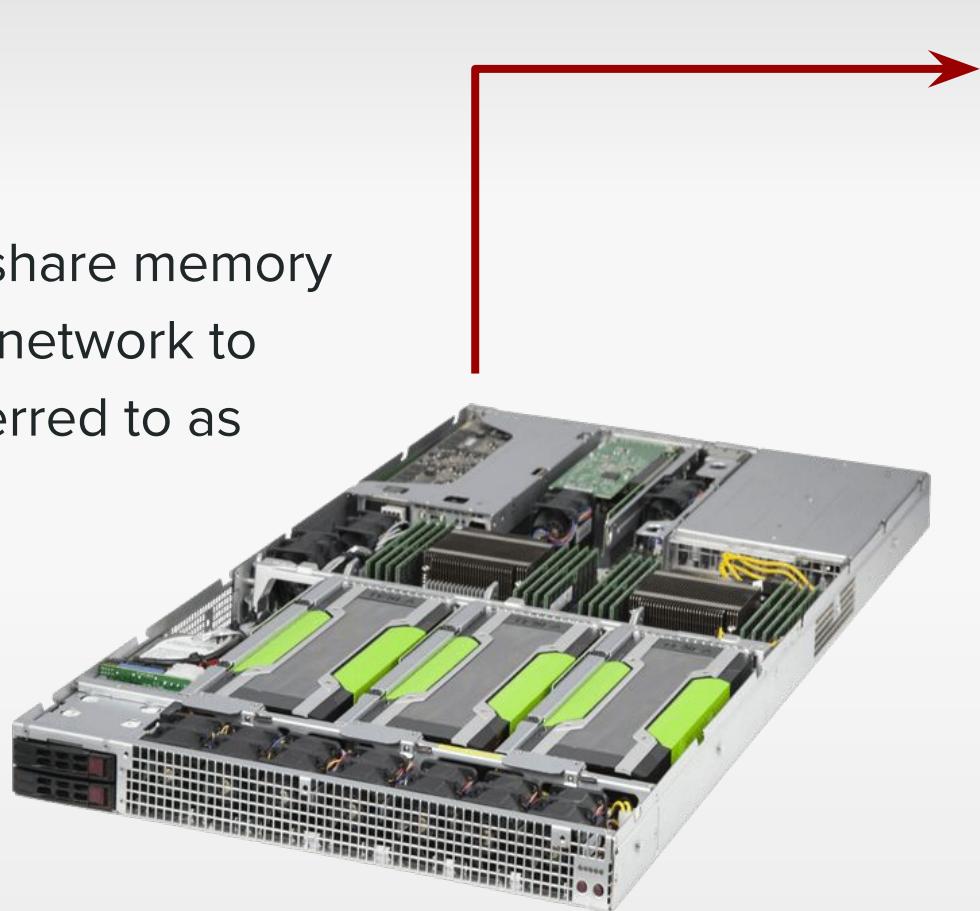
BLAS and Sparse BLAS Routines

Intel® oneAPI Math Kernel Library implements the BLAS and Sparse BLAS routines, and BLAS-like extensions.

- **BLAS Level 1 Routines** (vector-vector operations)
- **BLAS Level 2 Routines** (matrix-vector operations)
- **BLAS Level 3 Routines** (matrix-matrix operations)
- **Sparse BLAS Level 1 Routines** (vector-vector operations).
- **Sparse BLAS Level 2 and Level 3 Routines** (matrix-vector and matrix-matrix operations)
- **BLAS-like Extensions**

HPC is not only in-node performance

- Within a single node one can use **multithreading** and **shared memory**
 - E.g. see OpenMP
- But various nodes do not share memory and one needs to use the network to exchange data. This is referred to as **distributed computing!**
 - E.g. see MPI
- How to distribute?

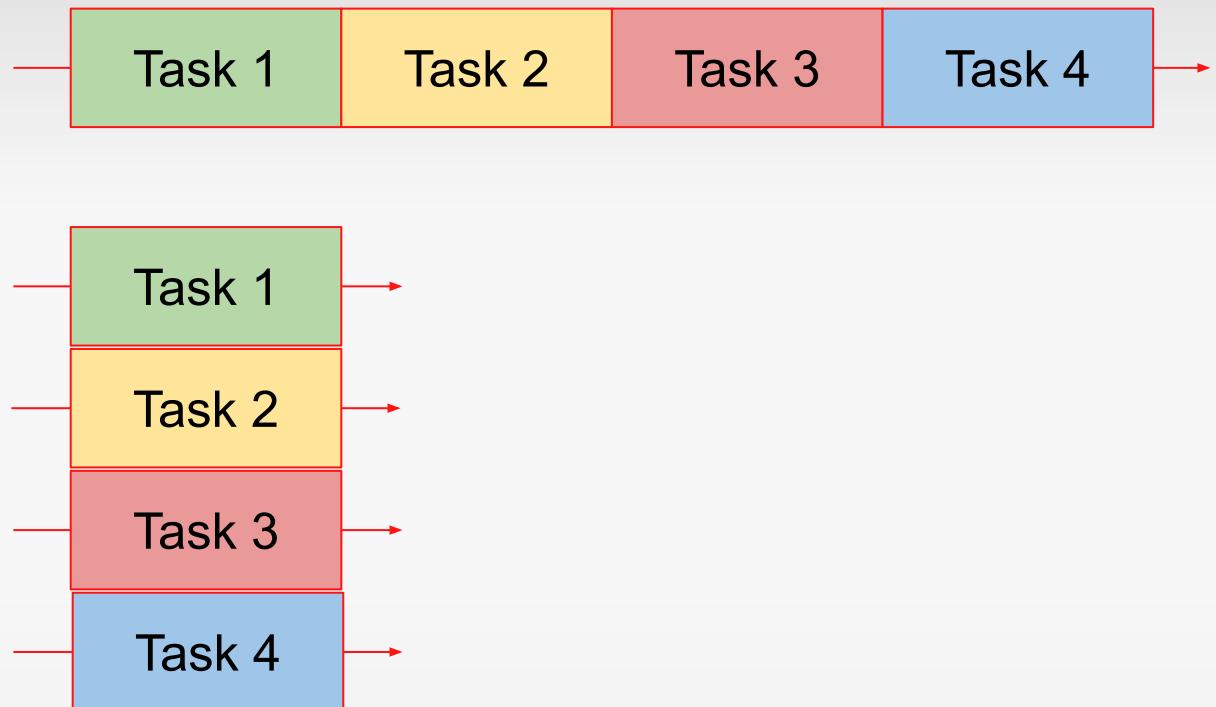


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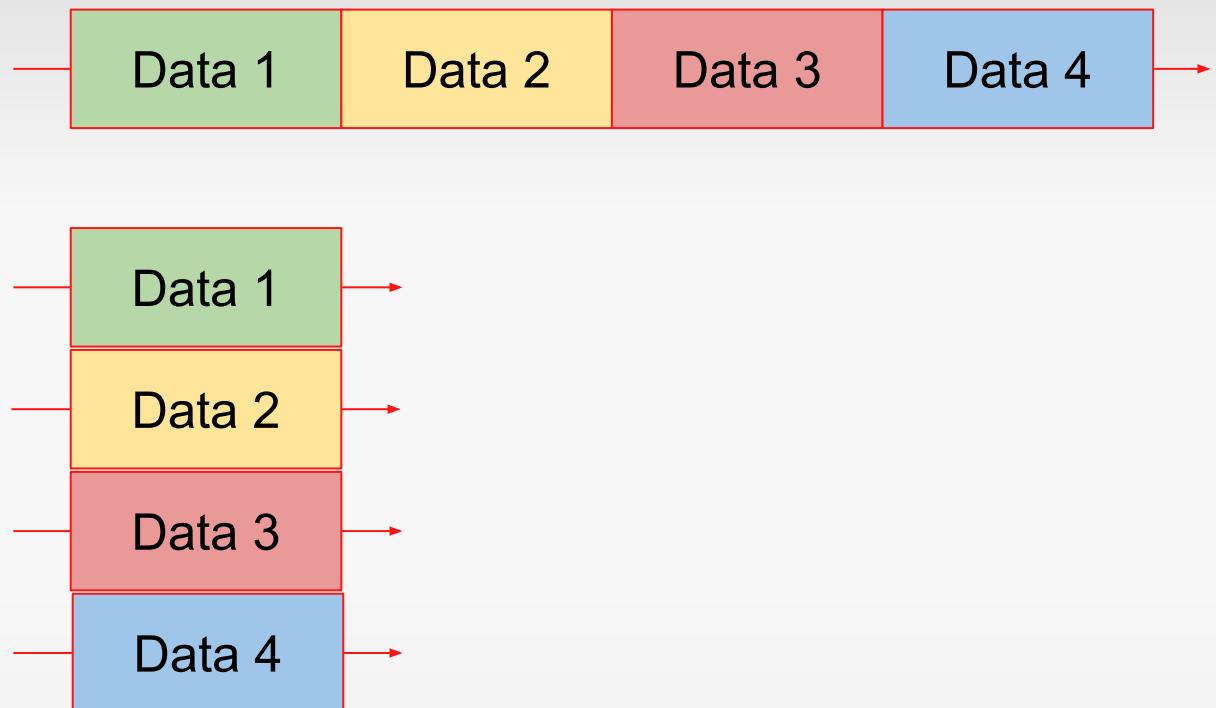
Parallel computing

- Task parallelism:
 - Independent tasks
- Distributed Data:
 - Independent Data
- Pipeline parallelism:
 - Dependent tasks/data
- Modular computing:
 - Architecture-dependent



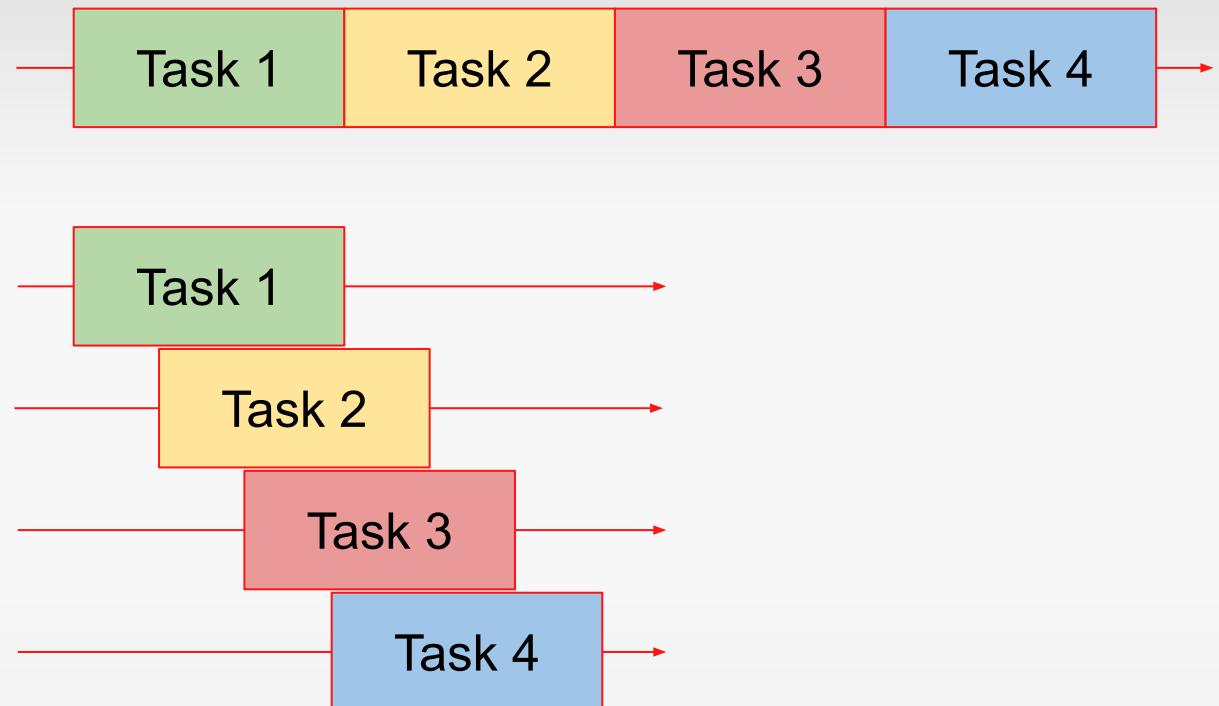
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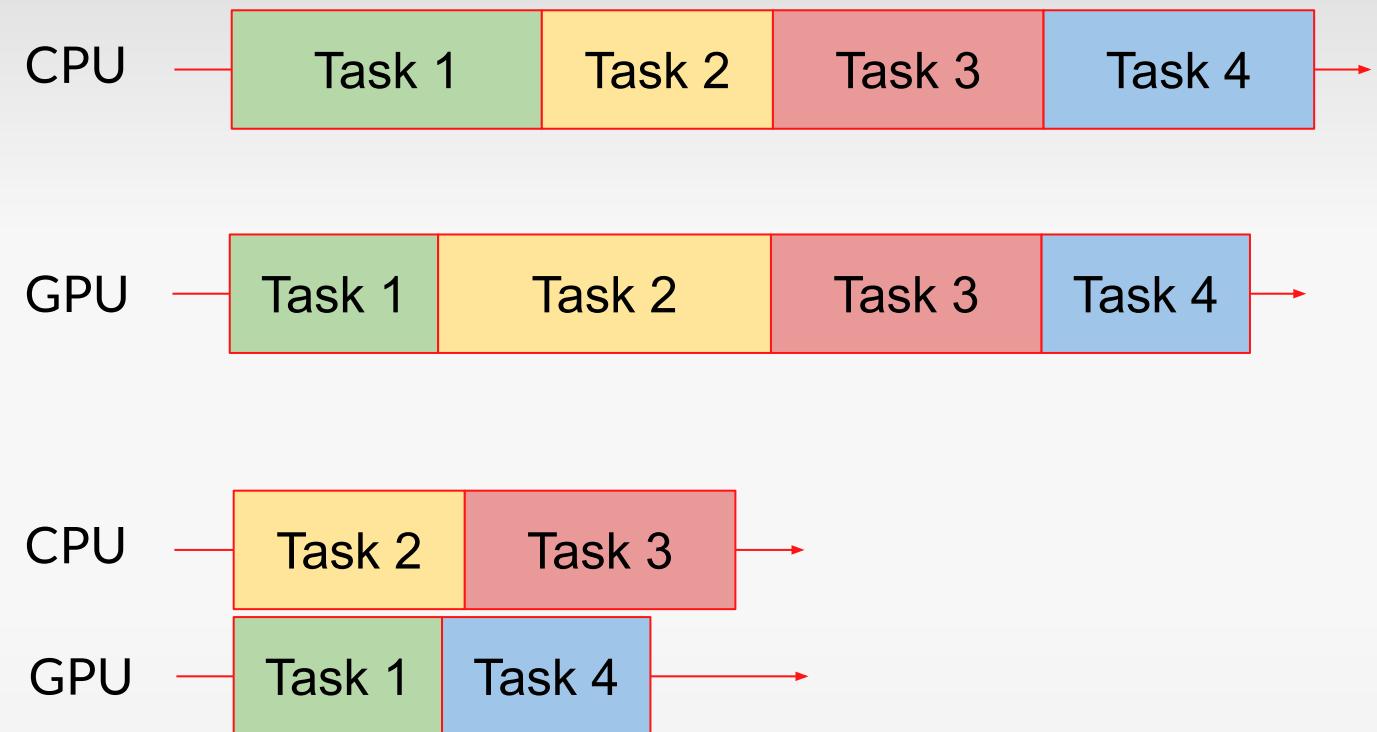
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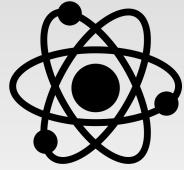
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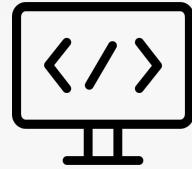




How to research using HPC



- ❖ **Scientific problem**
 - Numerical approach
 - Computationally intensive
 - Parallelizable (task or data)



- ❖ **Software**
 - Optimized for HPC
 - Scalable



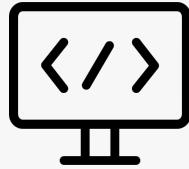
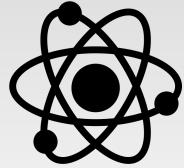
- ❖ **Access to a Supercomputer**
 - Preparatory access
 - Software test and benchmark
 - Competitive proposal for computing time



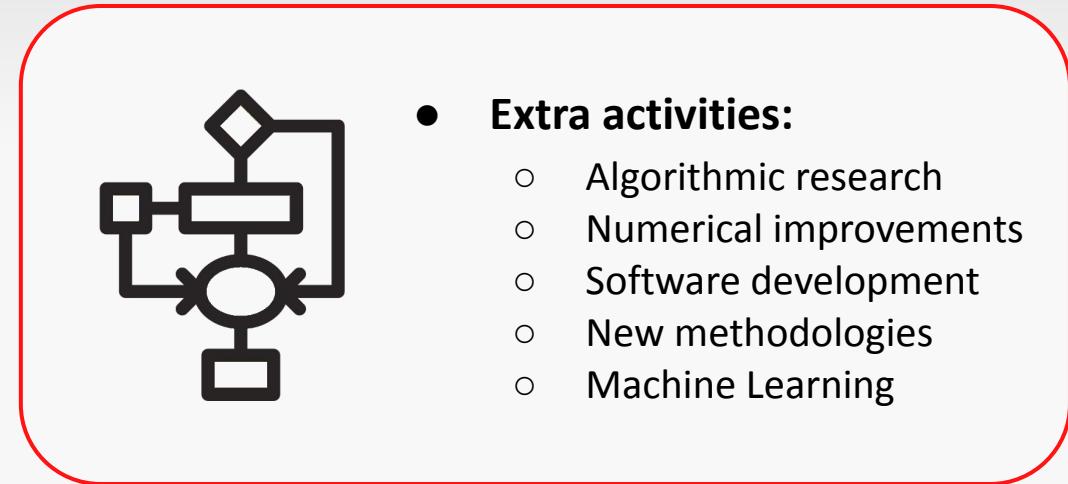
- ❖ **Production of results and analysis**
 - About 1 year long or more
 - Tera-/Peta-bytes of data produced
 - Various publications



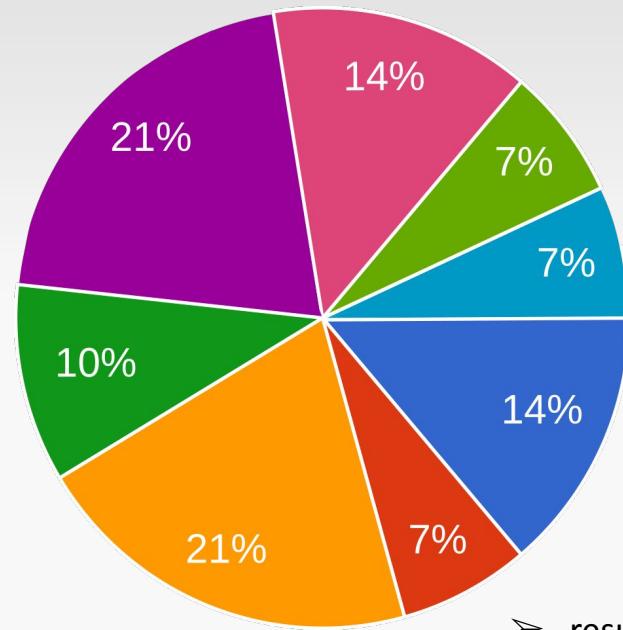
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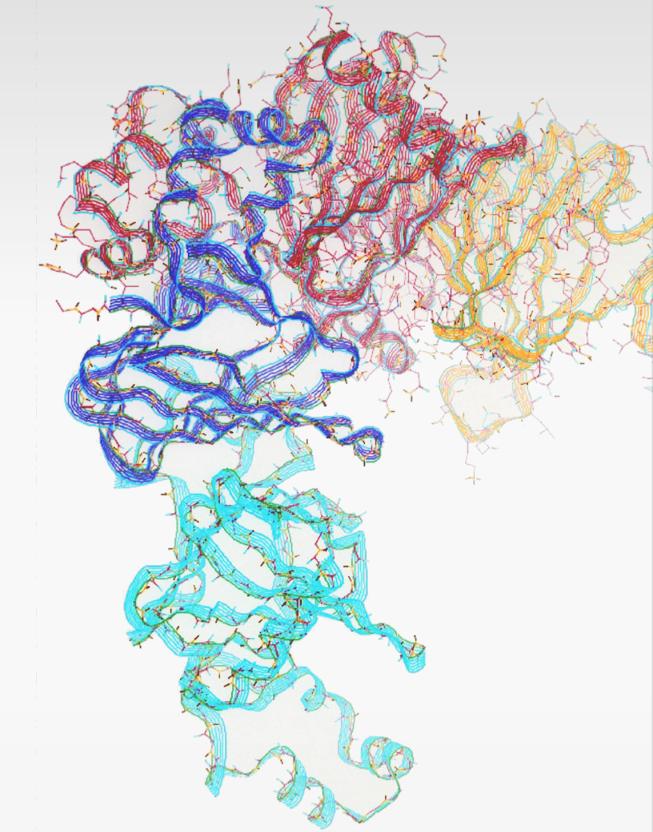
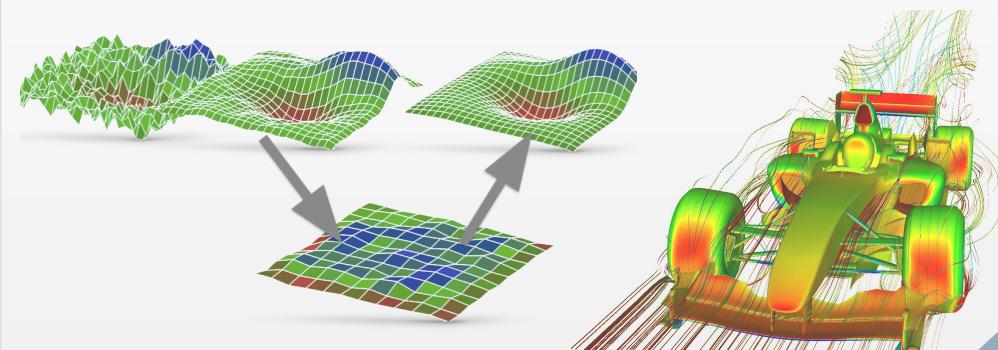


HPC research in Cyprus



- Biochemistry, Bioinformatics
- Chemical Sciences
- Earth System Sciences
- Engineering
- Physics
- Mathematics and Computer Sc.
- Economics, Finance
- Others

➤ results from our survey on the scientific community in Cyprus



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Our HPC systems

- **Cy-Tera** (2012 - Legacy):
 - 98 nodes, 12-cores Intel Xeon CPU
 - ~300 TFlops
 - served > 480 projects
- **Cyclone** (2020 - Active):
 - 33 nodes, 2 x 20-cores Intel Xeon CPUs
 - 16 nodes with 4 x NVIDIA V100 GPUs
 - ~600 TFlops
 - Applications for access at <https://hpcf.cyi.ac.cy/apply/>
- **Upcoming** a new system for industrial applications with latest NVIDIA or AMD GPUs
- **Prototype systems:**
 - **Cyclamen** (2018): 8 nodes, 2 x 16-cores Intel Xeon CPU, 2 x NVIDIA P100 GPUs
 - **Phi** (2011): 4 nodes, 16-cores Intel Xeon CPU, 16 Xeon Phi accelerators

For more details, see <https://castorc.cyi.ac.cy/infrastructure>



Thank you!

HPC NCC - CaSToRC



Questions?



Thank you!

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Thank you for your attention

... and talk to you later!

