STUDY ON HARDWARE REALIZATION OF GPS SIGNAL FAST ACQUISITION

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ABSTRACT

In GPS receiver the acquisition process generates two important parameters: the initial carrier frequency and the initial phase of the C/A code. In this paper two different methods for acquisition are mainly discussed: serial search in the time domain and FFT search in the frequency domain. Frequency domain acquisition involves using the Fast Fourier Transform (FFT) to convert the GPS signals into the frequency domain. One fast and easy-to-implement algorithm for averaging correlation is implemented and explained in detail. The FFT search method is both simulated in Matlab and evaluated in Altera Stratix DSP development board.

KEYWORDS

GPS FFT Modified C/A Code Hardware In the Loop

INTRODUCTION

Global Positioning System (GPS) has been found useful in most civil surveying and navigation applications. In GPS, each of the satellites uses a unique spreading sequence, and the receiver must acquire and track the pseudo-random number (PRN) code and carrier signals from GPS satellites.

Obviously signal cannot be demodulated when the three items are unknown to a receiver: 1) the received code, which is unique to each satellite, 2) code phase, which indicates the signal energy at correlation functions, and 3) carrier frequency offset, which is mostly due to Doppler effects

and limited precision of receiver clocks. If we assume that a GPS receiver knows which satellite code it is searching for, then a 2-D search is required.

Many algorithms for acquisition of GPS signals have been developed and evaluated, such as serial acquisition, parallel acquisition, matched-filter acquisition and FFT acquisition method. In this paper two different methods for acquisition are mainly presented: serial search in the time domain and FFT search in the frequency domain.

SERIAL SEARCH IN THE TIME DOMAIN

Serial search is the simplest and most frequently used acquisition algorithm. The most frequently used code acquisition system is the non-coherent correlator, show in Figure1. First the digital IF, $x[n]$, is multiplied by the replicated CA code, $CA[n+m]$. Here n represents the n^{th} sample and m represents the number of samples the replicated CA code is phase shifted. After code removal, the in-phase (I) and quadrature (Q) components are generated. The I and Q components are accumulated for one or more code periods. The accumulated sum is squared. If the correlation point is larger than a certain threshold it is assumed that the satellite is acquired.

The serial search can be done by evaluating each unknown until a correct combination of the parameters is achieved. If there is no correct combination of carrier frequency and code phase, the receiver searches for a different PRN code. The disadvantage of this search is that it might necessitate exploring all of the combinations of the 2-D search plane serially. For a stationary receiver it is common to assume a ±10 kHz Doppler offset on the carrier. The acquisition process for each code period is stepped in the Doppler range in 500 Hz frequency increments. Choosing 500 Hz steps is a compromise in accuracy and speed. Thus, serial search tests 2,046 half chips on the code phase dimension for 21 carrier frequency search steps[11]. The slow acquisition process is due to many reasons; one of them is the large computation cost of the circular correlation.

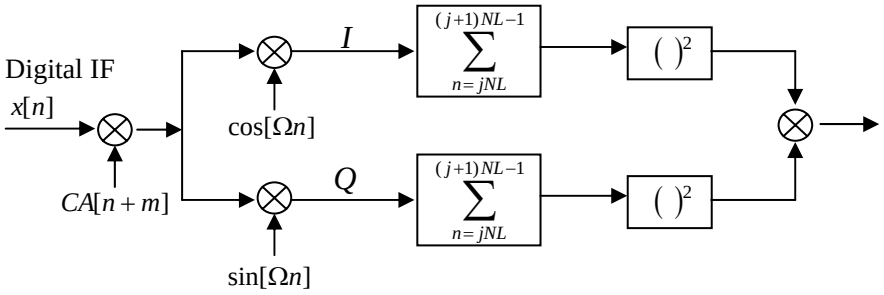

Figure 1 Non-coherent Correlator in Time Domain[12]

FFT SEARCH IN THE FREQUENCY DOMAIN

In order to shorten the acquisition time, many algorithms are investigated to reduce the computations required by the correlation function. One algorithm uses averaging correlations for GPS signal acquisitions that simplify the implementation and reduce the required computations. This method is implemented in FPGA to benefit from the parallel processing of this technology and solves the presented problem of the GPS receivers by significantly reduce the acquisition time.

I. FFT SEARCH PRINCIPLE

The acquisition process time is shortened when the search dimensions can be searched in parallel. Since C/A code is periodic, its correlation can be replaced by circular correlation, in presence of random noise. It has been proven that circular correlation can be efficiently accomplished in frequency domain processing using Fast Fourier Transform (FFT).

$$S[n] \otimes CA[n] = \sum_{r=1}^{N} (S[r] \times CA[r-n]) = F^{-1}[F(S[n]) \times \overline{F(CA[n])}] \qquad (1)$$

The circular correlation is performed by using the FFT convolution property. FFT-based circular convolution is achieved by multiplying the two sequences (or signals) in the frequency domain. Equation 1 shows how the convolution is calculated using the FFT/IFFT functions.

Assuming that the correct code phase is utilized, a FFT is performed to the signal after wiping off the code (see Figure 2). The acquisition is complete if there is a peak in the output of the Inverse Fast Fourier Transform (IFFT) after its magnitude is squared. This means the search is performed in parallel for all of the frequencies. However, the calculation of one FFT requires much more effort than one serial search.

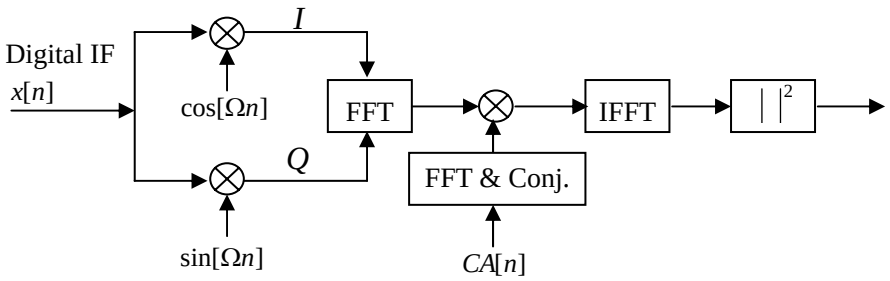

Figure 2 Non-coherent Correlator in Frequency Domain [12]

II. MODIFIED-CODE AVERAGING CORRELATION

The incoming signal of the GPS receiver passes through down-converter and A/D and forms the intermediate signal. If we assume that data-sampling rate is 6.144MHz, the intermediate frequency is 1.835MHz.

This means that every 1-ms of the GPS signal has 6,144 samples. Therefore, two 6,144-point FFTs and one 6,144-point IFFT are required to implement the C/A code correlator. However, it has been found that acquisition with 6,144 point FFT is not easy to be accomplished in real time even with the powerful FPGA devices, which might be the reason why the frequency domain process is not popular in present GPS receivers.

Different algorithms were suggested to ease the implementation of this method in an FPGA. One fast and easy-to-implement algorithm for averaging correlation is introduced here. The algorithm is called modified-code averaging correlation based GPS block processing, which is proven to be a convenient realization of frequency domain correlation in [2,3].

The averaging method averages the incoming 6,144 samples to become 1,023 averaged samples. If the starting point of the averaging operation is chosen in the right place, the 1,023 new samples may represent the original chips of the C/A code. In other words, one can say that a full C/A code is presented by 6,144 samples and that its chips are represented by approximate six samples each. Since the C/A code is circular, therefore, the right averaging starting point is one of six successive samples. This will generate six of the 1,023 averaged-samples code. One of the generated sequences is considered a good approximation of the original C/A code[2]. This best recovered averaged sequence contains the strongest peak among the other five and estimates the code phase in chips (1/1023 ms).

This method retains the signal to noise ratio observed in more expensive correlators[2]. The acquisition time is reduced by using this method, because calculating six 1,023-point FFTs and IFFTs requires less time (in software and in hardware) than the 6,144-point FFTs and IFFTs. However, implementing 1,023-point FFT (or IFFT) is not an easy task since it is not a power of two and cannot use the available Altera's 1024-point FFT IP core.

The size incompatibility problem between C/A code and the available FFT core can be solved by changing the down-sampling rate from 1,023 to 1,024. So, the 6,144 samples will be down sampled (or averaged) to 1,024 points. A similar procedure will be done to the local code. Therefore, the local code will be up-sampled to 6,144 and then down sampled to 1,024 points. Therefore, the averaging correlator here will use 1,024 averaged samples and 1,024-point modified C/A code. This modified C/A code is still considered a unique code related to the selected C/A code. It cannot be generated from a different C/A code[6].

III. FPGA IMPLEMENTATION

A block diagram of modified-code averaging correlation based acquisition is shown in Figure 3. The averaging correlator is performed on both the in-phase and the quad-phase by considering the in-phase values as the real input components, while the quad-phase values are used as the imaginary input components. First, apply 1024-point FFT to the local modified code and perform the conjugate operation to the FFT output (In practice this can be pre-calculated in Matlab and stored in RAM of FPGA). The next step is to multiply the complex outputs of the FFTs. The results are then changed back to the time domain using 1024-point IFFT. When the magnitude of the IFFT result is carried out, the 1024 values are inspected for the maximum (or the peak) value. The location of the peak reflects the code phase in chips (or in 1/1024 ms). Additional, a state machine and feedback unit is needed to control the whole process.

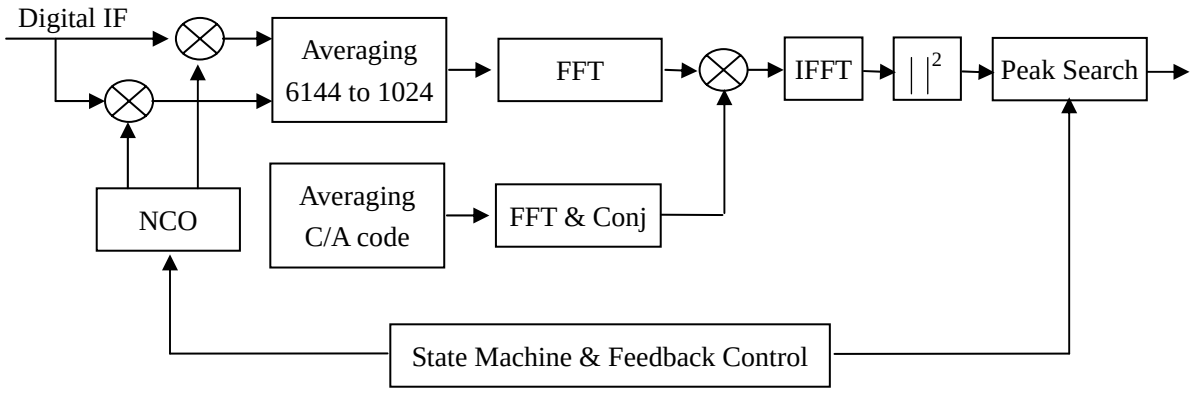

Figure 3 Acquisition Using Modified-code Averaging Correlation

In the experiment, we choose to perform algorithm development and analysis in Matlab, system level design and hardware simulation using Altera DSP Builder which integrates DSP tools by combining the algorithm development, simulation, and verification capabilities of The MathWorks MATLAB and Simulink system-level design tools with VHDL and Verilog HDL design flows.

Figure 4 shows the FPGA simulation model using the HIL (Hardware In the Loop) block of the DSP Builder, which allows user to co-simulate a software design with a physical FPGA board implementing a portion of that design. The simulation sources are transmitted to FPGA through JTAG line, and results generated by hardware are transmitted back to the sinks in Simulink.

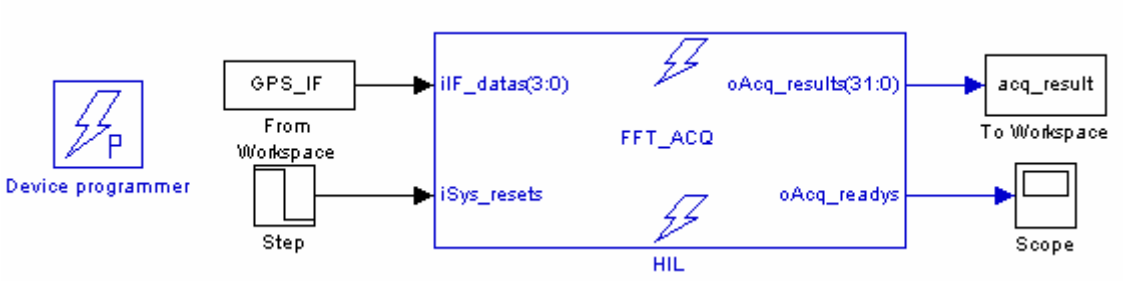

Figure 4 FPGA Simulation Model Using HIL Block

IV. SIMULATION RESULTS

For the benefits of our selected development tools described above, we can apply the same sources to the hardware simulation in Altera Stratix EP1S25 DSP development board as the software simulation in Matlab.

The results of three simulation modes according to the different SNR signals (from 0dB to -25dB) are shown in Figure 5 (The x-axis represents SNR of signals; y-axis represents the peak to the second peak ratio.).

Comparing the simulation results in Figure 5, we can see that the modified-code averaging based FFT acquisition method (in Matlab) has approximate the same good performance as direct FFT acquisition method using the whole 6,144 samples.

Another conclusion we can draw is that, when the modified-code averaging based FFT acquisition method is implemented in FPGA, the performance has declined in a receivable range by reason of quantization error from floating-point calculation to fixed-point calculation and truncation error between fixed-point buses for sake of saving FPGA resources.

So it is proven that the implementation of this averaging FFT search architecture provided fast acquisition with accurate synchronization without losing much of the signal energy. The hardware implementation in Stratix EP1S25F780C5 FPGA was able to process 1-ms of a normal GPS signal in less than 1-ms.

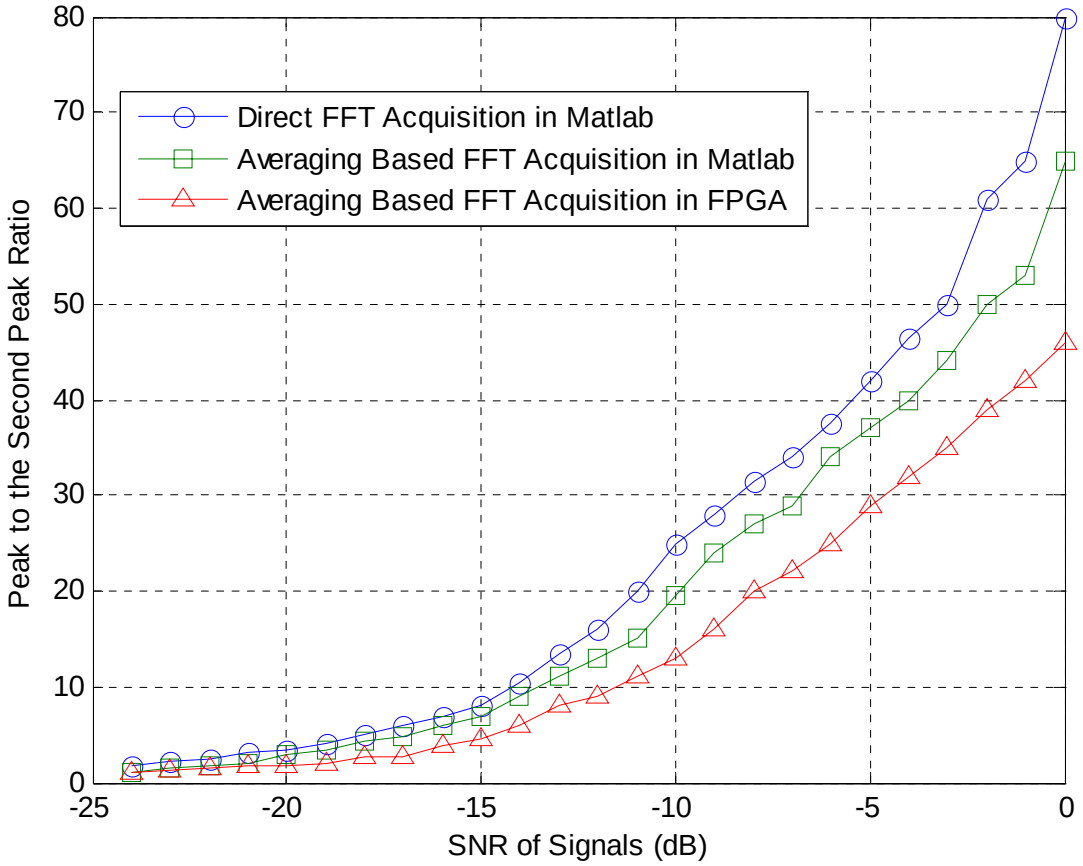

Figure 5 the Comparison of Three Simulation Modes

CONCLUSIONS

Through the software simulation and hardware experiments, the FFT search method implementation can enable real-time acquisition of one satellite in less than 20 milliseconds. Comparing this performance with the performance of the traditional GPS receivers whose acquisition time is more than 40 seconds, the search method minimizes the acquisition time 2000 times. It is considered a viable solution to satisfy the stringent demand for the cold-start acquisition time and high-dynamic working environment. Also frequency domain processing will become more feasible and popular if this method is implemented in civil GPS receivers.

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