2025 Digital IC Design

Homework 1: Median Finders Using Comparator2

1. Introduction:

This homework focuses on designing digital modules to implement a median finder circuit using hierarchical design. In this homework, you are requested to design a dual-input Comparator2 circuit, which determines the maximum and minimum value among two input 4-bit numbers. The dual-input Comparator2 circuit is then used to construct larger modules to determine median value for higher amounts of input number.

1.1. Dual-input Comparator2

The logic diagram of the dual-input Comparator2 for this homework is shown in Fig. 1, and its specification and I/O interface is listed in Table I. The Comparator2 is a basic module that takes two 4-bit numbers as inputs and outputs their minimum and maximum values.

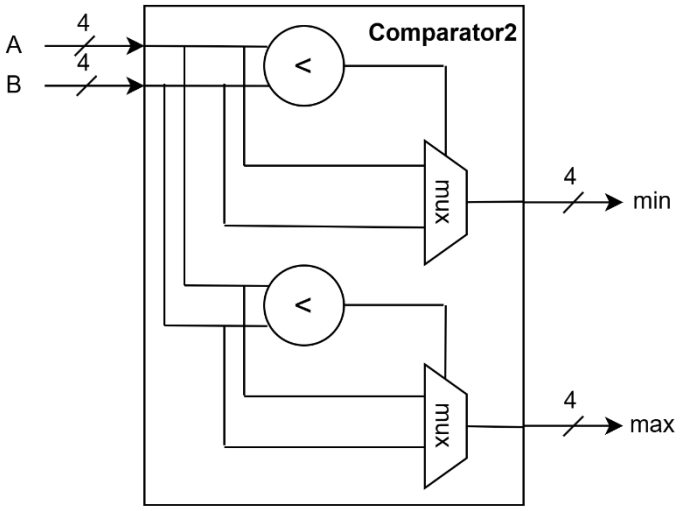

Fig. 1 Logic diagram of the dual-input Comparator2.

Table I. Specification and I/O interface of Comparator2.

Signal Name	I/O	Width	Description
A	I	4	First 4-bit input number
B	I	4	Second 4-bit input number
min	O	4	The smaller of the two input numbers
max	O	4	The larger of the two input numbers

1.2. Three-input Median Finder

The logic diagram of the three-input Median Finder module for this homework is shown in Fig. 2, and its specification and I/O interface is listed in Table II. The three-input Median Finder module takes three 4-bit input numbers and finds the median value. In this homework, you must construct the three-input Median Finder circuit with your dual-input Comparator2 modules.

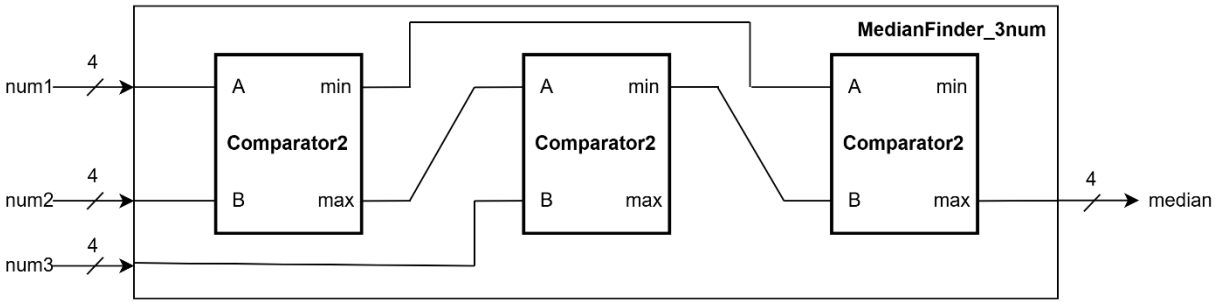

Fig. 2 Logic diagram of the three-input Median Finder.

Table II. Specification and I/O interface of Median_Finder3.

Signal Name	I/O	Width	Description
num1 ~ 3	I	4	Input number 1 ~ 3.
median	O	4	The median value of the three input numbers

1.3. Five-input Median Finder

The logic diagram of the three-input Median Finder module for this

homework is shown in Fig. 3, and its specification and I/O interface is listed in Table III. The five-input Median Finder module takes five 4-bit input numbers and finds the median value. In this homework, you must construct the five-input Median Finder circuit with your dual-input Comparator2 modules and MedianFinder_3num module.

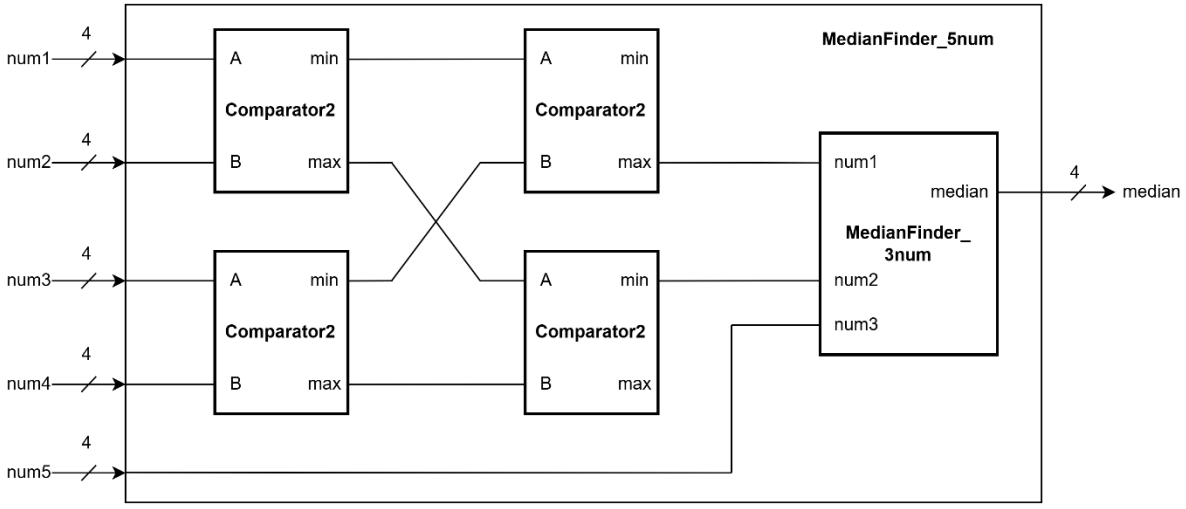

Fig. 3 Logic diagram of the five-input Median Finder.

Table III. Specification and I/O interface of Median_Finder5.

Signal Name	I/O	Width	Description
num1 ~ 5	I	4	Input number 1 ~ 5.
median	O	4	The median value of the three input numbers

1.4. Seven-input Median Finder

The specification and I/O interface of the seven-input Median Finder for this homework is listed in Table IV. The seven-input Median Finder module takes seven 4-bit input numbers and finds the median value. In this homework, you must construct the seven-input Median Finder circuit with your dual-input Comparator2 modules, while using MedianFinder_3num and MedianFinder_5num modules is accepted.

Table IV. Specification and I/O interface of Median_Finder7.

Signal Name	I/O	Width	Description
num1 ~ 7	I	4	Input number 1 ~ 7.
median	O	4	The median value of the three input numbers

1.5. File Description

File Name	Description
Comparator2.v	The module of dual-input Comparator2.
MedianFinder_3num.v	The module of three-input Median Finder.
MedianFinder_5num.v	The module of five-input Median Finder.
MedianFinder_7num.v	The module of seven-input Median Finder.
testfixture.sv	Testbench file. The content in this file is not allowed to be modified.
golden_comp.dat	Test and golden data file for Comparator2.
golden_3num.dat	Test and golden data file for MedianFinder_3num.
golden_5num.dat	Test and golden data file for MedianFinder_5num.
golden_7num.dat	Test and golden data file for MedianFinder_7num.

2. Scoring:

2.1. Dual-input Comparator2 [40%]

The result should be generated correctly, and you will get the following message in ModelSim simulation.

```
#
# ------------              Stage1: Comparator2 Pass !              ------------
#
```

Fig. 4 Simulation result for Comparator2.

2.2. Three-input Median Finder [30%]

The result should be generated correctly, and you will get the following message in ModelSim simulation. Please construct the MedianFinder_3num

circuit with your dual-input Comparator2 modules. Otherwise, you can just get half of the points.

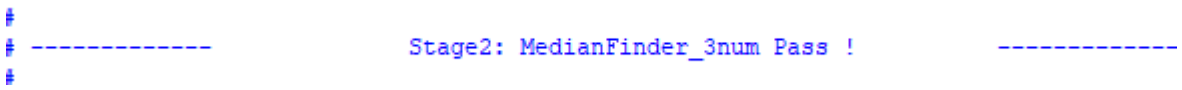

Fig. 5 Simulation result for MedianFinder_3num.

2.3. Five-input Median Finder [20%]

The result should be generated correctly, and you will get the following message in ModelSim simulation. Please construct the MedianFinder_5num circuit with your Comparator2 modules and MedianFinder_3num module. Otherwise, you can just get half of the points.

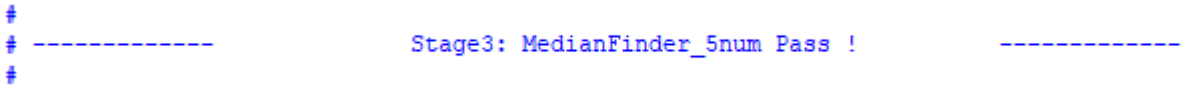

Fig. 6 Simulation result for MedianFinder_5num.

2.4. Seven-input Median Finder [10%]

The result should be generated correctly, and you will get the following message in ModelSim simulation. Please construct the MedianFinder_5num circuit with your Comparator2 modules (using MedianFinder_3num and MedianFinder_5num modules is accepted). Otherwise, you can just get half of the points.

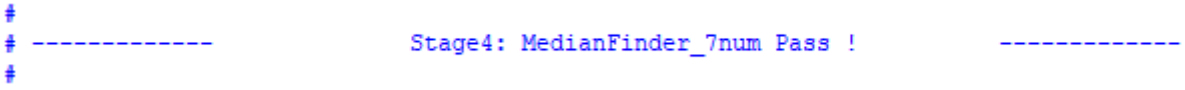

Fig. 7 Simulation result for MedianFinder_7num.

3. Submission

3.1. File Submission

You should classify your files into two directories and compress them to .zip format. The naming rule is StudentID.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL

*.v	All of your Verilog RTL code
	Documentary
Report.pdf	The report file of your design (in pdf).

Fig. 8 File hierarchy

StudentID.zip
- StudentID
  - RTL
    - *.v (All of your Verilog RTL code)
  - Documentary
    - Report.pdf

3.2. Report File

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible. Please focus on the description of the hierarchy of your MedianFinder_7num module.

3.3. Notes

a. Please submit your .zip file to folder HW1 in moodle.
   Deadline: 2025/03/23 23:55
b. Late submissions will result in a penalty of 5 points per day.