2025 Digital IC Design Homework 3

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| NAME | 方騏為 | | | | |
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| **Simulation Result** | | | | | |
| Functional simulation | | Pass | | Pre-Layout simulation | Fail |
|  | | | | Please specify your clock width: (ns) (your pre-sim result) | |
| **Synthesis Result** | | | | | |
| Total logic elements | | |  | | |
| Total memory bits | | |  | | |
| Total registers | | |  | | |
| Embedded multiplier 9-bit elements | | |  | | |
| (your flow summary) | | | | | |
| **Description of your design** | | | | | |
| 用pipeline完成，在中間會同時有讀訊號、計算和傳送的三組資料。  並且用狀態有限基控制完成狀況 | | | | | |