



UVM Reference Flow Design Overview

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Acronyms

Acronym	Meaning
AHB	Advanced High Performance Bus
AMBA	Advanced Micro-controller Bus Architecture
APB	Advanced Peripheral Bus
SoC	System On Chip
IP	Intellectual Property
MAC	Media Access Controller
UVM	Universal Verification Methodology
DMA	Direct Memory Access

Licenses, Terms and Conditions

Refer to the README_terms_and_conditions.txt file located in the installation directory in the <UVM Reference Flow Install area>.

Scope

This document provides the architectural design for the Ethernet Switch SoC design, which used as the basis to demonstrate the UVM reference flow.

Introduction

The functional block diagram of the complete Ethernet switch SoC design is shown in Figure 1. It has an Ethernet MAC, a processor (Open Risc) and a look-up table to carry out the address resolution. This document specifies the architecture of the SoC.

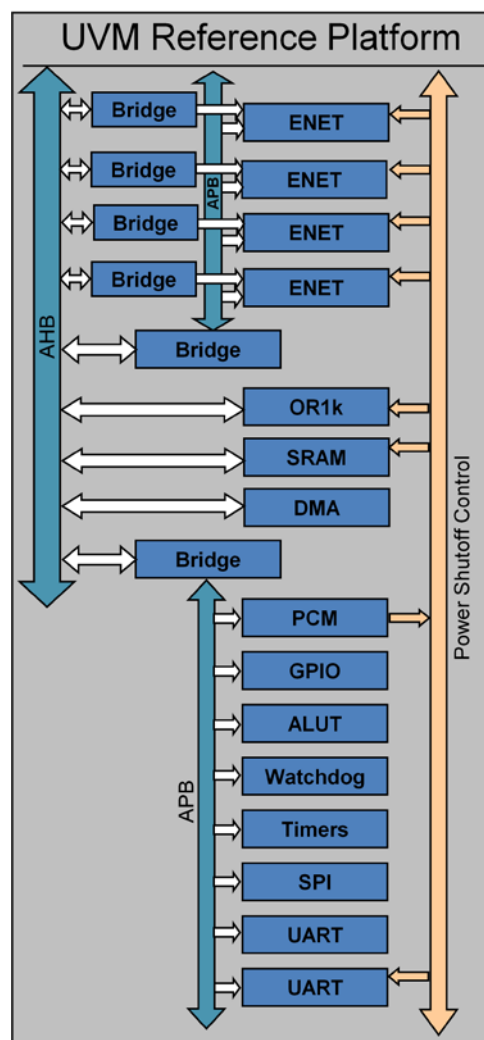


Figure 1: Ethernet Switch Design

The SoC has the following key components:

1. Processor Subsystem
 - a. An Open RISC Processor
 - b. AMBA AHB network interconnect
 - c. On-chip Memories and memory controllers
 - d. DMA
2. Open Core Ethernet Media Access controller (MAC)
3. Address Look up table (ALUT)
4. Support and Control functions. For instance power management and peripherals like UART, SPI, GPO, timer etc

In normal operation, the data flow occurs between two or more of the Ethernet MAC ports. An incoming Ethernet packet from a MAC interface is switched to one or more (broadcast) MAC ports based on the result from Address Lookup up Table (ALUT).

The switching is performed by the embedded firmware running on the processor. The firmware is responsible to allocate the buffers (in the on-chip RAM) into which the MACs can source and sink packets. When a complete packet is available in the memory, the firmware is notified about it. The firmware then parses the packet, extracts the headers and does a lookup on the ALUT. Based on the lookup result, the packet is switched by the firmware to one or more MACs.

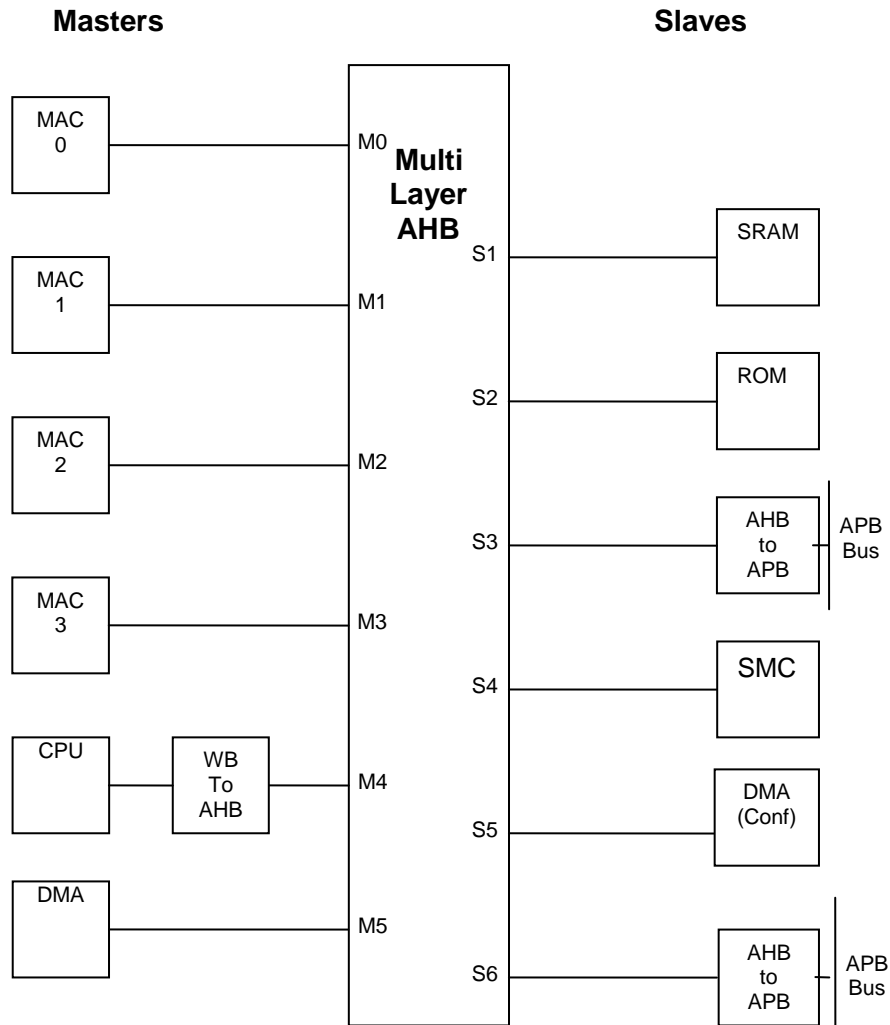
System AHB bus

The SoC is built around a multilayer AHB bus which inter-connects the CPU, the memory and peripherals.

A multi-layer implementation can support more parallel accesses than a single layer bus.

AHB masters on the bus initiate data transfers and AHB slaves respond to the data requests. The masters are not memory mapped, while the slaves are memory mapped. Refer to the memory map at the end of the spec for information on the slaves' memory map.

The bus has a 32-bit data width and runs at half the CPU speed. At 100MHz, the bus can support burst data rates of 400 MB per second for each master-slave channel.



The figure above shows six masters connected to six slaves through the multi-layer AHB. The APB peripherals interface to the AHB bus through a translating AHB-to-APB bridge.

The table below depicts the connectivity between masters and slaves in the design. An "X" indicates that access is legal.

Master	SRAM S1	ROM S2	APB Bridge S3	SMC S4	DMA S5	APB Bridge S6
MAC0	X					
MAC1	X					
MAC2	X					
CPU	X	X	X	X	X	X
DMA	X					