1. Introduction

This chapter describes the supply related low power modes are implemented on Soc Kit. The goal is to reduce both static and dynamic power consumption while avoiding area and timing penalties. This chapter does not describe clock gating for power reduction; this is described in a later chapter.

Section 2 describes the generic low power techniques that can be used to reduce both static and dynamic power consumption.

Section 3 looks at the options that we have for saving power on the SoC Kit design and then describes low power modes that are specific to the SoC Kit design. These modes build upon the techniques that are described in section 2.

Finally the remainder of the chapter describes the logic that implements the low power modes. The state machines for the Level1 and Level2 modes are described. The status and configuration registers for the various low power modes are also described.

2. Generic low power techniques

This section describes low power techniques that can be applied to any design to reduce power.

2.1. Using a Multi Vt library

MOSFETs that have a higher Vt will have a lower leakage current for a given supply voltage. However this reduction in leakage current comes with a penalty in switching speed. A multi Vt library typically has two versions of each functional gate – one implemented with high Vt transistors and the other implemented with low Vt transistor.

The goal is to use the faster low Vt gates on the speed critical paths and use high Vt gates on the rest of the paths.

During initial synthesis only low Vt gates so that the speed goal is quickly met. During the next round of synthesis, those paths that have a positive slack will have their gates replaced with high Vt versions until the positive slack goes down to zero.

Using multi Vt libraries reduces leakage power consumption.

2.2. Power Shut-off with Logic State Retention

In this technique, the current state or context of logic, is preserved while the logic is powered down to save power. This is done by using State Retention (SR) FFs in place of normal FFs wherever state has to be retained through a power cycle.

SR FFs have two power supplies, a main VDD supply which it shares with the rest of the combinatorial logic and a Vret retention supply which feeds the state retention portion of the state retention FFs. The main supply is shut off in retention mode but the retention supply is never shut off. Vret is equal to VDD during normal operation. In retention mode it may be possible to reduce Vret to save on leakage power but doing this will complicate the power supply structure and will not yield much of a power saving. The retention portion of the SR FF uses high Vt transistors to minimize its power consumption.

Using SR flops allows us to implement low power modes in which most of the logic are switched off thereby saving on leakage power.

Only those flops in a design whose state has to be retained through a power cycle should be implemented with state retention since the use of SR Flops comes with an area penalty and also a power penalty in normal mode.

Since we are not sure of which Flops should be preserved through a power cycle all flops in the design will be implemented as SR flops.

2.3. Memory retention

This low power technique makes use of the fact that on-chip RAMs can retain their contents even when the supply voltage is lowered from the normal operating level. The limiting voltage below which the memories lose data is known as the memory retention voltage. The memory can retain its contents indefinitely at the retention level, but the memory cannot be accessed by logic.

Do not confuse the memory retention voltage with the retention supply that the SR Flops use.

Memory retention can be used in conjunction with a module that implements logic state retention. When the module enters retention mode it cannot access its memories and hence any memory that is belongs to this module can be placed in its retention mode. This way both the logic and its memory retain their state in the low power mode and they can continue operation once the supplies are restored.

A RAM that implements memory retention cannot be connected to the main core power network because in retention mode its supply voltage is lower than the normal supply voltage. The memory must be supplied from a programmable voltage regulator which is controlled by the power control block. The regulator could be on-chip or off-chip.

2.4. Dynamic Voltage Frequency Scaling (DVFS)

DVFS refers to a technique in which both the supply voltage and the operating frequency of a module is scaled according to the processing load on the module. When the load is low both the operating frequency and the supply voltage are reduced relative to their normal values. Reducing the supply voltage reduces both the dynamic and leakage power. The frequency has to be scaled down along with the supply voltage because of the increase in path delays at lower voltages.

The operating point of a module with DVFS is controlled by high level software such as the Operating System which is aware of load that the module has to handle.

Implementing DVFS requires both level shifters and synchronizers around the target module to handle the voltage and frequency changes.

2.5. Low supply voltage islands

The voltage island technique aims to reduce the power consumption of a module by having it work at the lowest supply voltage which can sustain its rated frequency. While the rest of the chip runs at its rated supply. It makes use of the fact that modules that do not contain the critical timing paths when the supply is at its normal level can have their supply reduced until the module's timing paths approach the critical timing paths. The module with the reduced supply is placed in a dedicated voltage island which isolates it from the rest of the chip.

The low supply technique can be considered to be a reduced form of DVFS in which the frequency is not scaled. Further the scaling of the supply voltage is not done dynamically by the Operating System. The lowest possible supply voltage is determined statically based on the results of timing analysis at different voltages.

A module that runs on a reduced supply voltage will need level shifters around it.

3. Low Power modes for the SoC Kit design

This section describes the basis on which the lower power modes are defined and gives details on how they operate.

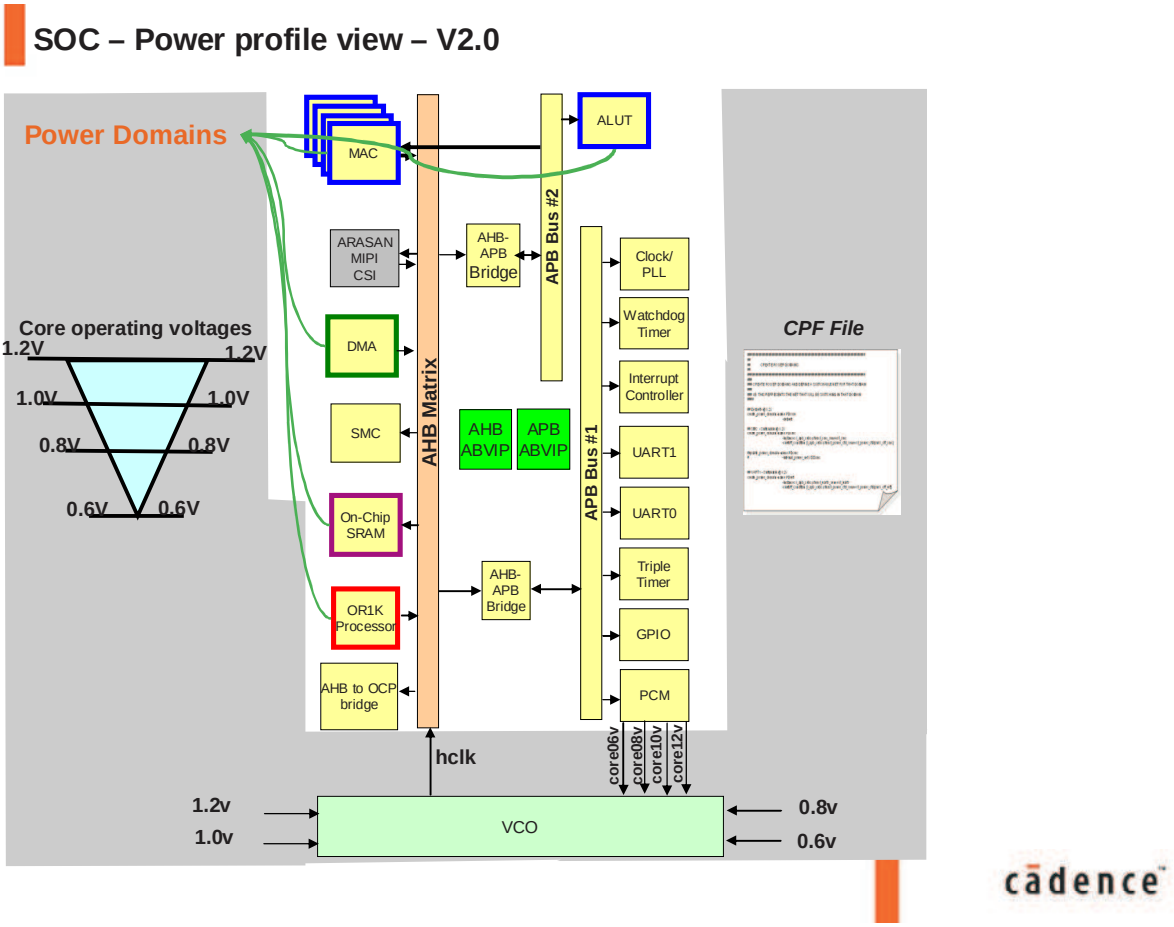
The first step in the definition of the low power modes is the identification of the largest consumers of static and dynamic power on the chip. Then low power modes must be defined to target these parts of the chip. The low power modes should also be viable from the customer's usage point of view.

The low power techniques that will be applied on this chip are

- Power shut off (with logic state retention)
- Memory retention
- Low supply voltage islanding.

Since we do not have the power numbers at this point of time, we have to go by heuristics in selecting which parts of the chip will have low power modes.

Modules that have a high gate count are the best candidates for power shut-off and Low supply voltage islanding. Similarly, the largest memories are the best candidates for saving power through Implementation of memory retention modes.



The MAC (4x), DMA and the CPU are the largest modules on the chip. These IP's will be targeted for low supply voltage islanding and for module level power shut off. We will also shut off the Address lookup table (ALUT) when all the 4 MAC MAC's are shutoff.

The 256K Word SRAM memories are the largest on-chip memories. Hence they are selected for the implementation of memory retention modes to reduce leakage power. The on chip memory is split into 5 physical voltage islands. These voltage islands can work at independent voltage levels. The split is as below

PD_mem_macb0: Physical memory of 32 K bytes for MAC 0. This memory holds the buffer data for the MAC 0. When MAC 0 is shutoff, this memory segment's operating voltage can be brought down and held at standby voltage

PD_mem_macb1: Physical memory of 32 K bytes for MAC 1. This memory holds the buffer data for the MAC 1. When MAC 1 is shutoff, this memory segment's operating voltage can be brought down and held at standby voltage

PD_mem_macb2: Physical memory of 32 K bytes for MAC 2. This memory holds the buffer data for the MAC 2. When MAC 2 is shutoff, this memory segment's operating voltage can be brought down

PD_mem_macb3: Physical memory of 32 K bytes for MAC 3. This memory holds the buffer data for the MAC 3. When MAC 3 is shutoff, this memory segment's operating voltage can be brought down and held at standby voltage

Based on the above analysis and taking into account the likely customer usage scenarios the chip will have the following low power modes/techniques.

- Level1 modes (module level power shut off for MAC (4x), ALUT, CPU and DMA modules)
- Hibernate Mode (chip level power shut off)
- Retention mode for the on-chip Instr and Data mem

PDcore	Pduart	PDsmc	PDmacb	PDmacb	PDmacb2	PDmacb3	PDalut	PDdma	PDcpu	PDmem _macb0	PDmem _macb1	PDmem _macb2	PDmem _macb3	PDmem _others	PDmem _ins_ram
1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
1.2V	Off	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
1.2V	1.2V	Off	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	Off	1.2V	1.2V	1.2V	1.0V	1.0V	1.0V	STANDBY	1.2V	1.2V	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	Off	1.2V	1.2V	1.0V	1.0V	1.0V	1.2V	STANDBY	1.2V	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	1.2V	Off	1.2V	1.0V	1.0V	1.0V	1.2V	1.2V	STANDBY	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	1.2V	1.2V	Off	1.0V	1.0V	1.0V	1.2V	1.2V	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	Off	Off	1.2V	1.2V	1.0V	1.0V	1.0V	STANDBY	STANDBY	1.2V	1.2V	1.2V	1.2V
0.8V	0.8V	0.8V	Off	1.2V	Off	1.2V	1.0V	1.0V	1.0V	STANDBY	1.2V	STANDBY	1.2V	1.2V	1.2V
0.8V	0.8V	0.8V	Off	1.2V	1.2V	Off	1.0V	1.0V	1.0V	STANDBY	1.2V	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	Off	Off	1.2V	1.0V	1.0V	1.0V	1.2V	STANDBY	STANDBY	1.2V	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	Off	1.2V	Off	1.0V	1.0V	1.0V	1.2V	STANDBY	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	1.2V	Off	Off	1.0V	1.0V	1.0V	1.2V	1.2V	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	Off	1.2V	Off	1.0V	1.0V	STANDBY	STANDBY	STANDBY	1.2V	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	1.2V	Off	Off	1.0V	1.0V	STANDBY	STANDBY	1.2V	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	1.2V	Off	Off	Off	1.0V	1.0V	STANDBY	1.2V	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	1.2V	Off	Off	Off	Off	1.0V	1.0V	1.2V	STANDBY	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	Off	Off	Off	1.0V	1.0V	STANDBY	STANDBY	STANDBY	STANDBY	1.2V	1.2V
1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	Off	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	Off	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V
0.6V	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off	Off
1.0V	1.0V	1.0V	Off	1.2V	1.2V	1.2V	1.0V	1.0V	Off	STANDBY	1.2V	1.2V	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	Off	1.2V	1.2V	1.0V	1.0V	Off	1.2V	STANDBY	1.2V	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	1.2V	Off	1.2V	1.0V	1.0V	Off	1.2V	1.2V	STANDBY	1.2V	1.2V	1.2V
1.0V	1.0V	1.0V	1.2V	1.2V	1.2V	Off	1.0V	1.0V	Off	1.2V	1.2V	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	Off	Off	1.2V	1.2V	1.0V	1.0V	Off	STANDBY	STANDBY	1.2V	1.2V	1.2V	1.2V
0.8V	0.8V	0.8V	Off	1.2V	Off	1.2V	1.0V	1.0V	Off	STANDBY	1.2V	STANDBY	1.2V	1.2V	1.2V
0.8V	0.8V	0.8V	Off	1.2V	1.2V	Off	1.0V	1.0V	Off	STANDBY	1.2V	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	Off	1.2V	Off	1.0V	1.0V	Off	1.2V	STANDBY	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	Off	1.2V	Off	1.0V	1.0V	Off	1.2V	STANDBY	1.2V	STANDBY	1.2V	1.2V
0.8V	0.8V	0.8V	1.2V	1.2V	Off	Off	1.0V	1.0V	Off	1.2V	1.2V	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	Off	1.2V	Off	1.0V	Off	STANDBY	STANDBY	STANDBY	1.2V	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	1.2V	Off	Off	1.0V	Off	STANDBY	STANDBY	1.2V	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	1.2V	Off	Off	Off	1.0V	Off	STANDBY	1.2V	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	1.2V	Off	Off	Off	Off	1.0V	Off	1.2V	STANDBY	STANDBY	STANDBY	1.2V	1.2V
0.6V	0.6V	0.6V	Off	Off	Off	Off	Off	1.0V	Off	STANDBY	STANDBY	STANDBY	STANDBY	1.2V	1.2V
1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V	Off	Off	1.2V	1.2V	1.2V	1.2V	1.2V	1.2V

3.1. Level 1 modes – Level1_MAC, Level1_ALUT, Level1_DMA and Level1_CPU

The Level1 modes are module–level power shutoff strategies. The Level1_MAC, Level1_ALUT, Level1_DMA and Level1_CPU modes shut off power to the Ethernet MAC, the ALUT, the DMA and the CPU respectively while preserving their state. This is achieved by using state retention flops (SR Flops) in these IP's. Level1_MAC, Level1_DMA and Level1_CPU power modes are independent of one another and do not affect the rest of the chip. Level1_ALUT is reached only when all the 4 MAC's are shutoff

Ideally state retention flops should only be used for those flops in an IP that define its state. However as we currently lack this information we will be implementing all the flops in the IP as SR flops. This will cause an area and power penalty.

Entry into the Level 1 modes is under software control (software writes into bits in the power control block).

Wakeup can be through software for all the modes (except Level1_CPU mode)

Wakeup through signal events detected by MAC serial link interface for Level1_MAC is supported (a small power control monitor looks for activity at the MAC RX interface). The Level1_ALUT is also woken up when any of the 4 MAC is awake

Wake through any interrupt for Level1_CPU modes.

3.2. Hibernate Mode

In this mode, the power supply to the entire chip except the portion that controls its wakeup (power control block) will be turned off. Hence the MAC, ALUT, CPU, DMA will be powered down. All memories will be turned off. This mode leads to a complete loss of state and the chip has to be reset after a Hibernate power cycle.

Software writes to a bit in the Power Control Block to enter this state. Wakeup from this state can either be through a wakeup timer in the power control block or through a transition on the wakeup (gpio pin 0) pin.

This mode will showcase the ability of the tools to implement one block that powered (the power control block) while the rest of the chip is powered down.

3.3. Retention mode for On chip memory

Retention for On chip memory is independent of the Level 1 and Hibernate modes described above.

The On chip memory of 256K Words is distributed across 5 voltage islands. If a portion of the address space is unused, its supply can be brought down to the memory retention level. The address range of on chip memory will be split across the 5 voltage islands. Since this mode does not destroy the memory contents, a memory that is accessed intermittently can be placed in its retention state between accesses.

This mode will showcase the ability of the tools to implement voltage islands for memories where the islands can be kept at memory retention levels.

3.4. System Level issues

This section lists out things to watch out for during the implementation and use of the low power modes.

Software should only enable a Level1 mode when the corresponding module is inactive. Inadvertent activation of a module's level1 mode will cause a data overflow/underflow condition for that module.

When a module has been turned off in its Level1 mode, the isolation cells on its output signals should produce values that are the inactive values of these signals. If a signal value is held at the active level, the rest of the chip may respond to it even through the module is inactive. A good example of this is a level sensitive interrupt line and the request signal for AHB bus master ship.