

# OCPEN411 Assignment3 Report

Sizhe Yan 22164982

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File Edit Selection View Go Run Terminal Help
EXPLORER
  ASSIGNMENT3
    README.md
    $ runall.sh
    > bin
    > branch
    > btb
    > inc
    > obj
    > output
      matmul_basic.txt
      matmul_opt1.result
      matmul_opt2.txt
    > prefetcher
    > replacement
    > results
      matmul_basic.result
      matmul_opt1.result
      matmul_opt2.result
    > src
    > tracer
      .champsimconfig_cache
      .clang-format
      .gitignore
    {} champsim_config.json
    $ compile_champsim.sh
    $ config.sh
    $ create_submission.sh
    LICENSE
    Makefile
    README.md
    $ run_all.sh
    $ run_single.sh
    $ submission.tar.gz
    > OUTLINE

ChampSim > results > matmul_basic.result
12 CPU 0 runs /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_basic-720M.champsim
13 CPU 0 Bimodal branch predictor
14 Basic BTB sets: 1024 ways: 8 indirect buffer size: 4096 RAS size: 64
15
16 Warmup complete CPU 0 instructions: 1000003 cycles: 402653 (Simulation time: 0 hr 0 min 0 sec)
17
18 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_basic-720M.champsim
19 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt1-720M.champsim
20 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt2-720M.champsim
21 Heartbeat CPU 0 instructions: 1000004 cycles: 1193862 heartbeat IPC: 0.837615 cumulative IPC: 0.837615
22 Finished CPU 0 instructions: 1000000 cycles: 12775246 cumulative IPC: 0.782764 (Simulation time: 0 hr 0 min 0 sec)
23
24 ChampSim completed all CPUs
25
26 Region of Interest Statistics
27
28 CPU 0 cumulative IPC: 0.782764 instructions: 1000000 cycles: 12775246
29 cpu0_DTLB TOTAL ACCESS: 3073695 HIT: 2953812 MISS: 119883
30 cpu0_DTLB LOAD ACCESS: 2710848 HIT: 2590968 MISS: 119880
31 cpu0_DTLB RFO ACCESS: 362847 HIT: 362844 MISS: 3
32 cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
33 cpu0_DTLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
34 cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
35 cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
36 cpu0_DTLB AVERAGE MISS LATENCY: 9.28107 cycles

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M.champsim.xz
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ cd ../../
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 0
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 1

```

```

File Edit Selection View Go Run Terminal Help
EXPLORER
  ASSIGNMENT3
    README.md
    $ runall.sh
    > bin
    > branch
    > btb
    > inc
    > obj
    > output
      matmul_basic.txt
      matmul_opt1.txt
      matmul_opt2.txt
    > prefetcher
    > replacement
    > results
      matmul_basic.result
      matmul_opt1.result
      matmul_opt2.result
    > src
    > tracer
      .champsimconfig_cache
      .clang-format
      .gitignore
    {} champsim_config.json
    $ compile_champsim.sh
    $ config.sh
    $ create_submission.sh
    LICENSE
    Makefile
    README.md
    $ run_all.sh
    $ run_single.sh
    $ submission.tar.gz
    > OUTLINE

ChampSim > results > matmul_basic.result
35 cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
36 cpu0_DTLB AVERAGE MISS LATENCY: 9.28107 cycles
37 cpu0_ITLB TOTAL ACCESS: 35349 HIT: 35349 MISS: 0
38 cpu0_ITLB LOAD ACCESS: 35349 HIT: 35349 MISS: 0
39 cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0
40 cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
41 cpu0_ITLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
42 cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
43 cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
44 cpu0_ITLB AVERAGE MISS LATENCY: -nan cycles
45 cpu0_STLB TOTAL ACCESS: 119883 HIT: 119721 MISS: 162
46 cpu0_STLB LOAD ACCESS: 119880 HIT: 119718 MISS: 162
47 cpu0_STLB RFO ACCESS: 3 HIT: 3 MISS: 0
48 cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
49 cpu0_STLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
50 cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
51 cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
52 cpu0_STLB AVERAGE MISS LATENCY: 208 cycles
53 cpu0_L1D TOTAL ACCESS: 2837631 HIT: 2571108 MISS: 266523
54 cpu0_L1D LOAD ACCESS: 2359815 HIT: 2093295 MISS: 266520
55 cpu0_L1D RFO ACCESS: 477654 HIT: 477651 MISS: 3
56 cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0
57 cpu0_L1D WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
58 cpu0_L1D TRANSLATION ACCESS: 162 HIT: 162 MISS: 0
59 cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
60 cpu0_L1D AVERAGE MISS LATENCY: 22.5479 cycles

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M.champsim.xz
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ cd ../../
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 0
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 1

```

Basic info

```

EXPLOSER
... C matmul_opt2.c matmul_opt2.txt matmul_opt1.result x matmul_basic.txt
v ASSIGNMENT3
  README.md
  $ runall.sh
  > bin
  > branch
  > btb
  > inc
  > obj
  v output
    matmul_basic.txt
    matmul_opt1.txt
    matmul_opt2.txt
  > prefetcher
  > replacement
  v results
    matmul_basic.result
    matmul_opt1.result
    matmul_opt2.result
  > src
  > tracer
  .champsimconfig_cache
  .clang-format
  .gitignore
  {} champsim_config.json
  $ compile_champsim.sh
  $ config.sh
  $ create_submission.sh
  LICENSE
  Makefile
  README.md
  $ run_all.sh

ChampSim > results > matmul_opt1.result
40 cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
41 cpu0_DTLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
42 cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
43 cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
44 cpu0_DTLB AVERAGE MISS LATENCY: -nan cycles
45 cpu0_DTLB TOTAL ACCESS: 434 HIT: 353 MISS: 81
46 cpu0_DTLB LOAD ACCESS: 434 HIT: 353 MISS: 81
47 cpu0_DTLB RFO ACCESS: 0 HIT: 0 MISS: 0
48 cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
49 cpu0_DTLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
50 cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
51 cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
52 cpu0_DTLB AVERAGE MISS LATENCY: 208 cycles
53 cpu0_L1D TOTAL ACCESS: 2626932 HIT: 2597988 MISS: 28944
54 cpu0_L1D LOAD ACCESS: 2149197 HIT: 2120253 MISS: 28944
55 cpu0_L1D RFO ACCESS: 477654 HIT: 477654 MISS: 0
56 cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0
57 cpu0_L1D WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
58 cpu0_L1D TRANSLATION ACCESS: 81 HIT: 81 MISS: 0
59 cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
60 cpu0_L1D AVERAGE MISS LATENCY: 35.4008 cycles
61 cpu0_L2C TOTAL ACCESS: 29136 HIT: 14427 MISS: 14709
62 cpu0_L2C LOAD ACCESS: 28944 HIT: 14235 MISS: 14709
63 cpu0_L2C RFO ACCESS: 0 HIT: 0 MISS: 0
64 cpu0_L2C PREFETCH ACCESS: 0 HIT: 0 MISS: 0
65 cpu0_L2C WRITEBACK ACCESS: 192 HIT: 192 MISS: 0

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ xz -v3 matmul_opt2-720M.champsim
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01

```

```

EXPLOSER
... C matmul_opt2.c matmul_opt1.result x matmul_opt2.txt matmul_basic.txt
v ASSIGNMENT3
  README.md
  $ runall.sh
  > bin
  > branch
  > btb
  > inc
  > obj
  v output
    matmul_basic.txt
    matmul_opt1.txt
    matmul_opt2.txt
  > prefetcher
  > replacement
  v results
    matmul_basic.result
    matmul_opt1.result
    matmul_opt2.result
  > src
  > tracer
  .champsimconfig_cache

ChampSim > results > matmul_opt1.result
9 VirtualMemory physical capacity: 8588801920 num_ppages: 2096895
10 VirtualMemory page size: 4096 log2_page_size: 12
11
12 CPU 0 runs /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt1-720M.champsim
13 CPU 0 BiModal branch predictor
14 Basic BTB sets: 1024 ways: 8 indirect buffer size: 4096 RAS size: 64
15
16 Warmup complete CPU 0 instructions: 1000001 cycles: 403321 (Simulation time: 0 hr 0 min 0 sec)
17
18 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt1-720M.champsim
19 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt1-720M.champsim
20 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/matmul_opt1-720M.champsim
21 Heartbeat CPU 0 instructions: 10000003 cycles: 6106885 heartbeat IPC: 1.6375 cumulative IPC: 1.59115
22 Finished CPU 0 instructions: 10000000 cycles: 6284765 cumulative IPC: 1.59115 (Simulation time: 0 hr 0 min 0 sec)
23
24 ChampSim completed all CPUs
25
26 Region of Interest Statistics
27
28 CPU 0 cumulative IPC: 1.59115 instructions: 10000000 cycles: 6284765
29
30 cpu0_DTLB TOTAL ACCESS: 2763909 HIT: 2763475 MISS: 434
31 cpu0_DTLB LOAD ACCESS: 2372994 HIT: 2372560 MISS: 434
32 cpu0_DTLB RFO ACCESS: 390915 HIT: 390915 MISS: 0
33 cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
34 cpu0_DTLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
35 cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M.champsim
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.champsim
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ xz -v3 matmul_opt2-720M.champsim
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ cd ../..
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2

```

Opt1 info



```
File Edit Selection View Go Run Terminal Help

EXPLORER
ASSIGNMENTS3
  assignment3.o
  Makefile
  matmul_basic.c
  matmul_basic.h
  matmul_basic.o
  matmul_opt1.c
  matmul_opt1.h
  matmul_opt1.o
  matmul_opt2.c
  matmul_opt2.h
  matmul_opt2.o
  README.md
  runall.sh
  bin
  branch
  btb
  inc
  obj
  output
    matmul_basic.txt
    matmul_opt1.txt
    matmul_opt2.txt
  prefetcher
  replacement
  results
    matmul_basic.result
    matmul_opt1.result
    matmul_opt2.result
  src
  tracer
  npsimconfig.cache

matmul_opt2.c
matmul_opt2.result
matmul_opt2.txt
matmul_basic.txt

ChampSim > results > matmul_opt2.result
17
18 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/n
19 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/n
20 *** Reached end of trace: /home/caesar/Desktop/assignment3/ChampSim/tracer/traces/n
21 Heartbeat CPU 0 instructions: 10000000 cycles: 6881646 heartbeat IPC: 1.45314 cumul
22 Finished CPU 0 instructions: 10000004 cycles: 7259698 cumulative IPC: 1.37747 (Simu
23
24 ChampSim completed all CPUs
25
26 Region of Interest Statistics
27
28 CPU 0 cumulative IPC: 1.37747 instructions: 10000004 cycles: 7259698
29 cpu0_DTLB TOTAL ACCESS: 2367239 HIT: 2366814 MISS: 425
30 cpu0_DTLB LOAD ACCESS: 1940903 HIT: 1940478 MISS: 425
31 cpu0_DTLB RFO ACCESS: 426336 HIT: 426336 MISS: 0
32 cpu0_DTLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
33 cpu0_DTLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
34 cpu0_DTLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
35 cpu0_DTLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
36 cpu0_DTLB AVERAGE MISS LATENCY: 50.6 cycles
37 cpu0_ITLB TOTAL ACCESS: 466174 HIT: 466174 MISS: 0
38 cpu0_ITLB LOAD ACCESS: 466174 HIT: 466174 MISS: 0
39 cpu0_ITLB RFO ACCESS: 0 HIT: 0 MISS: 0
40 cpu0_ITLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
41 cpu0_ITLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
42 cpu0_ITLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
43

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul_opt2-
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M.champ
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-720M.
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ xz -v3 matmul_opt2-720M.
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ cd ../..
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
```

```
File Edit Selection View Go Run Terminal Help

EXPLORER
ASSIGNMENTS3
  assignment3.o
  Makefile
  matmul_basic.c
  matmul_basic.h
  matmul_basic.o
  matmul_opt1.c
  matmul_opt1.h
  matmul_opt1.o
  matmul_opt2.c
  matmul_opt2.h
  matmul_opt2.o
  README.md
  runall.sh
  bin
  branch
  btb
  inc
  obj
  output
    matmul_basic.txt
    matmul_opt1.txt
    matmul_opt2.txt
  prefetcher
  replacement
  results
    matmul_basic.result
    matmul_opt1.result
    matmul_opt2.result
  src
  tracer
  npsimconfig.cache

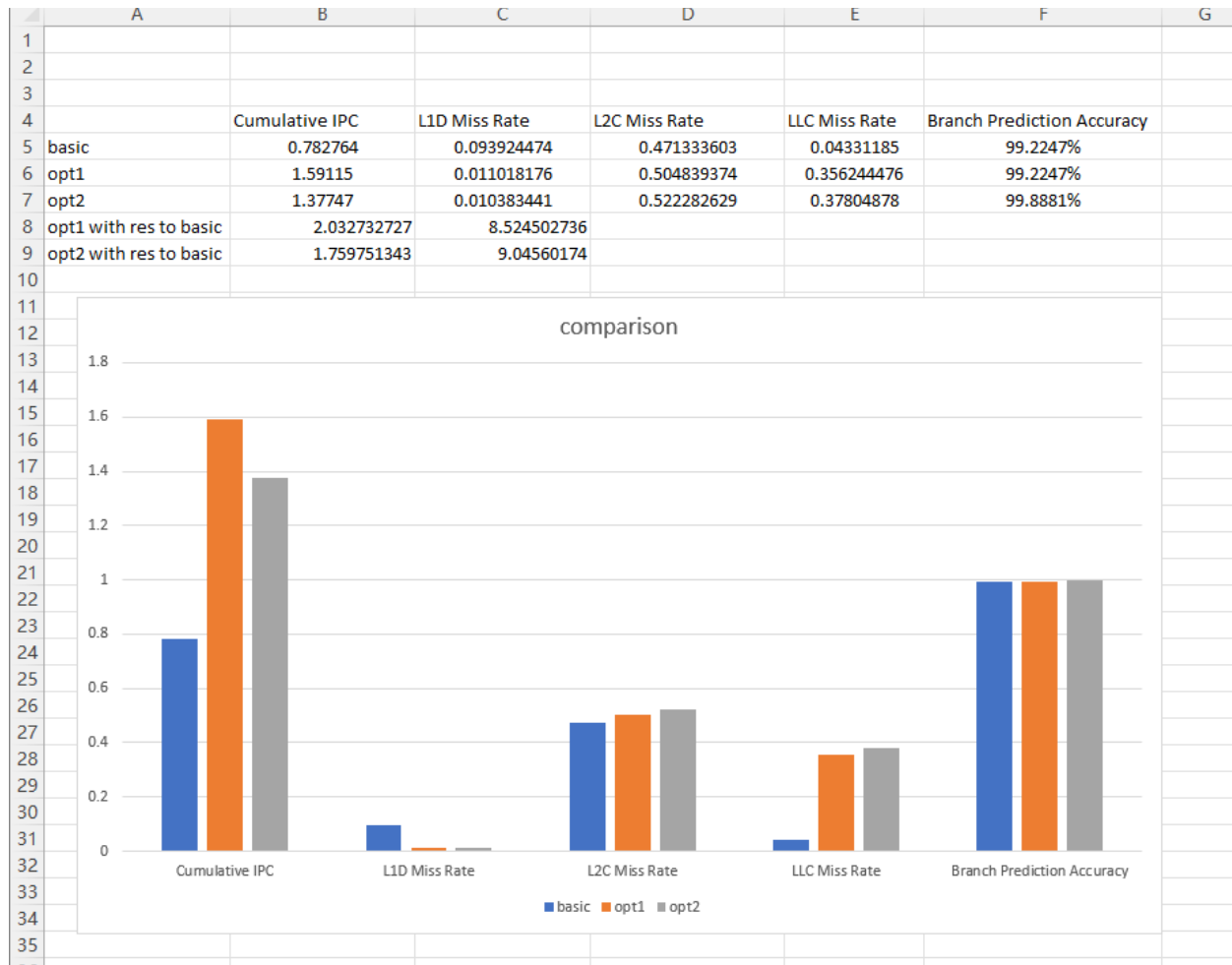
matmul_opt2.c
matmul_opt2.result
matmul_opt2.txt
matmul_basic.txt

ChampSim > results > matmul_opt2.result
43 cpu0_ITLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
44 cpu0_ITLB AVERAGE MISS LATENCY: -nan cycles
45 cpu0_L1I TOTAL ACCESS: 1010287 HIT: 1010287 MISS: 0
46 cpu0_L1I LOAD ACCESS: 1010287 HIT: 1010287 MISS: 0
47 cpu0_L1I RFO ACCESS: 0 HIT: 0 MISS: 0
48 cpu0_L1I PREFETCH ACCESS: 0 HIT: 0 MISS: 0
49 cpu0_L1I WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
50 cpu0_L1I TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
51 cpu0_L1I PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 U
52 cpu0_L1I AVERAGE MISS LATENCY: -nan cycles
53 cpu0_STLB TOTAL ACCESS: 425 HIT: 340 MISS: 85
54 cpu0_STLB LOAD ACCESS: 425 HIT: 340 MISS: 85
55 cpu0_STLB RFO ACCESS: 0 HIT: 0 MISS: 0
56 cpu0_STLB PREFETCH ACCESS: 0 HIT: 0 MISS: 0
57 cpu0_STLB WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
58 cpu0_STLB TRANSLATION ACCESS: 0 HIT: 0 MISS: 0
59 cpu0_STLB PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0
60 cpu0_STLB AVERAGE MISS LATENCY: 208 cycles
61 cpu0_L1D TOTAL ACCESS: 2585559 HIT: 2558712 MISS: 26847
62 cpu0_L1D LOAD ACCESS: 2158295 HIT: 2131448 MISS: 26847
63 cpu0_L1D RFO ACCESS: 427179 HIT: 427179 MISS: 0
64 cpu0_L1D PREFETCH ACCESS: 0 HIT: 0 MISS: 0
65 cpu0_L1D WRITEBACK ACCESS: 0 HIT: 0 MISS: 0
66 cpu0_L1D TRANSLATION ACCESS: 85 HIT: 85 MISS: 0
67 cpu0_L1D PREFETCH REQUESTED: 0 ISSUED: 0 USEFUL: 0 U
68 cpu0_L1D AVERAGE MISS LATENCY: 37.3797 cycles

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ ls
matmul_basic-720M.champsim.xz matmul_opt1-720M.champsim matmul_opt1-720M.champsim.xz matmul
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ rm matmul_opt2-720M
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ zx -v3 matmul_opt2-
zx: command not found
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ xz -v3 matmul_opt2-
matmul_opt2-720M.champsim (1/1)
100 % 133.1 KiB / 183.1 MiB = 0.001 0:01
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim/tracer/traces$ cd ../..
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
caesar@caesar-virtual-machine:~/Desktop/assignment3/ChampSim$ bash run_single.sh 2
```

Opt2 info

## Comparison



## OPT1:

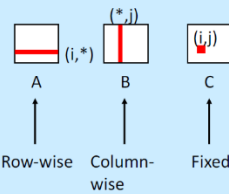
OPT1 analyse the pattern of the matrix multiplication of the original code. To increase the row-wise special locality, the change is from the logic of first picture to second. With reference to

<https://cs.brown.edu/courses/cs033/lecture/18cacheX.pdf>

## Matrix Multiplication (ijk)

```
/* ijk */
for (i=0; i<n; i++) {
  for (j=0; j<n; j++) {
    sum = 0.0;
    for (k=0; k<n; k++)
      sum += a[i][k] * b[k][j];
    c[i][j] = sum;
  }
}
```

Inner loop:



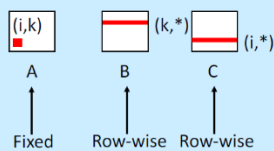
Misses per inner loop iteration:

|          |          |          |
|----------|----------|----------|
| <u>A</u> | <u>B</u> | <u>C</u> |
| 0.25     | 1.0      | 0.0      |

## Matrix Multiplication (kij)

```
/* kij */
for (k=0; k<n; k++) {
  for (i=0; i<n; i++) {
    r = a[i][k];
    for (j=0; j<n; j++)
      c[i][j] += r * b[k][j];
  }
}
```

Inner loop:



Misses per inner loop iteration:

|          |          |          |
|----------|----------|----------|
| <u>A</u> | <u>B</u> | <u>C</u> |
| 0.0      | 0.25     | 0.25     |

## OPT2:

OPT2 is based on OPT1 with another buffer called temp, OPT2 is with 2 loads 1 store instructions per loop. The idea is to use a buffer called temp to generate the result of matrix b, as it is in the loop of "k" and we are adding k for each loop, thus, this action is with special locality to increase the accuracy of prediction