5-bit subtractor

Inputs are A(5-bit) and B(5-bit), the outputs are Result(5-bit) and Overflow(1-bit).

Raise your hand after each part is completely finished.

- Implement the design with structural Verilog (only logic gates)
  - You have to write at 3 modules. The main module is _5_bit_subtractor. For submodules:
    - _1_bit_FA
    - _1_bit_HA
  - Running your designs (_1_bit_FA & _5_bit_subtractor) on the simulator take a screenshots (add your project folder).

Total Time: 40min