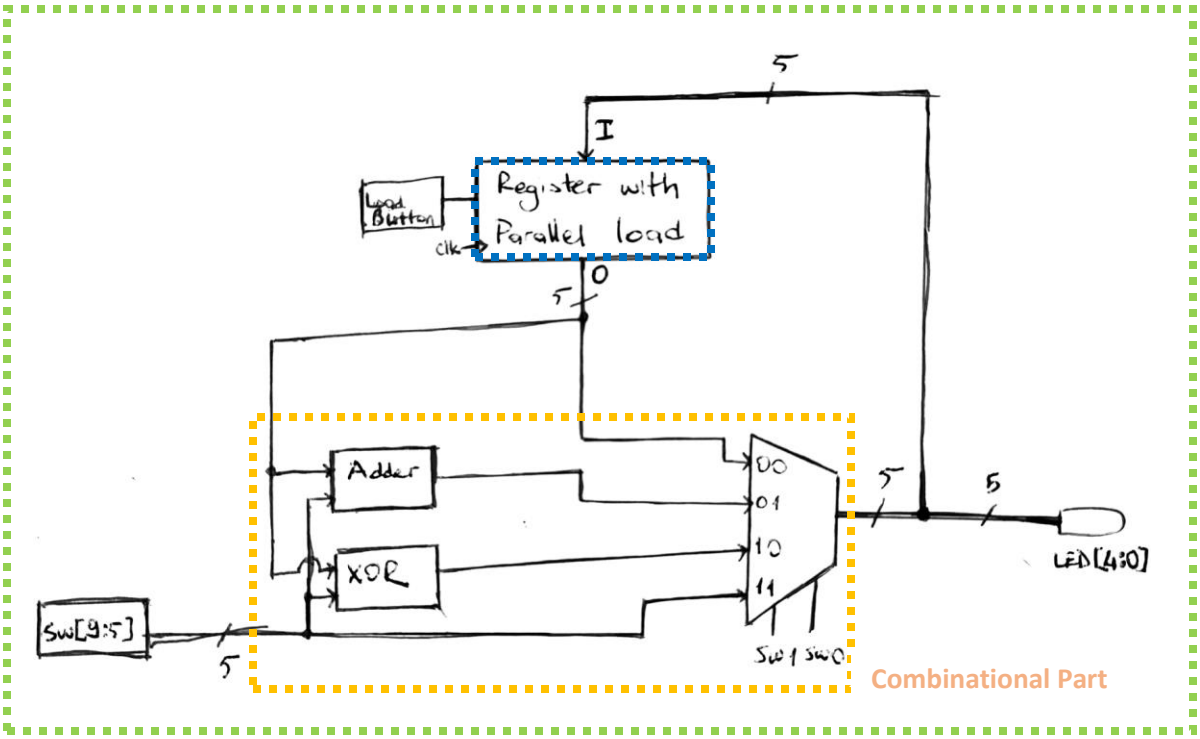
Designing a Custom Datapath



- All wires (except those that connect to SW1, SW0, clk, and Load Button) are **5 bits.**
- The **register module should assign the flip-flops after the load button is pressed.** If the value of load button is one(1), it's pressed. It must have multiplexers and flip-flops in it. You can use the ternary operator (?:) to implement multiplexers in the register module.
- You are **free to choose any Verilog style** to implement the modules. The only requirement is to create separate modules for each component.

- You must write **at least these 3 modules;**
  - Combinational part
    - Includes Adder , Xor , Mux designs
  - Register with parallel load
  - Main
- You need to upload unedited & uncut screenshots on your project folder. **Take two screenshots;**
  - show your entire screen when Quartus is on and compiled,
  - run your main design on the simulator to show square waves.

Total time : 50min