1) A)

$$F = YZ + \bar{X}YW + XZ\bar{W} + X\bar{Y}\bar{Z}$$

XY\\ZW	00	01	11	10
00	0 $_0$	0 $_1$	0 $_3$	0 $_2$
01	0 $_4$	1 $_5$	1 $_7$	1 $_6$
11	0 $_{12}$	0 $_{13}$	1 $_{15}$	1 $_{14}$
10	1 $_8$	1 $_9$	0 $_{11}$	1 $_{10}$

K-map for F function

1) B)

X	Y	Z	W	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Truth Table for F function

4×16 Decoder

16 × 1 Multiplexer (Mux)

X Y Z W
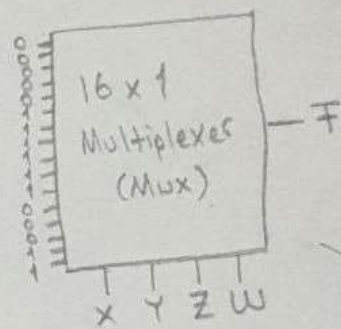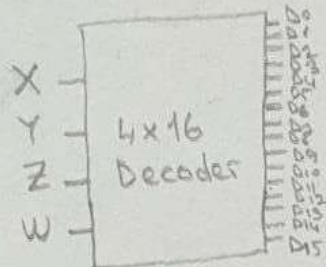
This belongs to question 1)C)

It is continuing on the other page ....

1) B)

X

Y

Z

W

d15 d14 d13 d12 d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

Decoder

1) C

X

Y

Z

W

d15 d14 d13 d12 d11 d10 d9 d8 d7 d6 d5 d4 d3 d2 d1 d0

F
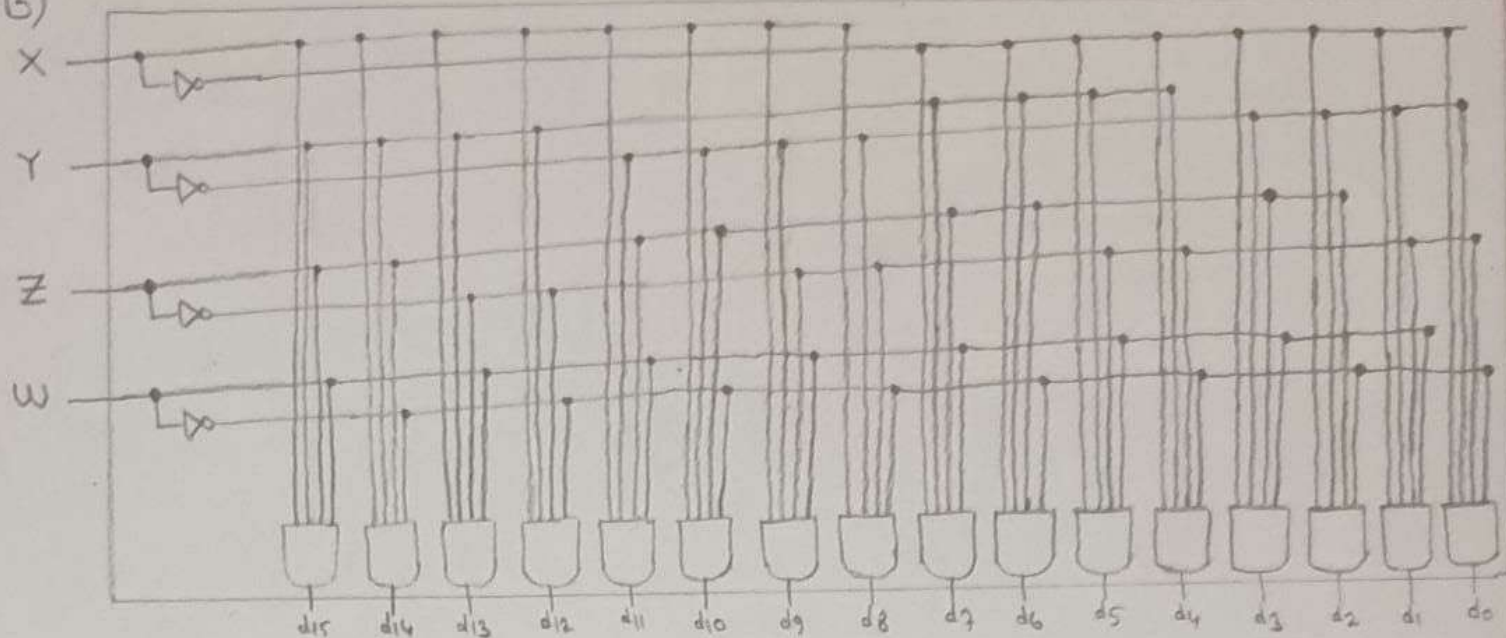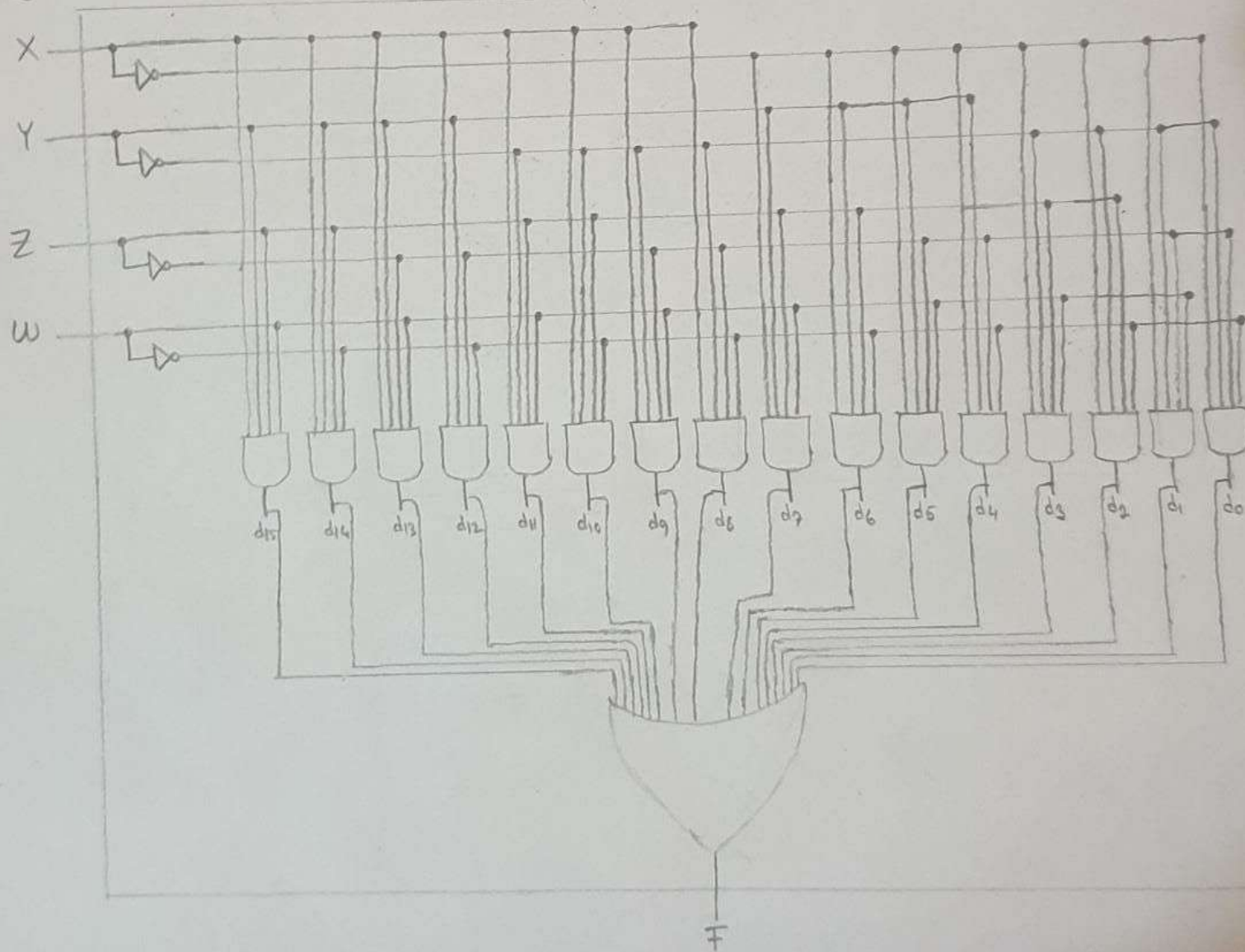
Multiplexer

2) A)

X	Y	Z	L
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Truth table

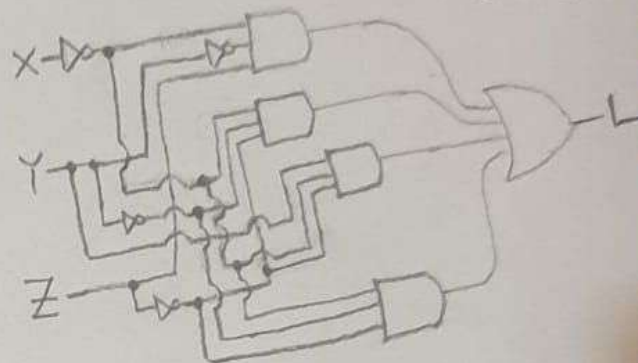| X\YZ	00	01	11	10
0	1_0	1_1	0_3	1_2
1	0_4	0_3	0_3	0_6

$$L = \bar{X}\bar{Y} + \bar{X}\bar{Z}$$

$$L = \bar{X}\bar{Y}(Z + \bar{Z}) + \bar{X}\bar{Z}(Y + \bar{Y})$$

$$L = \bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Z}Y + \bar{X}\bar{Z}\bar{Y}$$

Canonical form $= \bar{X}\bar{Y}Z + \bar{X}\bar{Y}\bar{Z} + \bar{X}\bar{Z}Y + \bar{X}\bar{Z}\bar{Y}$

↓ circuit

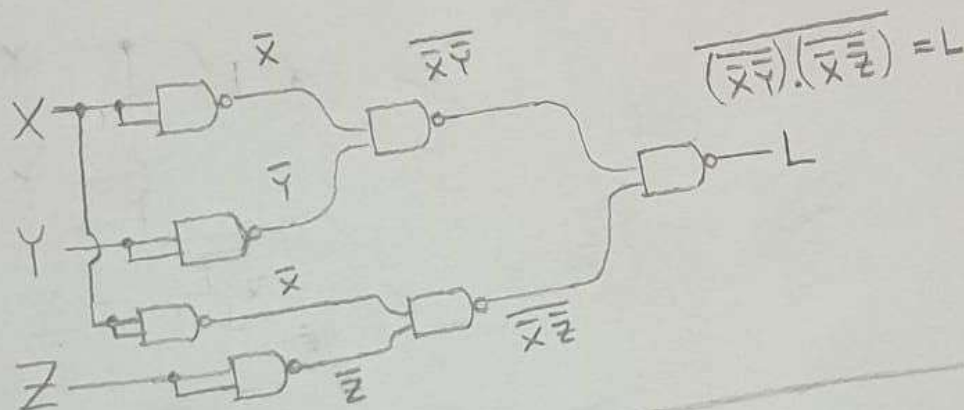## 2) B)
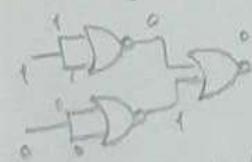
$$L = \bar{X}\bar{Y} + \bar{X}\bar{Z}$$

$$\bar{\bar{L}} = \overline{\bar{X}\bar{Y} + \bar{X}\bar{Z}}$$

$$\bar{\bar{L}} = \overline{(\overline{\bar{X}\bar{Y}}) \cdot (\overline{\bar{X}\bar{Z}})} = L$$

$$\overline{(\overline{\bar{X}\bar{Y}}) \cdot (\overline{\bar{X}\bar{Z}})} = L$$
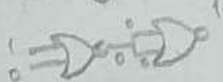

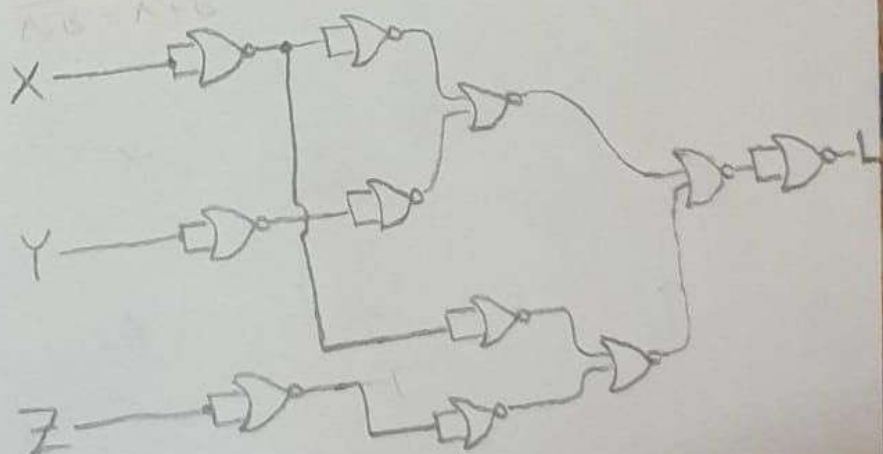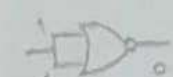## 2) C) $L = \bar{X}\bar{Y} + \bar{X}\bar{Z}$

AND gate

OR gate

Truth table is valid. It is tested.

NOR truth table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0

Inverter

3)

S_0

S_1

$d_3[3]\ d_2[3]\ d_1[3]\ d_0[3]$
$d_3\ d_2\ d_1\ d_0$
S_0 4x1
S_1 Mux

$d_3[2]\ d_2[2]\ d_1[2]\ d_0[2]$
$d_3\ d_2\ d_1\ d_0$
S_0 4x1
S_1 Mux

$d_3[1]\ d_2[1]\ d_1[1]\ d_0[1]$
$d_3\ d_2\ d_1\ d_0$
S_0 4x1
S_1 Mux

$d_3[0]\ d_2[0]\ d_1[0]\ d_0[0]$
$d_3\ d_2\ d_1\ d_0$
S_0 4x1
S_1 Mux

O_3 O_2 O_1 O_0
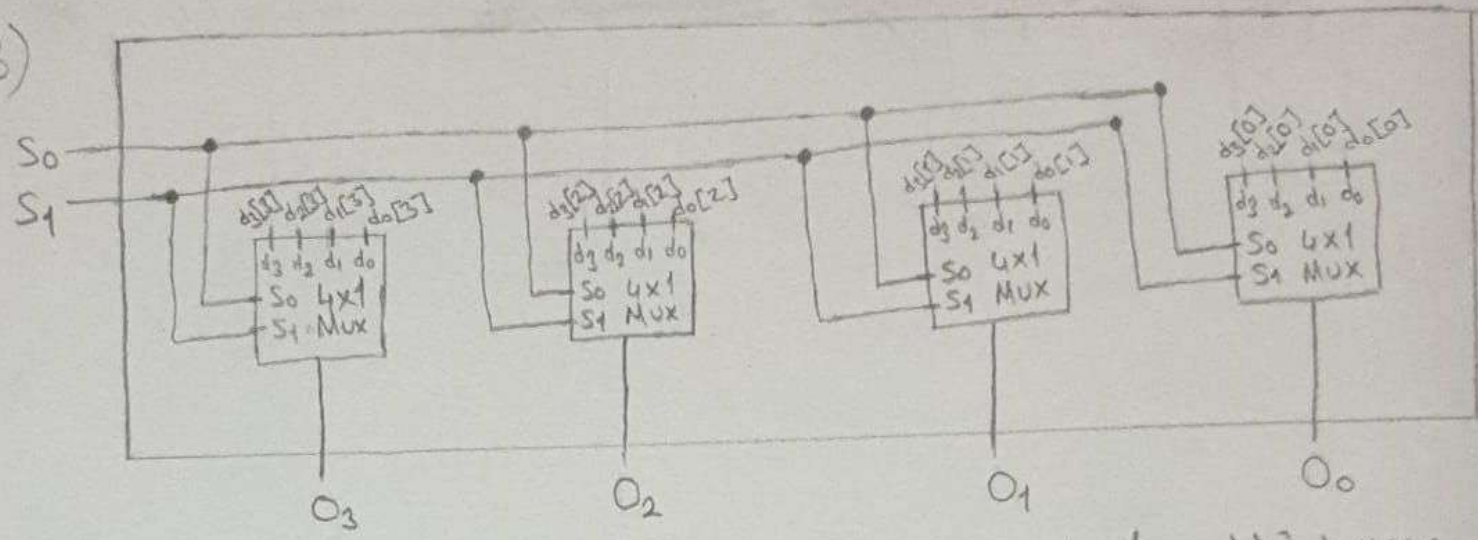
It is a 4-bit 4x1 multiplexer that uses four 4x1 multiplexers.