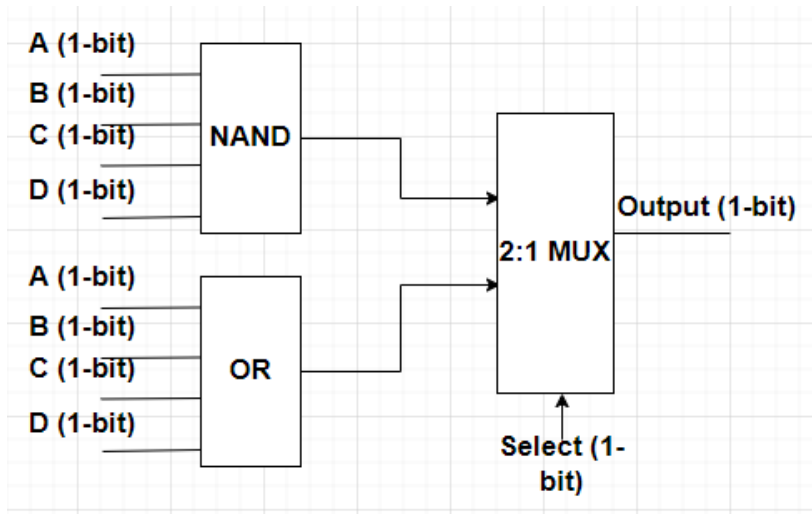## Problem – Combinational Design

Raise your hand after each part is completely finished.

- Implement the design with ONLY structural Verilog
  - You have to write these modules, take screenshots after successfully compile:
    - Your main module
    - _4nand
    - _4or
    - _2to1_mux

  - Running your designs (main module & _2to1_mux) on the simulator take screenshots (add your project folder).

Total Time: 45min