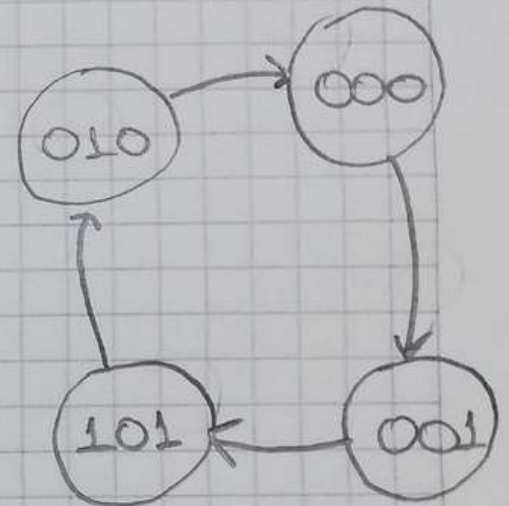


Homework 5

Student ID: 2021510010

$\downarrow \text{mod } 8$
2, 0, 2, 1, 5, 1, 0, 0, 1, 0 \rightarrow 2, 0, 1, 5
 \downarrow 010 \downarrow 000 \downarrow 001 \downarrow 101

Q(+)	Q(+++)	J1	K1	J2	K2	J3	K3
000	001	0	X	0	X	1	X
001	101	1	X	0	X	X	0
010	000	0	X	X	1	0	X
011	000	0	X	X	1	0	1
100	000	X	1	0	X	0	X
101	010	X	1	1	X	X	1
110	000	X	1	X	1	0	X
111	000	X	1	X	1	X	1



\Rightarrow for J1

Q1 \ Q2 Q3	00	01	11	10
0	0	1	0	0
1	X	X	X	X

$\rightarrow Q_2' Q_3$

\Rightarrow for K1

Q1 \ Q2 Q3	00	01	11	10
0	X	X	X	X
1	1	1	1	1

\Rightarrow for J2

Q1 \ Q2 Q3	00	01	11	10
0	0	0	X	X
1	0	1	X	X

$\rightarrow Q_1 Q_3$

\Rightarrow for K2

Q1 \ Q2 Q3	00	01	11	10
0	X	X	1	1
1	X	X	1	1

\Rightarrow for J3

Q1 \ Q2 Q3	00	01	11	10
0	1	X	0	0
1	0	X	X	0

$\rightarrow Q_1' Q_2'$

\Rightarrow for K3

Q1 \ Q2 Q3	00	01	11	10
0	X	0	1	X
1	X	1	1	X

$\rightarrow Q_1 + Q_2$

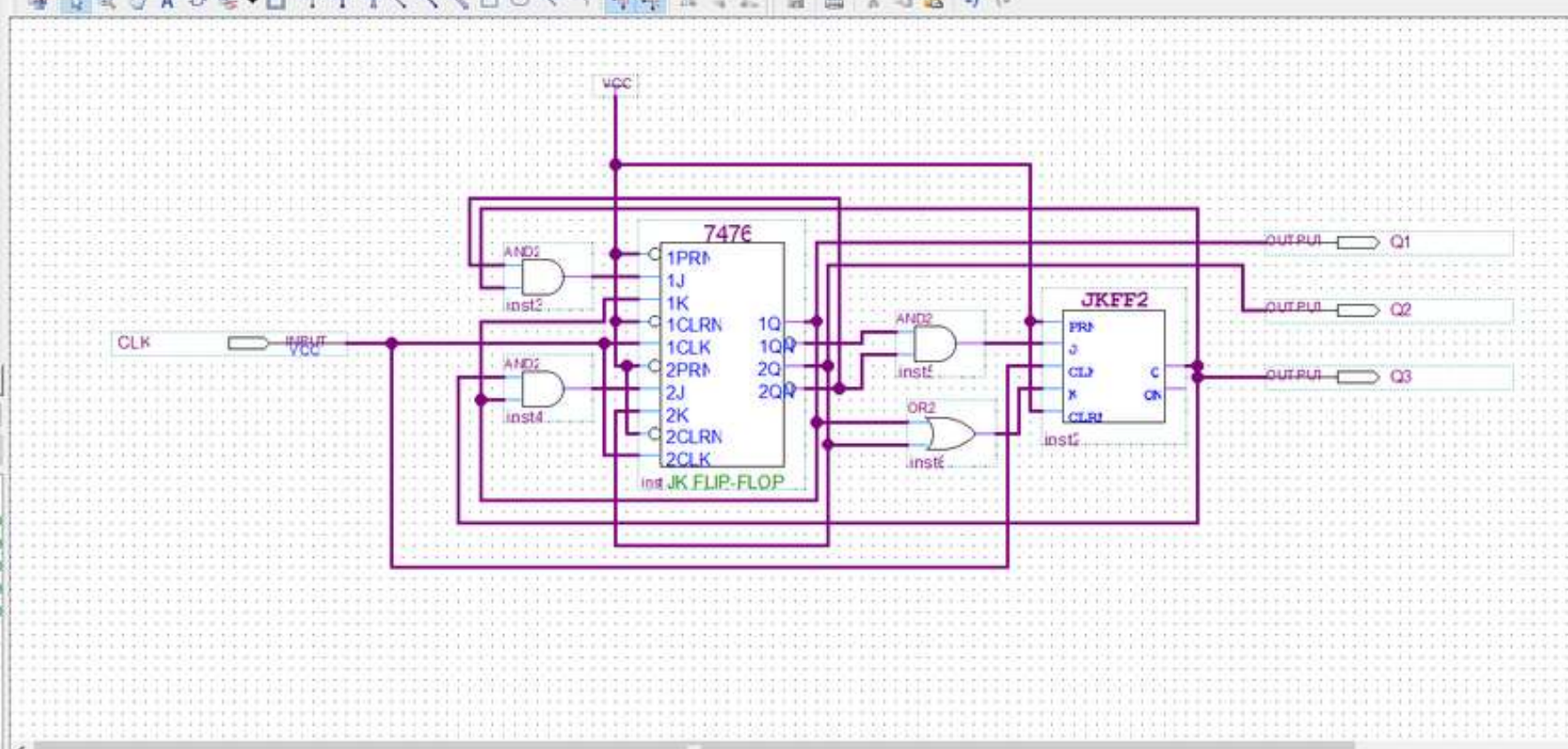
Entity
Cyclone III: EP3C16F484C6
2021510010_cagri_aydin_hw5
7476:inst
jkff2:inst2

Hierarchy Files Design Units

Tasks

Flow: Compilation Customize...

Task	
Compile Design	00:00
Analysis & Synthesis	00:00
Fitter (Place & Route)	00:00
Assembler (Generate programming files)	00:00
TimeQuest Timing Analysis	00:00
EDA Netlist Writer	
Program Device (Open Programmer)	



332102 Design is not fully constrained for setup requirements
332102 Design is not fully constrained for hold requirements
Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings
293000 Quartus II Full Compilation was successful. 0 errors, 11 warnings

System Processing (109)

