CME 2206 – LAB PROJECT

ASSIGNMENT 1 – ALU DESIGN

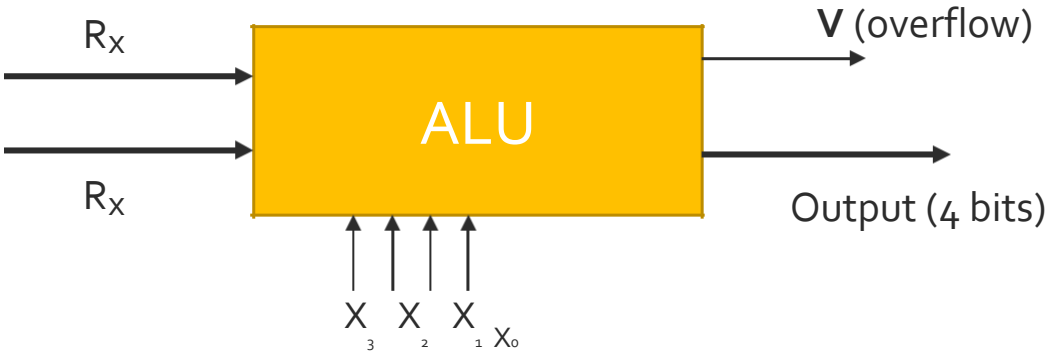

Figure 1 Block Diagram of ALU

You are expected to implement an ALU design that is suitable for your common bus (assignment-1) and save it as a block diagram ('symbol file') with the name, "ALU" as shown in Figure 1. Test and simulate your implementation by applying supported operations listed in Table 1. The ALU must support following operations that is selected by the input control X**[3..0].**

X[3..0]	CODE	OPERATION	SYMBOL	DESCRIPTION
0	0000	$R_d \leftarrow R_S \times 2$	DBL	Double content of R_S and store result in R_d
1	0001	$R_d \leftarrow R_S/2$	DBT	Divide content of R_S by 2 and store result in R_d
2	0010	$R_d \leftarrow R_S \wedge S_2$	AND	R_S AND S_2 (can be R_x or data) and store result in R_d
3	0011	$R_d \leftarrow \overline{R_S}$	NOT	Complement Rs content and load the result into Rd
4	0100	$R_d \leftarrow R_S \oplus S_2$	XOR	XOR contents of S1 and S2 and store result in Rd
5	0101	$R_d \leftarrow R_S + S_2$	ADD	Add R_S to S_2 (can be R_x or data) and store result
6	0110	$R_d \leftarrow R_S + 1$	INC	Increment content of R_S and store result in R_d

Table 1 ALU Operation Control