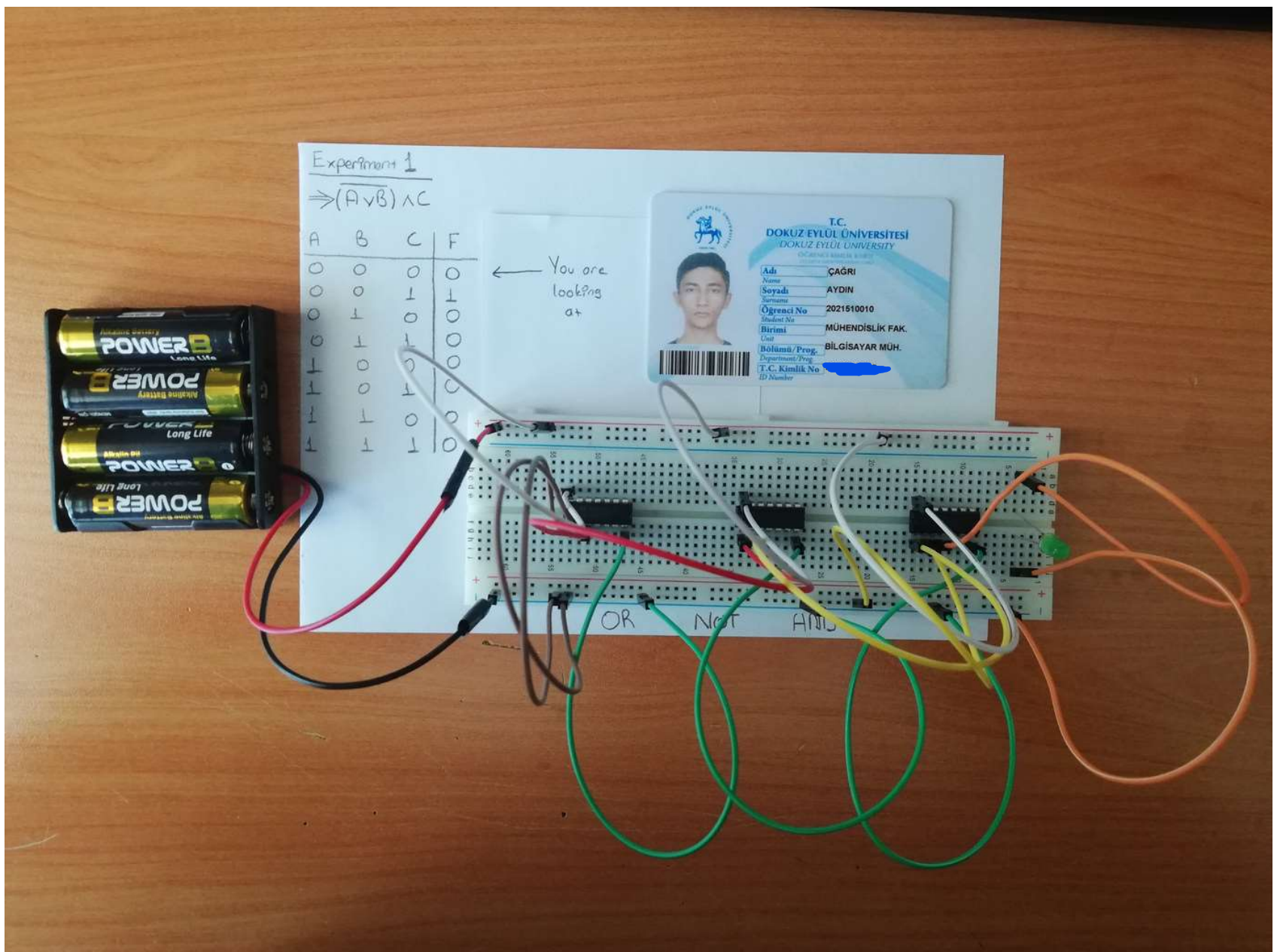
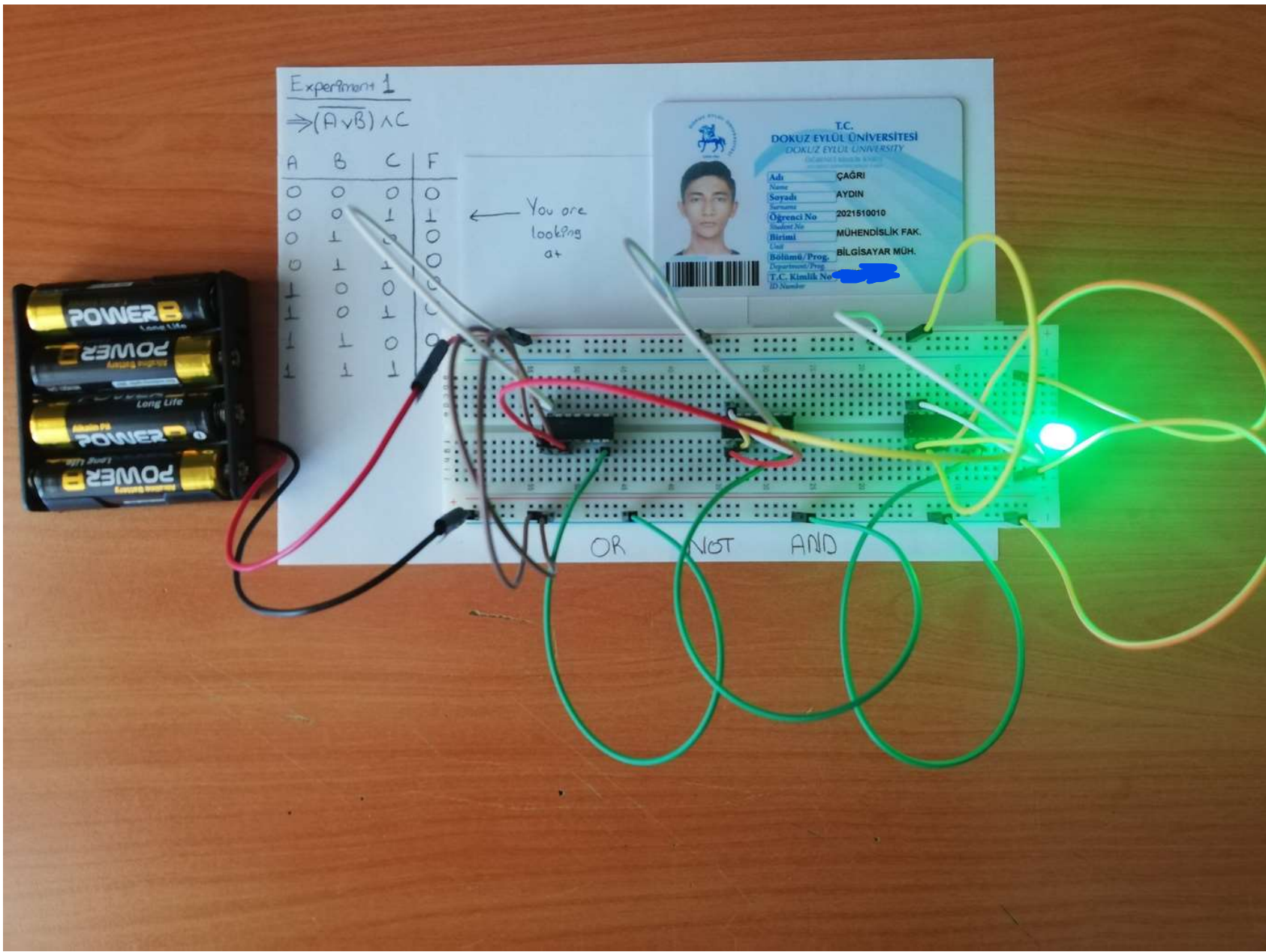


Experiment 1



Quartus II 64-Bit - C:/altera/13.0sp1/2021510010_cagri_aydin/Homework_1_exp_1 - Homework_1_exp_1

File Edit View Project Assignments Processing Tools Window Help

Homework_1_exp_1

Project Navigator

Entity

Cyclone III: EP3C16F404C6

Homework_1_exp_1

Homework_1_exp_1.bdf

Compilation Report - Homework_1_exp_1

Task

Flow: Compilation

Task

Compile Design 00:00

Analysis & Synthesis 00:00

Fitter (Place & Route) 00:00

Assembler (Generate programming files) 00:00

TimeQuest Timing Analysis 00:00

EDA Netlist Writer

Program Device (Open Programmer)

Messages

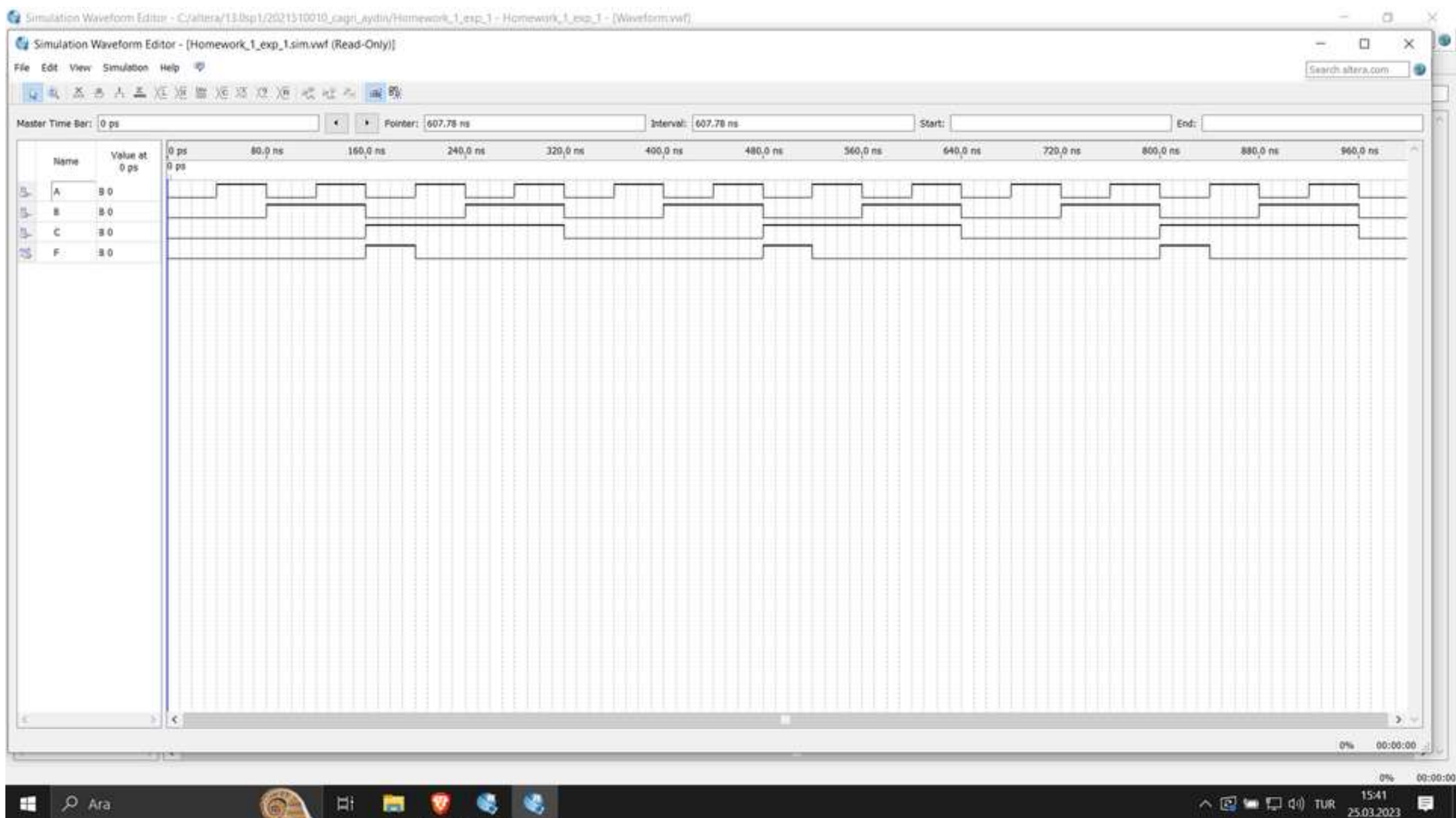
253000 Quartus II Full Compilation was successful. 0 errors, 12 warnings

System Processing (113)

801,371 100% 00:00:09

Ara 15:20 25.03.2023

```
graph LR; A[INPUT VCC] --> OR2[OR2 inst2]; B[INPUT VCC] --> OR2; OR2 --> NOT[NOT inst1]; NOT --> AND2[AND2 ins1]; C[INPUT VCC] --> AND2; AND2 --> F[OUTPUT F];
```



Experiment 2

