CME 2206 Computer Architecture

Lab 1

Background

A **sequential circuit** consists of **a combinational circuit** and **storage elements** that together form a feedback system. **Synchronous sequential circuit** is a system whose behavior can be defined from the knowledge of its signals at **discrete instants of time**.

The **storage elements** are devices capable of storing binary information within them. The binary information stored at any given time defines the **state** of the sequential circuit.

Flip-flops are clocked storage elements. Each flip-flop can hold one bit of information.

J K Flip Flop

Characteristic Table

J	K	Q(t+1)	
0	0	Q(t)	No Change
0	1	0	Clear to 0
1	0	1	Set to 1
1	1	Q'(t)	Complement

Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

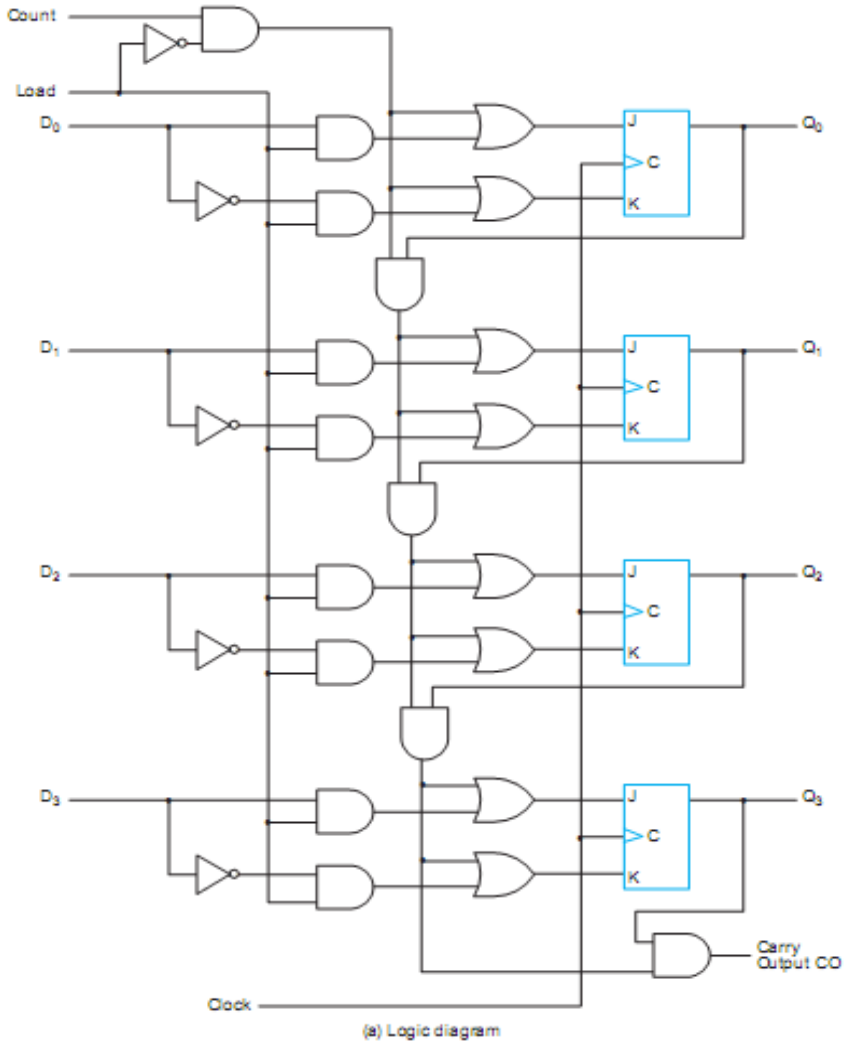
A **register** is a group of flip-flops with each flip-flop capable of storing one bit of information. An "*n*-bit" **register** has *n* flip-flops, and is capable of storing any binary information of "n" bits. "**Registers with Parallel-Load**" have the capability of loading their content parallelly in one clock cycle.

A **counter** is a register that goes through a predetermined sequence of states upon the application of input pulses. Binary counters are counters that follows the binary number sequence.

Binary Counter with Parallel Load can set the binary counter from input lines.

Experiment – 4 Bit Binary Counter with Parallel Load

a) Design a **4-bit Binary Counter with parallel load** in Quartus II by using J-K flip flops and necessary logic gates as shown in the figure below.



(a) Logic diagram

b) Design a **4 bit Binary Counter with parallel load** in Quartus II by using ***lpm_counter.***