

Design of Universal Digital Flight Control Bus Acquisition Unit

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Abstract-The data format of the digital flight control bus (FTI) output by the flight control computer of different models is not standardized, and it does not match the data format of the general acquisition system, which makes it impossible to collect it directly. The existing flight controller collector is large in size, high in cost, and complex in-system programming and maintenance, which does not meet the strict requirements of the airborne environment for the size, weight, and maintenance of the test equipment. In this paper, we design a general-purpose integrated and modular FTI signal acquisition scheme that converts FTI signals into standard signals for output to other test equipment. This solution improves the flexibility and maintainability of test equipment, reduces test costs, and provides design ideas for the integration and modularization of other test equipment in the future.

Keywords-digital flight control bus, airborne environment, signal conversion, integration

I. INTRODUCTION

The digital flight control bus is a non-standard bus, and the data format of different models is different, so it is necessary to design a special acquisition system, and the acquisition system is difficult to standardize. The airborne environment has very demanding requirements for the size, weight, and maintainability of the test equipment. The existing flight control bus collector collects digital flight control data as an independent device, causing large weight pressure and waste of equipment installation space, and the programming is complex, and small software changes can increase the workload of data acquisition, processing, and monitoring, increases the maintenance difficulty of the test system, and reduces the

efficiency of the test system update.^[1]In view of the above problems, the flight control data acquisition system should try to control the volume, quality, and cost of the equipment, and at the same time take into account the versatility and scalability of the equipment, to reduce the maintenance difficulty of the test system.

II. THE SYSTEM DESIGN SCHEME

In view of the shortcomings of the existing acquisition equipment, an integrated and modular FTI signal acquisition scheme is designed to demodulate the original FTI signal into a standard signal. The acquisition system is divided into power supply, signal conditioning, level translation, and processor modules, and adopts the EP3C series of ALTERA series devices integrated with processor IP soft core design. The Verilog hardware description language allows for flexible configuration of internal signal processing logic.^[2]

As shown in Figure 1, the FTI acquisition unit is mainly composed of four parts, namely the power module, the signal conditioning module, the level translation module, and the processor. The power module processes the 5V power supply and outputs voltages of different amplitudes for other modules. The signal conditioning module performs impedance matching and shaping filtering on the input signal. The level translation module converts the data output from the processor from TTL level to RS422 level output for external devices. The processor completes the parsing cache of FTI data and the sending of 422 data.

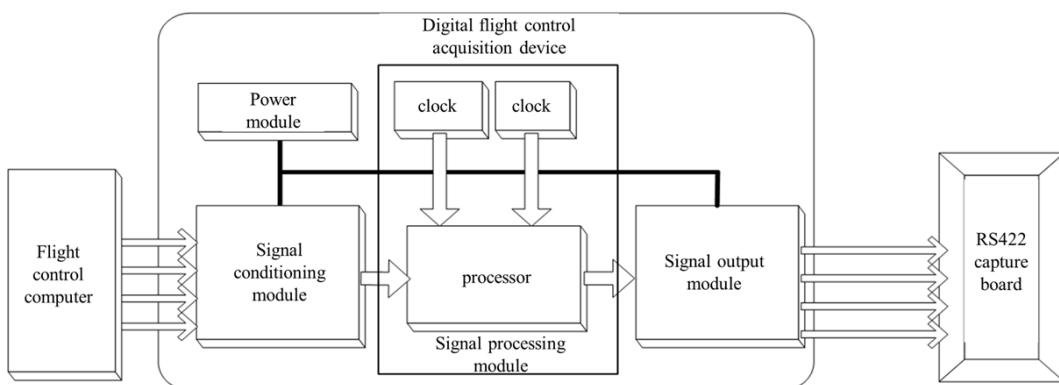


Figure 1. Schematic diagram of the system structure of the FTI acquisition unit.

The FTI acquisition unit adopts an embedded design architecture, and the FPGA is used as the processor for the analysis, buffering, and forwarding of flight control data. The firmware program is written in the Verilog HDL hardware

description language. The FPGA selected ALTERA's EP3C series devices, which met the design requirements in terms of speed and resources.^[3]

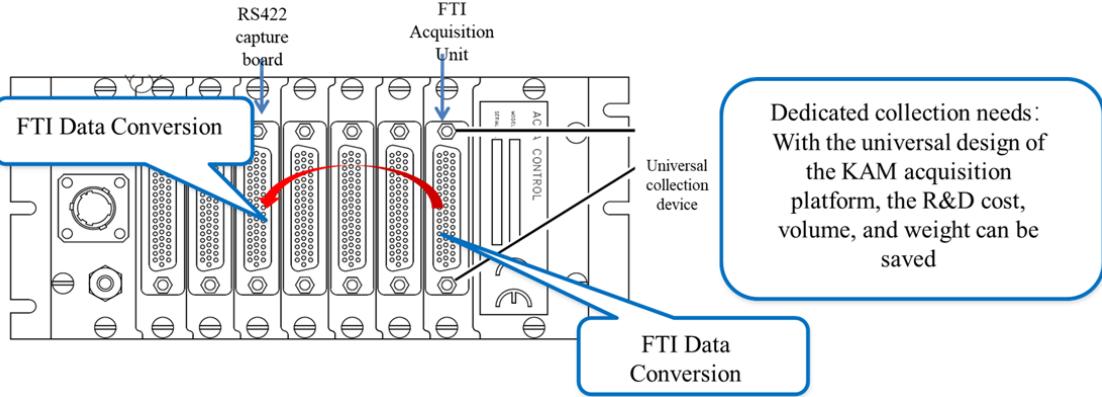


Figure 2. Schematic diagram of the extended platform design.

The FTI signal conversion and acquisition scheme adopts an extended platform design, mainly with the help of a general acquisition system as the platform, and the general design of the board is used, and the appearance and structure are shown in Figure 2. The FTI acquisition unit is directly charged from the bottom plate of the general collector chassis through the power supply connector of the lower base plate, and the FTI acquisition unit and RS422 acquisition board are stuck in the same collector chassis in the layout of the test system, which optimizes the layout of the test system and reduces the difficulty of system maintenance. The structural design of the universal board greatly enhances the flexibility of the system, and the replacement, inspection, and maintenance of equipment are also more convenient.

The FTI acquisition unit adopts the general collector board structure design, which draws power from the bottom plate of the universal collector chassis, simplifies the power module design of the FTI acquisition unit, and enhances the stability of the system power supply. The expandable platform design makes it easier to layout, replace and maintain the equipment. At the same time, this scheme does not need to design a shell for the acquisition unit separately, simplifies the design of signal conversion and acquisition scheme, can reduce the cost and difficulty of R&D to a certain extent, shortens the cycle of

R&D, and also provides a reference scheme that can enhance the scalability and versatility of the system for similar special acquisition requirements in the future.

III. FLIGHT CONTROL DATA COLLECTION AND FORWARDING

The flight control data adopts the RS422 level data encoded by Manchester II, the data is transmitted in a fixed period in the format of packets, and each packet data is composed of synchronous words and data words.

A. FTI data conversion encoding

Each data word is composed of 20 bits, of which the first 3 bits are synchronous bits, the middle 4~19 bits are effective information bits, and the 20th bit is the parity check bit. The data packet starts with the synchronization word and follows the data word of fixed length, and the synchronization bit analysis, data bit analysis, data synchronization word, and data packet length of different models of digital flight control are different, and they need to be parsed and processed into standard data packets, and the existing general acquisition system is used to complete the collection. Figure 3 shows the data format and conversion mode of the digital flight control signal of a certain type of aircraft.

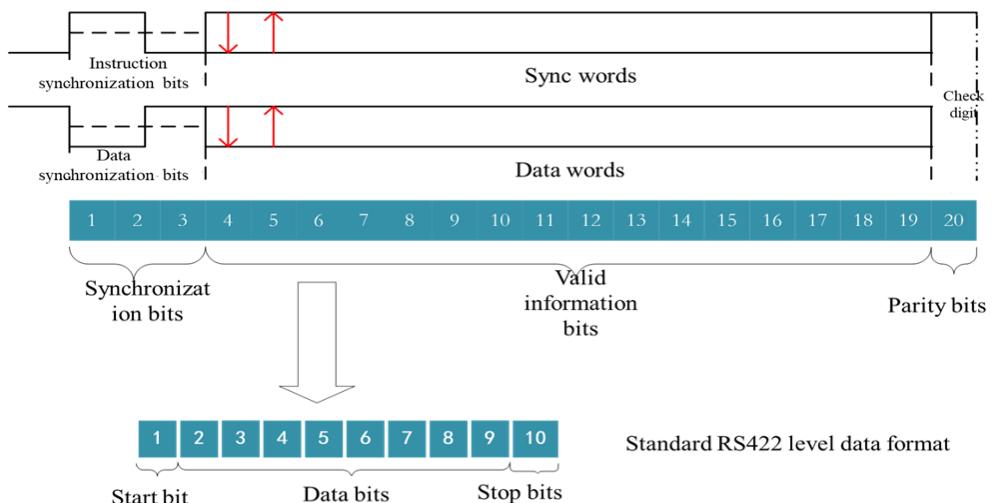


Figure 3. Schematic diagram of signal format conversion.

When the flight control signal enters the FTI acquisition unit, the FTI acquisition unit first adjusts the signal and converts the level, and then parses and forwards it to the standard data output in real time. The main function of the FPGA of the FTI acquisition unit is to realize the analysis, buffering, data format conversion, encoding, and data forwarding functions of the flight control data. The flight control data is collected at the front end, and photoelectric isolation is adopted between the flight control data and the back-end acquisition and recording equipment to reduce the impact on the working status of the flight control computer and the back-end equipment.^[4]

Figure 4 shows the post-processing process of the FPGA of the processor module after receiving the flight controller data. The following process is used to complete the analysis, verification, data format conversion, and transmission of the signal.

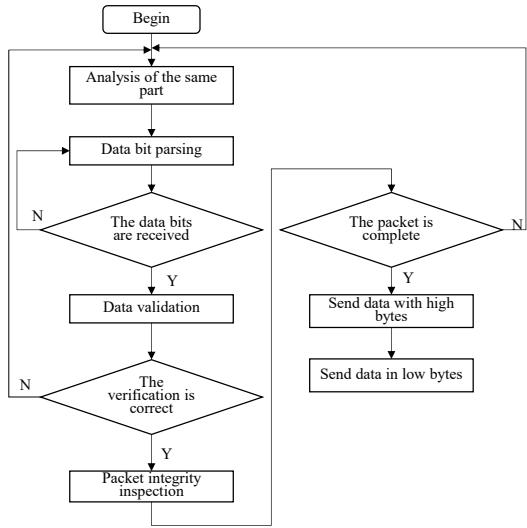


Figure 4. Schematic diagram of FPGA processing logic.

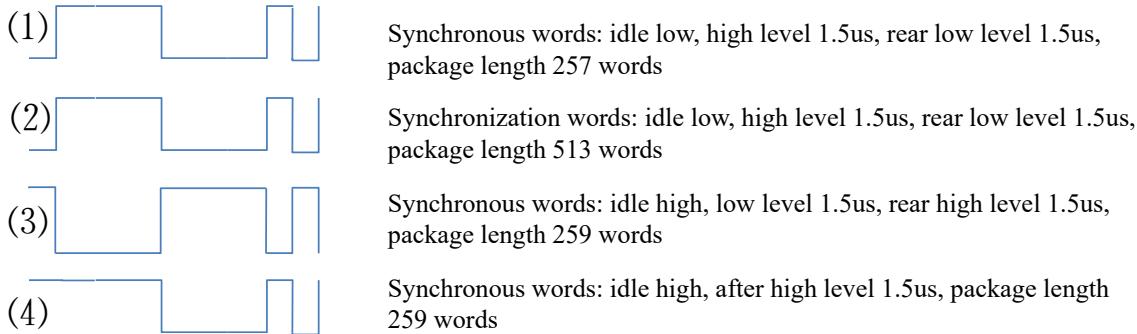


Figure 5. Flight controller data format.

a) Synchronous word recognition

The synchronization word needs to be determined based on the idle state and synchronization bits, as shown in Figure 5;

(1) (2) Two flight controller data formats, low level at idle, high level 1.5 us after the signal jump, then low level 1.5 us, followed by data bits;

1) Synchronization bit analysis, the signal high level for 1.5 us to change to low level and 1.5 us for the instruction synchronization bit, followed by the data for a frame of data synchronization word; signal low level for 1.5 us to change to high level and last for 1.5 us for data synchronization bit, followed by the data word for a frame of data;

2) Data bit parsing, the data bit lasts for 1us, the data bit is 0 at the rising edge of 0.5 us, and the data bit is 1 at the falling edge of 0.5 us;

3) Data verification, the flight control data adopts odd check, and all data bits are parsed out by bitwise difference or then inverted to parse their check digits;

4) Data caching, instantiation of RAM inside the FPGA, and storage of parsed data in RAM;

5) Packet integrity checking, which checks whether the cached data conforms to the packet structure;

6) Data sending, the data is taken out and sent in 422 format according to high and low bytes.^[5]

B. Adaptive collection of flight control bus data

Usually, the flight controller collector model used by each type of aircraft is different, and the output flight control bus protocol is different, so an adaptive acquisition method is designed to automatically identify the flight control data protocol type, and the software of the acquisition unit is automatically configured to change to realize the acquisition of multi-type flight control bus data.

1) *Analysis of flight control data.* Flight controller data analysis needs to identify two key characteristics: synchronization word and packet length, according to which the existing flight control data types can be divided into the following four categories.

(3) In this data format, when idle, the high level is high, and the signal jumps after the low level is 1.5 us, and then the high level is 1.5 us, followed by the data bits;

(4) In this data format, when idle, the high level, the signal jumps and then the low level is 1.5 us, followed by the data bits.

b) Packet length identification

the flight control data stream is sent according to the packet during transmission, and the first word of the packet is followed by the data word. The data format of each packet is consistent, and the sending cycle is fixed.

Data words are counted when they are received, and the count value is the packet length when synchronization words are detected. If the synchronization word and packet length are detected to be the same in five consecutive packets, a valid feature value is identified.

As shown in Figure 6, the flight controller data is parsed with the acquisition program 1, and when the valid synchronization word and packet length are parsed, the current parser program matches the flight control protocol, and if the valid synchronization word and packet length cannot be detected within 1 second, the next acquisition program is jumped.

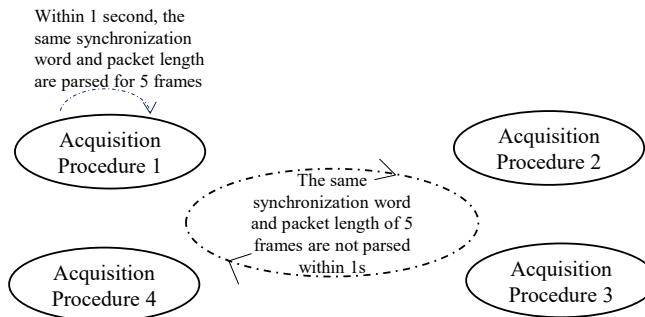


Figure 6. Jump diagram of the acquisition program.

C. Flight controller acquisition status detection

In order to facilitate the monitoring of the flight controller data acquisition status, the software is designed with signal status detection, eigenvalue detection, and packet loss detection.

1) Signal status detection

When no signal jump is detected within 1 second, the signal status indicates that there is no signal, and the signal transition time is less than 1 second, a valid signal is considered to be detected.

2) Eigenvalue detection

When a valid synchronization word and packet length are detected within 1 second, the synchronization word and packet length are cached as feature values.

3) Packet loss detection

When the packet length of the synchronization word is detected to be inconsistent with the packet length parsed by the previous packet, the current packet is considered to be an error packet and discarded, and the packet loss count value is increased by 1.

The above detection values are sent in RS422 packet format in a 1-second cycle, and the packet structure is as Table 1.

Table 1. Status package format.

3 bytes	1 byte	1 byte	1 byte	2 bytes	2 bytes	2 bytes
Sync words	Program version number	Capture program number	Signal status	Effectively synchronize words	Effective package length	Error packet count

IV. APPLICATION AND VERIFICATION:

A. Simulation debugging

The simulator is used to simulate the flight control data of the original machine, and it is sent to the FPGA processor module, and the difference between the data after signal conditioning and processor analysis, verification, encoding data filling, and other operations and the data input is compared with the simulation input data, and the feasibility of the signal acquisition and conversion scheme is verified

Use the flight controller simulator to send flight controller data, as shown in Table 2.

Table 2. Simulation data.

Sync words	Channel	Count numbers	Data 0	Data 1	...	Data n
AA55	0~3	0~65535	0	1	...	n

As shown in Figure 7, the simulation data parsed by the module is the analyzed data word, and it can be seen that the analyzed data synchronization word and subsequent data word are consistent with the flight control data.

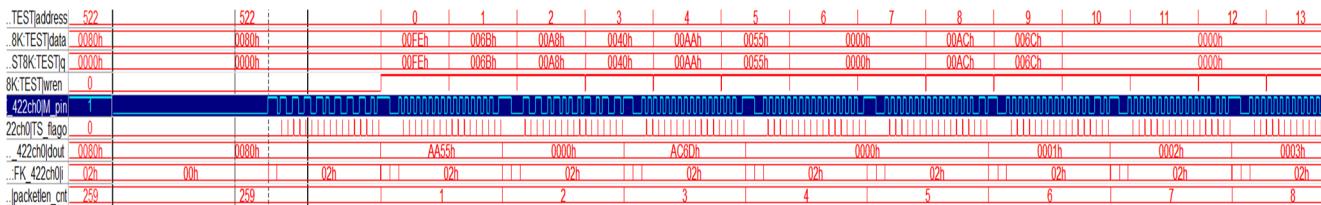


Figure 7. Real-time analysis of simulated flight controller data.

After the data cached by the module is shown in Figure 8 it can be found that the data of one frame parsed and cached is

completely consistent with the data of one frame flight controller.

Figure 8. Cached flight controller data for one frame.

According to the results of simulation debugging, the data sent by the simulation is consistent with the data collected by the FPGA, which proves that the scheme is feasible and can complete the signal conversion and acquisition functions.

B. Comparison and demonstration verification

In the laboratory, as shown in Figure 9 the simulator data collected by the FTI acquisition unit and the simulator data collected by the existing flight controller collector are demonstrated and compared, and the consistency of the two data is verified. The comparison showed that the results of the two groups were consistent, indicating that the signal conversion and acquisition scheme was feasible.

V. CONCLUSION

In this paper, the FTI signal acquisition and conversion scheme is studied, which converts the FTI flight controller data into RS422 data, which can be used by the general RS422 bus acquisition module for data acquisition, to realize the acquisition and recording of FTI data on the aircraft. The design of the acquisition scheme simplifies the structure of the test system, improves the flexibility and maintainability of the test equipment, and also provides a design idea for the integration and modularization of other test equipment in the future, which can be extended to the flight test tasks of other types of aircraft.

REFERENCES

- [1] Zhichao You. Airborne data bus technology and its application[M], National Defense Industry Press, 2009:35-41.
 - [2] Keke Su. Key technologies for embedded system development[J], Electronic Technology and Software Engineering,2018(11):212.
 - [3] Yucen Tian. FPGA chip design and its applications[J] , The world of digital communication,2019(4):228.
 - [4] Rongwei Wu. Design and implementation of high-speed data transmission scheme based on FPGA[J], Journal of Chongqing University of Posts and Telecommunications, 2010(11):104-112.
 - [5] Hongmei Shi. Implement the MAN codec in the 1553B bus interface with an FPGA [J], MCU and Embedded System Applications,2004(4):12-13



Figure 9. Schematic diagram of laboratory demonstration verification.