User Manual: 3rd Generation EPS (XUA)

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Document Control

Issue	Date	Section	Description of Change	Reason for Change
A	11/12/14	All	First Draft	N/A
B	10/02/14	4, 9.2	Update minimum operating voltage of 12W BCR	Update to reflect improved operating envelope of product following additional test.

Revision Control

Product	Part Number	Build Revision covered	Notes
3rd Generation EPS (XUA)	01-01317	A, B	

Acronyms and Abbreviations

BCR	Battery Charge Regulator
PCM	Power Conditioning Module
PDM	Power Distribution Module
MPPT	Maximum Power Point Tracker
USB	Universal Serial Bus
ESD	Electro Static Discharge
TLM	Telemetry
EPS	Electrical Power System
EoC	End of Charge
AMUX	Analogue Multiplexer
ADC	Analogue to Digital Converter
AIT	Assembly, Integration and Testing
1U	1 Unit (Cubesat standard size)
3U	3 Unit (Cubesat standard size)
FleXU/XU	FleXible Unit (suitable for various satellite configurations)
rh	Relative Humidity
Wh	Watt Hour
Ah	Ampere Hour
DoD	Depth of Discharge
$Kbits^{-1}$	Kilobits per second
Voc	Open Circuit Voltage
Isc	Short Circuit Current
2s1p	Battery configuration – 2 cells in series, 1 battery in parallel (single string)
2s2p	Battery configuration – 2 cells in series, 2 batteries in parallel
2s3p	Battery configuration – 2 cells in series, 3 batteries in parallel

Related Documents

No.	Document Name	Doc Ref.
RD-1	Battery board User Manual	TBC
RD-2	CubeSat Design Specification	CubeSat Design Specification Rev. 12
RD-3	NASA General Environmental Verification Standard	GSFC-STD-7000 April 2005
RD-4	CubeSat Kit Manual	UM-3
RD-5	Solar Panel User Document	TBC
RD-6	Power System Design and Performance on the World's Most Advanced In-Orbit Nanosatellite	As named

⚠ Warning ⚠	Risk
Ensure headers H1 and H2 are correctly aligned before mating boards	If misaligned, battery positive can short to ground, causing failure of the battery and EPS
Ensure switching configuration is implemented correctly before applying power to EPS	If power is applied with incorrect switch configuration, the output of the BCR can be blown, causing failure of the EPS
Observe ESD precautions at all times	The EPS is a static sensitive system. Failure to observe ESD precautions can result in failure of the EPS.
Ensure not to exceed the maximum stated limits	Exceeding any of the stated maximum limits can result in failure of the EPS
Ensure batteries are fully isolated during storage	If not fully isolated the battery may over-discharge, resulting in failure of the battery
No connection should be made to H2.35-36	These pins are used to connect the battery to the EPS. Any connections to the unregulated battery bus should be made to pins H2.43-44
H1 and H2 pins should not be shorted at any time	These headers have exposed live pins which should not be shorted at any time. Particular care should be taken regarding the surfaces these are placed on.

Table of Contents

1. Introduction

This document provides information on the features, operation, handling and storage of the 01-01317 EPS, designed to integrate with a suitable battery and solar arrays to form a complete power system for use on a 3U CubeSat with deployable solar panels or larger nanosatellites.

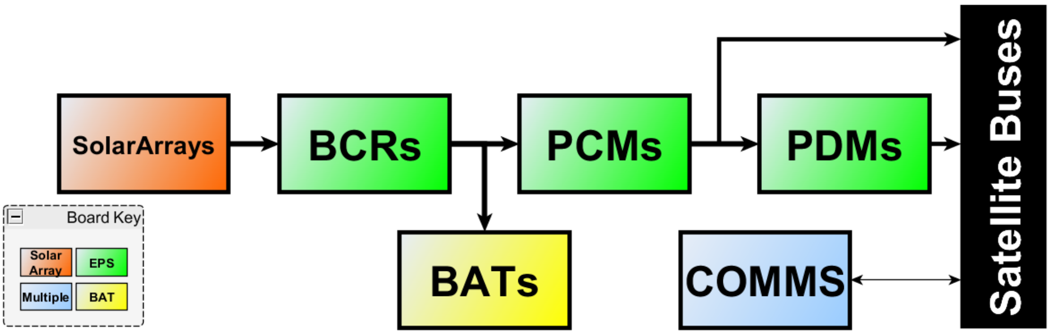

Figure 1-1 System Diagram

1.1 Additional Information Available Online

Additional information on CubeSats and Clyde Space Systems can be found at www.clyde-space.com. You will need to login to our website to access certain documents.

1.2 Continuous Improvement

At Clyde Space we are continuously improving our processes and products. We aim to provide full visibility of the changes and updates that we make, and information of these changes can be found by logging in to our website: www.clyde-space.com.

1.3 Document Revisions

In addition to hardware and software updates, we also update make regular updates to our documentation and online information.

2. Overview

This is the third generation of Clyde Space CubeSat Electronic Power System, developed by our team of highly experienced Spacecraft Power Systems and Electronics Engineers.

The EPS3G incorporates a number of additional features over and above what is included in the second generation, building on the extensive heritage we have gained along with the experience of delivering over 400 units to wide ranging customers. The main new features include:

- 10 commandable power switches
- Improved over-current protection on power buses
- Addition of a 12V regulated bus as standard
- Solid State flight switches
- Additional telemetry information
- Communications reset timeout

As a result of the new features there is a requirement to alter the interfaces to the main CubeSat Kit header. Further detail on the new features and interfaces can be found in this user manual.

Clyde Space is the World leading supplier of power system components for CubeSats. We have been designing, manufacturing, testing and supplying batteries, power system electronics and solar panels for space programmes since 2006. Our customers range from universities running student led missions, to major space companies and government organisations.

3. Maximum Ratings[1]

OVER OPERATING TEMPERATURE RANGE (UNLESS OTHERWISE STATED)				
		BCR	Value	Unit
Input Voltage[2]	SA1A &SA1B (pin 1 on each)	BCR1	25	V
	SA2A &SA2B (pin 1 on each)	BCR2	25	V
	SA3A &SA3B (pin 1 on each)	BCR3	10	V
	SA4 (pin 1 or pin5)	BCR4	25	V
	SA5 (pin 1 or pin5)	BCR5	25	V
	SA6 (pin 1 or pin5)	BCR6	25	V
	SA7 (pin 1 or pin5)	BCR7	25	V
	SA8 (pin 1 or pin5)	BCR8	25	V
	SA9 (pin 1 or pin5)	BCR9	25	V
	12V Bus		12.12	V
	Battery		8.3	V
	5V Bus		5.05	V
	3.3V Bus		3.33	V
			Value	Unit
Input Current	BCR1,2,4,5,6,7,8,9	@16V	750	mA
	BCR3	@6V	750	mA
Output Current	12V Bus	@12V	1.5	A
	Battery Bus	@8.26V	4.5	A
	5V Bus	@5V	4.5	A
	3.3V Bus	@3.3V	4.5	A
Operating Temperature			-40 to 85	°C
Storage Temperature			-50 to 100	°C
Vacuum			10^{-5}	torr
Radiation Tolerance			10kRad	kRad
Vibration			To [RD-3]	

Table 3-1 Max Ratings of the 01-01317

(1) Stresses beyond those listed under maximum ratings may cause permanent damage to the EPS. These are the stress ratings only. Operation of the EPS at conditions beyond those indicated is not recommended. Exposure to absolute maximum ratings for extended periods may affect EPS reliability

(2) De-rating of power critical components is in accordance with ECSS guidelines.

4. Electrical Characteristics

Description	Conditions	Min	Typical	Max	Unit
BCRs 1,2,4,5,6,7,8 and 9					
Input Voltage		7.4	--	25	V
Output Voltage		6.144	--	8.26	V
Output Current		0	--	2.5	A
Switching Frequency		245	250	255	KHz
Efficiency	@16.5V input, Full Load	85%	90%	92%	
BCR 3					
Input Voltage		3.5	--	8	V
Output Voltage		6.144	--	8.26	V
Output Current		0	--	0.5	A
Operating Frequency		160	170	180	KHz
Efficiency	@6V input, Full Load	77%	79%	80%	
12V Bus					
Output Voltage		11.88	--	12.12	V
Output Current		--	1.35	1.5	A
Operating Frequency		790	800	810	kHz
Efficiency	@12V input, Full Load	89%	90%	93%	
Unregulated Battery Bus					
Output Voltage		6.144	--	8.26	V
Output Current		--	4	4.5	A
Operating Frequency		--	--	--	
Efficiency	@8.26V input, Full Load	98.5%	99%	99.5%	
5V Bus					
Output Voltage		4.95	5	5.05	V
Output Current		--	4	4.5	A
Operating Frequency		470	480	490	kHz
Efficiency	@5V input, Full Load	95%	96%	98%	
3.3V Bus					
Output Voltage		3.267	3.3	3.333	V
Output Current		--	4	4.5	A
Operating Frequency		470	480	490	kHz
Efficiency	@3.3V input, Full Load	94%	95%	97%	
Communications					
Protocol		--	I^2C	--	
Transmission speed		--	100	400	$Kbits^{-1}$
Bus voltage		3.26V	3.3V	3.33V	
Node address		--	0x2B	--	Hex
Address scheme		--	7bit	--	
Node operating frequency		--	27MHz	--	
Quiescent Operation					
Power Draw	Flight Configuration of Activation Switches	--	--	<0.4	W
Physical		**L**	**W**	**H**	
Dimensions	Height from top of PCB to bottom of next PCB in stack	95	90	14.95	mm
Weight		145	148	150	g

Table 4-1 Performance Characteristics of the EPS

5. Handling and Storage

The EPS requires specific guidelines to be observed for handling, transportation and storage. These are stated below. Failure to follow these guidelines may result in damage to the units or degradation in performance.

5.1 Electro Static Discharge (ESD) Protection

The EPS incorporates static sensitive devices and care should be taken during handling. Do not touch the EPS without proper electrostatic protection in place. All handling of the system should be done in a static dissipative environment.

5.2 General Handling

The EPS is robust and designed to withstand flight conditions. However, care must be taken when handling the device. Do not drop the device as this can damage the EPS. There are live connections between the battery systems and the EPS on the CubeSat Kit headers. All metal objects (including probes) should be kept clear of these headers.

Gloves should be worn when handling all flight hardware.

Flight hardware, which will be delivered conformally coated, should only be removed from packaging in a class 100000 (or better) clean room environment.

5.3 Shipping and Storage

The devices are shipped in anti-static packaging, enclosed in a hard protective case. This case should be used for storage. All hardware should be stored in anti-static containers at temperatures between 20°C and 40°C and in a humidity-controlled environment of 40-60%rh.

The shelf-life of this product is estimated at 5 years when stored appropriately.

6. Materials and Processes

6.1 Materials Used

	Material	Manufacturer	%TML	%CVCM	%WVR	Application
1.	Araldite 2014 Epoxy	Huntsman	0.97	0.05	0.33	Adhesive fixing
2.	1B31 Acrylic	Humiseal	3.89	0.11	0.09	Conformal Coating
3.	DC 6-1104	Dow Corning	0.17	0.02	0.06	Adhesive fixing on modifications
4.	PCB material	FR4	0.62	0	0.1	Note: worst case on NASA out-gassing list
5.	Solder Resist	CARAPACE EMP110 or XV501T-4	0.95 or 0.995	0.02 Or 0.001	0.31	-
6.	Solder	Sn62 or Sn63 (Tin/Lead)	-	-	-	-
7.	Flux	Alpha Rosin Flux, RF800, ROL 0	-	-	-	Low activity flux to avoid corrosion
8.	300 Series Stainless Steel	Pemnet	-	-	-	PEMs
9.	A4 Stainless Steel (316L)	PTS-UK	-	-	-	M3 Fasteners

Table 6-1 Materials List

Part Used	Manufacturer	Contact	Insulator	Type	Use	Required mating Connector
DF13-8P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Solar Array Connectors (Daughter Board)	DF13-8s-1.25C and DF13-2630SCFA(04)
DF13-6P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Programming Header – not for customer use	DF13-6S-1.25C and DF13-2630SCFA(04)
DF13-5P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Solar Array Connectors	DF13-5S-1.25C and DF13-2630SCFA(04)
DF13-3P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Remove Before Flight Switch Connectors	DF13-3S-1.25C and DF13-2630SCFA(04)
DF13-2P-1.25DSA(50)	Hirose	Gold Plated	Polyamide	PTH	Separation Switch Connectors	DF13-2S-1.25C and DF13-2630SCFA(04)
SFM-110-02-L-D-A	Samtec	Gold Plated Beryllium Copper	Black Liquid Crystal Polymer	SMT	Expansion Header for daughterboard connection	TFM-110-22-L-D-A
TFM-110-22-L-D-A	Samtec	Gold Plated Beryllium Copper	Black Liquid Crystal Polymer	SMT	Daughterboard to motherboard connection header	SFM-110-02-L-D-A
ESQ-126-39-G-D	Samtec	Gold Plated	Black Glass Filled Polyester	PTH	CubeSat Kit Compatible Headers	ESQ-126 range

Table 6-2 Connector Headers

6.2 Processes and Procedures

All assembly is inspected to ESA Workmanship Standards; ECSS-Q-ST-70-08C and ECSS-Q-ST-70-38C.

7. System Description

The Clyde Space EPS is optimised for Low Earth Orbit (LEO). The EPS is designed for integration with a nanosatellite. The EPS can accommodate various solar panel configurations, and has been designed to be versatile; please consult our support team if you have specific requirements for connecting the EPS to your spacecraft.

The Clyde Space EPS connects to the solar panels via nine independent Battery Charge Regulators (BCRs). These are connected with panels on opposing faces of the satellite connected to the same BCR (e.g. –X array and +X array are connected to BCR1, -Y and +Y to BCR2 and –Z and +Z to BCR3). In this configuration only one panel per pair can be directly illuminated at any given time, with the second panel providing a limited amount of energy due to albedo illumination. Each of the BCRs has an inbuilt Maximum Power Point Tracker (MPPT). This MPPT will track the dominant panel of the connected pair (the directly illuminated panel).

The output of the nine BCRs are then connected together and, via the switch network, (described in Section 8.7), supply charge to the battery, Power Conditioning Modules (PCMs) and Power Distribution Modules (PDMs).

The PCM network has an unregulated Battery Voltage Bus, a regulated 5V supply, a regulated 3.3V supply and a regulated 12V supply. In addition to the main buses there are 10 commandable power switches – 2x12V, 2xBATV, 3x5V and 3x3.3V. The EPS also has multiple inbuilt protection methods to ensure safe operation during the mission and a full range of EPS telemetry via the I^2C network. These are discussed in detail in Sections 10 and 11.

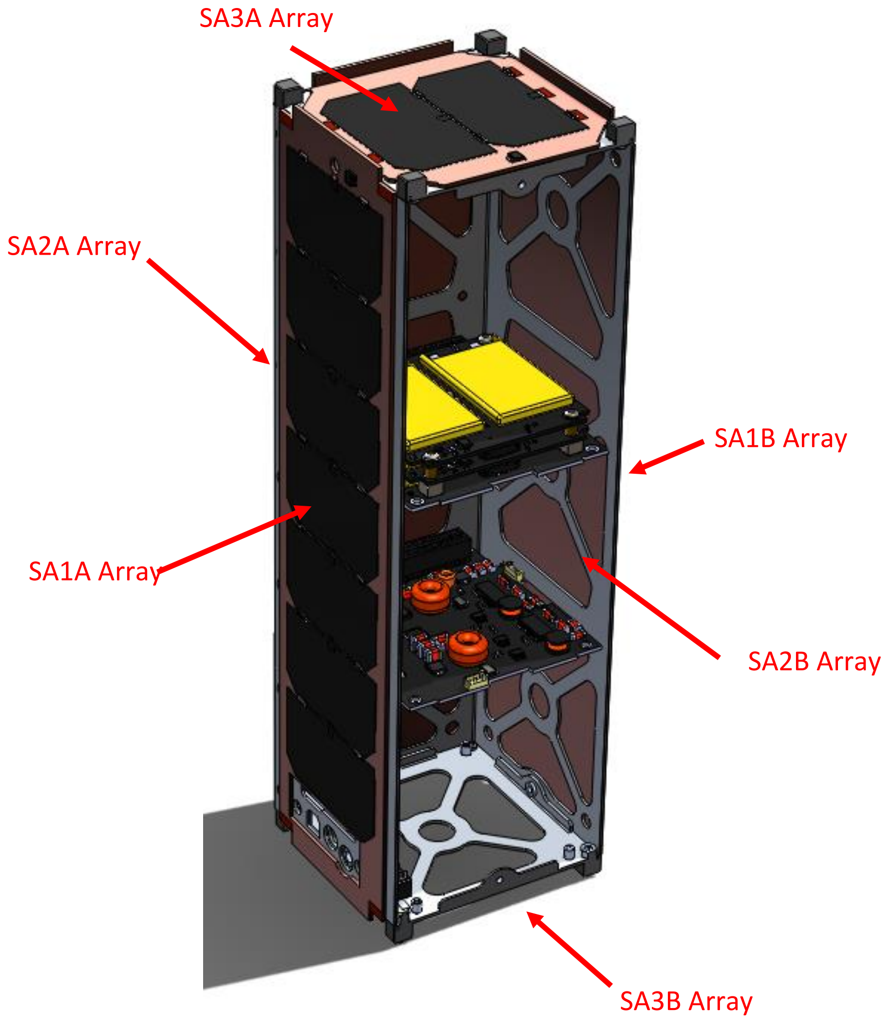

Figure 7-1 Array Configuration with Example Allocations **(additional deployed panels can interface to BCRs 4-9)**

7.1 System Overview

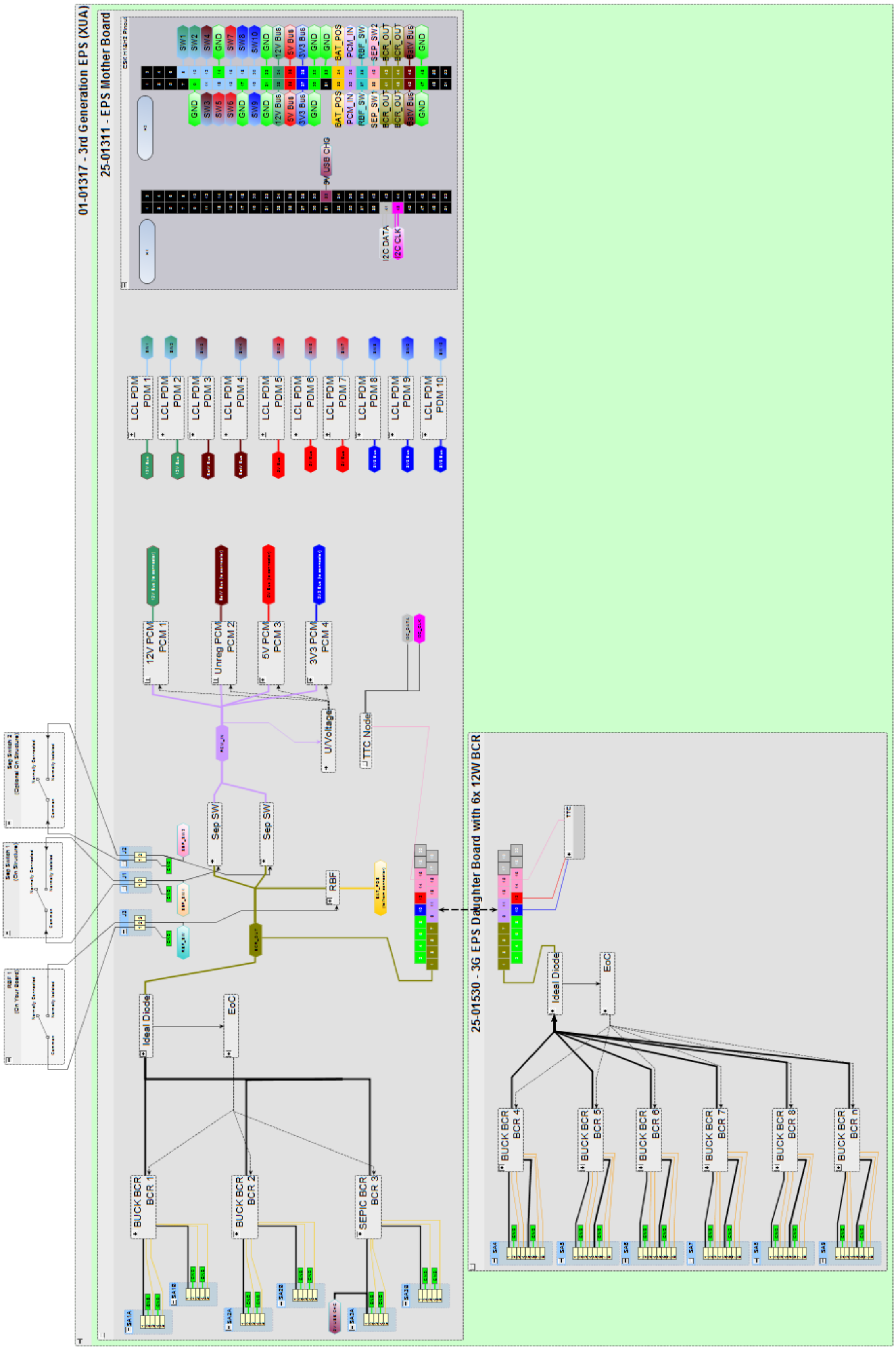

Figure 7-2 Function Diagram

7.2 Autonomy and Redundancy

All BCR power stages feature full system autonomy, operating solely from the solar array input and not requiring any power from the battery systems. This feature offers graceful degradation of the system as none of the BCRs depend on any other circuitry to operate correctly. Failure of all strings of the battery (any of the Clyde Space Battery range) will not damage the BCRs but, due to the MPPT, will result in an intermittent interruption on all power buses (approximately every 2.5 seconds). Failure of one battery on the CS-SBAT-20 or two batteries on the CS-SBAT2-30 will not damage the BCRs and the system can continue to operate with a reduced capacity of 10Wh.

The rest of the power system is a robustly designed single string.

7.3 Quiescent Power Consumption

All power system efficiencies detailed (for BCRs and PCMs) takes into consideration the associated low level control electronics. As such, these numbers are not included in the quiescent power consumption figures.

The quiescent current draw covers the power required to run the TTC node, PDMs and other monitoring and safety features of the EPS, totalling ≈0.39W.

7.4 Mass and Mechanical Configuration

The mass of the system is approximately 148g and is contained on one PC/104 size card with a mounted daughterboard, compatible with the Cubesat Kit bus. Other versions of the EPS are available without the Cubesat Kit bus header.

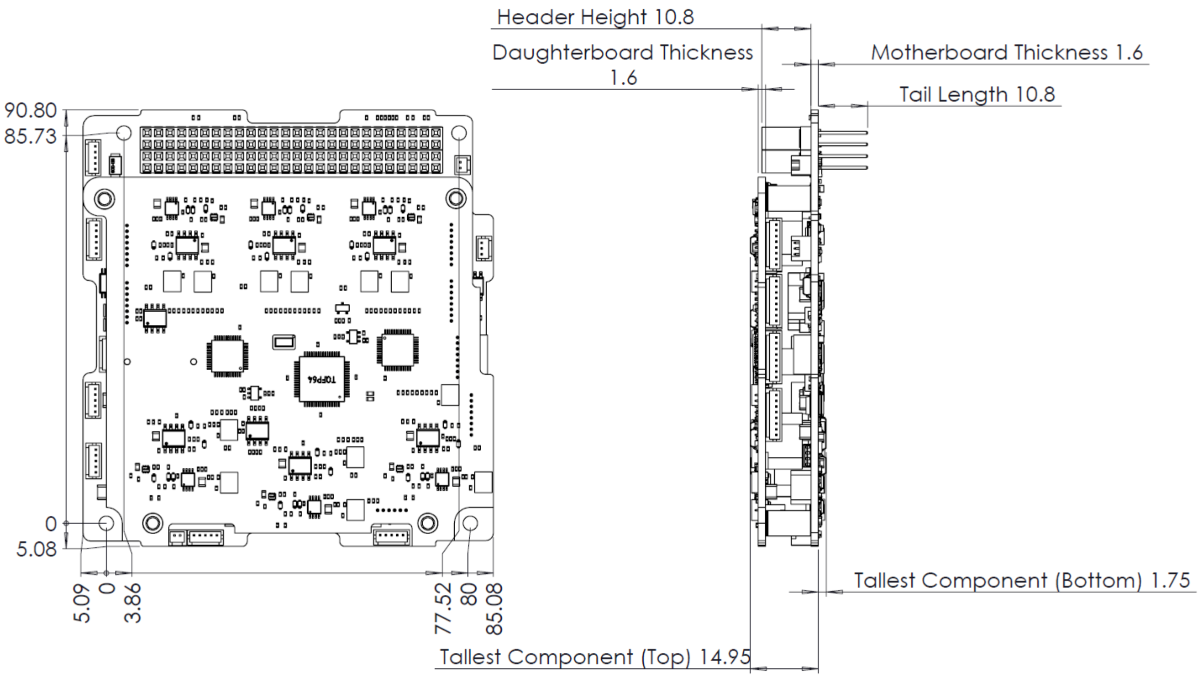

Figure 7-3 Mechanical Diagram

8. Interfacing

The connector interfaces of the EPS are outlined in Figure 8-1, including the solar array inputs, connection to the switch configuration, output of the power buses and communication to the I^2C node. In the following section it is assumed that the EPS will be integrated with a Clyde Space Battery.

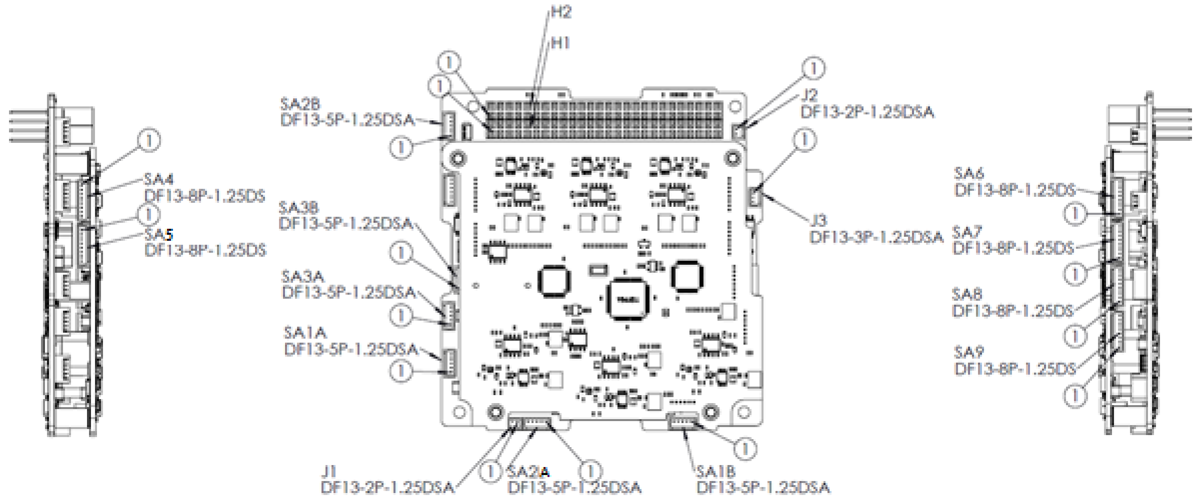

Figure 8-1 Clyde Space EPS and Battery Simplified Connection Diagram (connectors not marked are for CS use only)

The connector positions are described in Table 8-1.

Connector	Function
SA1A	Solar Array connector A for channel A of BCR1
SA1B	Solar Array connector B for channel B of BCR1
SA2A	Solar Array connector A for channel A of BCR2
SA2B	Solar Array connector B for channel B of BCR2
SA3A	Solar Array connector A for channel A of BCR3
SA3B	Solar Array connector B for channel B of BCR3
SA4	Solar Array connector for channels A&B of BCR4
SA5	Solar Array connector for channels A&B of BCR5
SA6	Solar Array connector for channels A&B of BCR6
SA7	Solar Array connector for channels A&B of BCR7
SA8	Solar Array connector for channels A&B of BCR8
SA9	Solar Array connector for channels A&B of BCR9
J1	Separation Switch 1 Connection
J2	Separation Switch 2 Connection
J3	Remove Before Flight Switch Connection
H1	CubeSat Kit bus compatible Header 1
H2	CubeSat Kit bus compatible Header 2

Table 8-1 Connector functions

8.1 Solar Array Connection

The EPS Motherboard has six connectors for the attachment of solar arrays. This interface accommodates inputs from the arrays with temperature and sun detector telemetry for each.

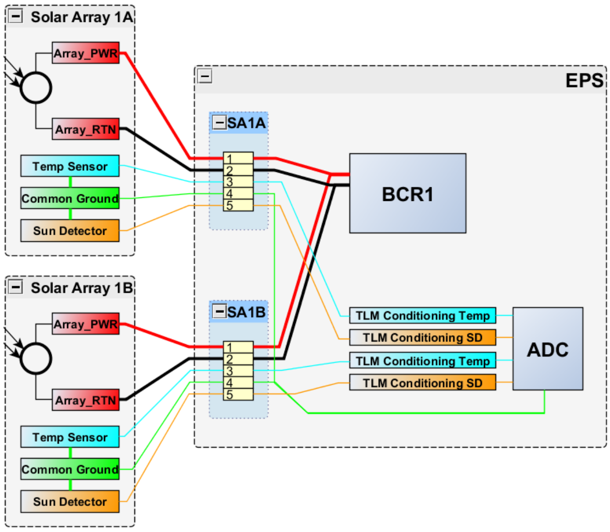

Figure 8-2 Example Solar Array Configuration SA1A and SA1B

HIROSE DP13-5P-1.25DSA(50) connector sockets are used on the EPS motherboard. These are labelled SA1A1-SA3B1. SA1A1-SA2B1 are routed to BCR1-BCR2 respectively. These BCRs are capable of interfacing to panels with between 4-8 triple junction solar cells in series. **Any arrays connected in parallel should have the same number of cells.**

SA3 routes to BCR3 and should be harnessed to the small arrays. The array lengths should be the same on joined panels, with 2-3 cells each.

The EPS Daughterboard has six connectors for the attachment of solar arrays. This interface accommodates inputs from the arrays with temperature and sun detector telemetry for each.

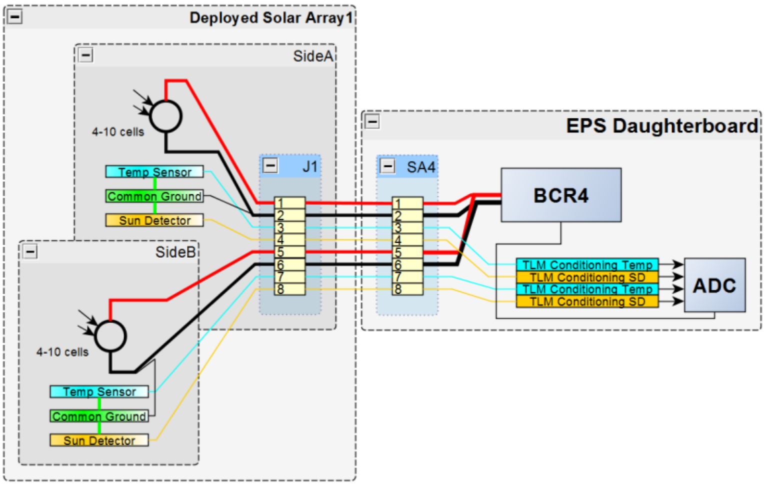

Figure 8-3 Example Solar Array Configuration SA4

HIROSE DP13-8P-1.25DSA(50) connector sockets are used on the EPS daughterboard. These are labelled SA4-SA9 and routed to BCR4-BCR9 respectively. These BCRs are capable of interfacing to panels with between 4-8 triple junction solar cells in series. **Any arrays connected in parallel should have the same number of cells.**

Pin	Name	Use	Notes
1	1_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	1_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	1_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-2 Pin out for Header SA1A

Pin	Name	Use	Notes
1	1_B ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	1_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	1_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-3 Pin out for Header SA1B

Pin	Name	Use	Notes
1	2_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	2_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	2_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-4 Pin out for Header SA2A

Pin	Name	Use	Notes
1	2_B ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	2_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	2_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-5 Pin out for Header SA2B

Pin	Name	Use	Notes
1	3_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	3_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	3_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-6 Pin out for Header SA3A

Pin	Name	Use	Notes
1	3_B ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	3_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	GND	Ground Line	Power RTN and GND connection for Temp Sensor
5	3_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-7 Pin out for Header SA3B

Pin	Name	Use	Notes
1	4_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	4_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	4_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	4_B ARRAY	Power Line	Power
6	GND	Ground Line	Power RTN and GND connection for Temp Sensor
7	4_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	4_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-8 Pin out for Header SA4

Pin	Name	Use	Notes
1	5_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	5_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	5_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	5_B ARRAY	Power Line	Power

6	GND	Ground Line	Power RTN and GND connection for Temp Sensor
7	5_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	5_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-9 Pin out for Header SA5

Pin	Name	Use	Notes
1	6_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	6_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	6_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	6_B ARRAY	Power Line	Power
6	GND	Ground Line	Power RTN and GND connection for Temp Sensor
7	6_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	6_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-10 Pin out for Header SA6

Pin	Name	Use	Notes
1	7_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	7_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	7_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	7_B ARRAY	Power Line	Power
6	GND	Ground Line	Power RTN and GND connection for Temp Sensor
7	7_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	7_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-11 Pin out for Header SA7

Pin	Name	Use	Notes
1	8_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	8_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	8_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	8_B ARRAY	Power Line	Power
6	GND	Ground Line	Power RTN and GND connection for Temp Sensor

7	8_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	8_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-12 Pin out for Header SA8

Pin	Name	Use	Notes
1	9_A ARRAY	Power Line	Power
2	GND	Ground Line	Power RTN and GND connection for Temp Sensor
3	9_A ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
4	9_A ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry
5	9_B ARRAY	Power Line	Power
6	GND	Ground Line	Power RTN and GND connection for Temp Sensor
7	9_B ARRAY_TEMP_TELEM	Temperature Telemetry	Telemetry
8	9_B ARRAY_SUN_TELEM	Sun Detector Telemetry	Telemetry

Table 8-13 Pin out for Header SA9

8.2 Solar Array Harness

Clyde Space supply harnesses (sold separately) to connect the solar panels to the EPS Motherboard, comprising one Hirose DF13-5S-1.25C connected at the panel and one connector at the other connected at the EPS. Similarly, harnesses to connect the solar panels to the EPS Daughterboard, comprise of one Hirose DF13-8S-1.25C connected at the panel and one connector at the other connected at the EPS.

8.3 Temperature Sensing Interface

Temperature sensing telemetry is provided for each solar array connected to the EPS. A compatible temperature sensor (LM335AM) is fitted as standard on Clyde Space solar arrays (for non-Clyde Space panels refer to Section 8.4). The output from the LM335AM sensor is then passed to the telemetry system via on board signal conditioning. Due to the nature of the signal conditioning, the system is only compatible with zener based temperature sensors i.e. LM335AM or equivalent. Thermistor or thermocouple type sensors are incompatible with the conditioning circuit.

The conditioning circuit shown in Figure 8-2 is biased by 5V. There is also a voltage divider to ensure the voltage output of the temperature sensor (V_{TEMP}) is conditioned to an acceptable voltage for the ADC circuit.

$$V_{ADC} = 0.787 \times V_{TEMP}$$

In the case of the LM335AM the output voltage varies with temperature as follows:

$$V_{TEMP} = 0.01 \times (TEMP(°C) - 273.15)$$

Hence the Voltage at the input of the ADC is:

$$V_{ADC} = 0.787 \times 0.01 \times (TEMP(°C) - 273.15)$$

As the ADC is a 10bit converter, referenced to 3V, the ADC counts can be calculated as follows:

$$V_{ADC} = \frac{3}{1023} \times Count_{ADC}$$

Combining the two equations for V_{ADC} above we get:

$$0.787 \times 0.01 \times (TEMP(°C) + 273.15) = \frac{3}{1023} \times Count_{ADC}$$

$$\boldsymbol{TEMP}(°C) = \mathbf{0.3724} \times \boldsymbol{Count_{ADC}} - \mathbf{273.15}$$

8.4 Non-Clyde Space Solar Arrays

When connecting non-Clyde Space solar arrays care must be taken with the polarity. Cells used should be of triple junction type. If other cells are to be interfaced please contact Clyde Space.

8.5 CubeSat Kit Compatible Headers

Connections from the EPS to the bus of the satellite are made via the CubeSat Kit compatible headers H1 and H2, as shown in Figure 8-4.

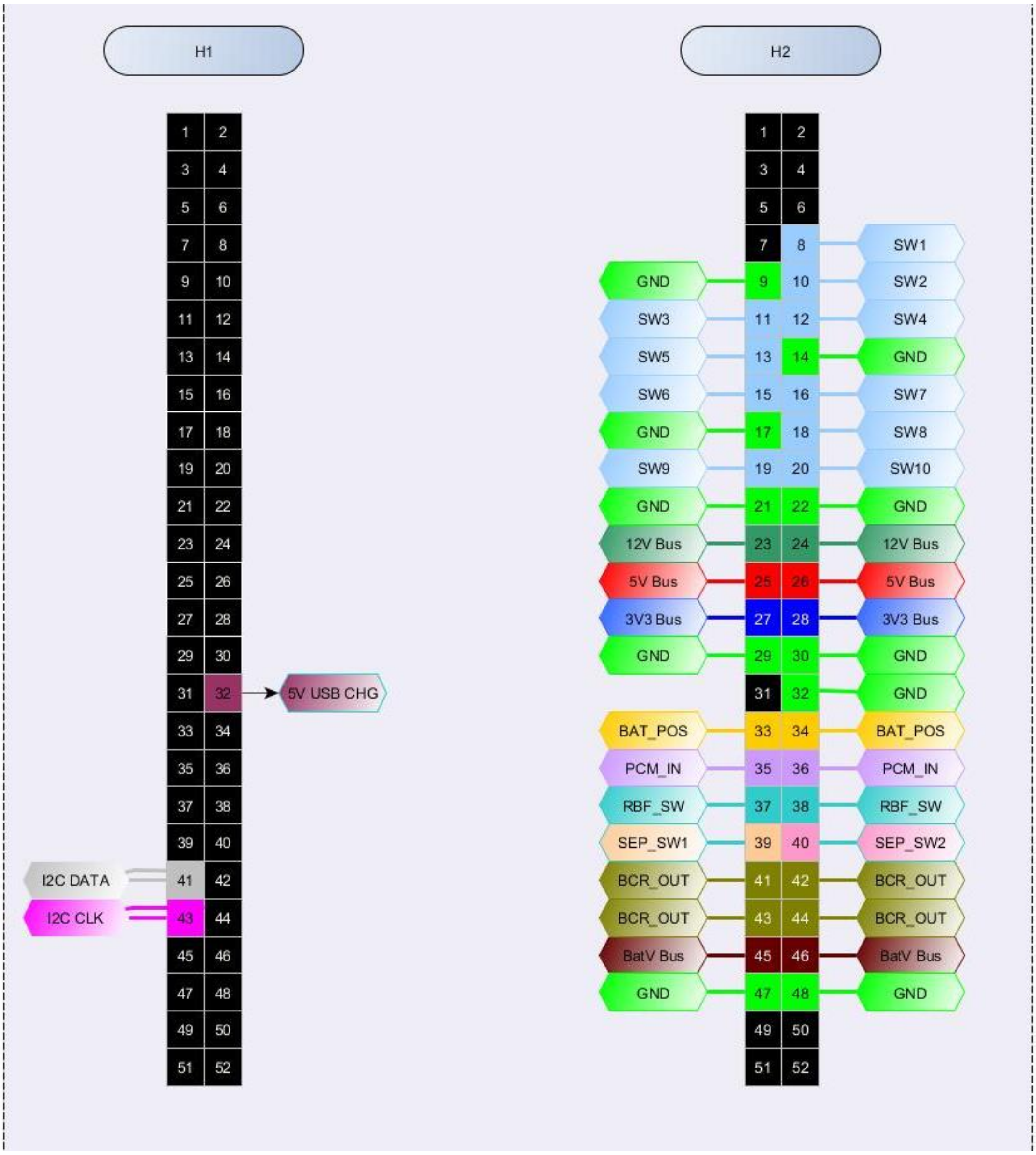

Figure 8-4 CubeSat Kit Header Schematic

8.6 Cubesat Kit Header Pin Out

HEADER 1				HEADER 2			
Pin	Name	Use	Notes	Pin	Name	Use	Notes
1	NC	-	-	1	NC	-	-
2	NC	-	-	2	NC	-	-
3	NC	-	-	3	NC	-	-
4	NC	-	-	4	NC	-	-
5	NC	-	-	5	NC	-	-
6	NC	-	-	6	NC	-	-
7	NC	-	-	7	NC	-	-
8	NC	-	-	8	SW1	Switch 1 Output	12V Switch
9	NC	-	-	9	GND	Ground	System Ground
10	NC	-	-	10	SW2	Switch 2 Output	12V Switch
11	NC	-	-	11	SW3	Switch 3 Output	BAT Switch
12	NC	-	-	12	SW4	Switch 4 Output	BAT Switch
13	NC	-	-	13	SW5	Switch 5 Output	5V Switch
14	NC	-	-	14	GND	Ground	System Ground
15	NC	-	-	15	SW6	Switch 6 Output	5V Switch
16	NC	-	-	16	SW7	Switch 7 Output	5V Switch
17	NC	-	-	17	GND	Ground	System Ground
18	NC	-	-	18	SW8	Switch 8 Output	3V3 Switch
19	NC	-	-	19	SW9	Switch 9 Output	3V3 Switch
20	NC	-	-	20	SW10	Switch 10 Output	3V3 Switch
21	NC	-	-	21	GND	Ground	System Ground
22	NC	-	-	22	GND	Ground	System Ground
23	NC	-	-	23	12VBUS	12V Bus	Power Bus
24	NC	-	-	24	12VBUS	12V Bus	Power Bus
25	NC	-	-	25	5VBUS	5V Bus	Power Bus
26	NC	-	-	26	5VBUS	5V Bus	Power Bus
27	NC	-	-	27	3V3BUS	3.3V Bus	Power Bus
28	NC	-	-	28	3V3BUS	3.3V Bus	Power Bus
29	NC	-	-	29	GND	Ground	System Ground
30	NC	-	-	30	GND	Ground	System Ground
31	NC	-	-	31	NC	-	-
32	5VUSB_CHG	5V USB Charge	Battery Top up Charge	32	GND	Ground	System Ground
33	NC	-	-	33	BAT_POS	Battery Positive	Direct Connection
34	NC	-	-	34	BAT_POS	Battery Positive	Direct Connection
35	NC	-	-	35	PCM_IN	PCM Input	Reserved
36	NC	-	-	36	PCM_IN	PCM Input	Reserved
37	NC	-	-	37	RBF_SW	Remove Before Flight Switch	Short to GND = Battery Disconnected
38	NC	-	-	38	RBF_SW	Remove Before Flight Switch	Redundant Connection
39	NC	-	-	39	SEP_SW1	Separation Switch1	Short to GND = PCMs Disconnected
40	NC	-	-	40	SEP_SW2	Separation Switch2	Short to GND = PCMs Disconnected
41	I2C_DATA	I2C Data	-	41	BCR_OUT	BCR Output	Reserved
42	NC	-	-	42	BCR_OUT	BCR Output	Reserved
43	I2C_CLK	I2C Clock	-	43	BCR_OUT	BCR Output	Reserved
44	NC	-	-	44	BCR_OUT	BCR Output	Reserved
45	NC	-	-	45	BatVBUS	Unregulated Battery Bus	Power Bus
46	NC	-	-	46	BatVBUS	Unregulated Battery Bus	Power Bus
47	NC	-	-	47	GND	Ground	System Ground
48	NC	-	-	48	GND	Ground	System Ground
49	NC	-	-	49	NC	-	-
50	NC	-	-	50	NC	-	-
51	NC	-	-	51	NC	-	-
52	NC	-	-	52	NC	-	-

Table 8-14 Pin Descriptions for Header H1 and H2

8.7 Flight Switches

The Flight Switches provide a method of isolation of the BCRs and battery from the satellite power buses during storage, transportation and launch.

There are two standard types of flight switches used on CubeSat missions: remove before flight switches and separation switches.

All switches are implemented using solid state switch designs. This means that only a signal current is passed through the physical switches, so high power rated physical switches are not required and magnetic loops are minimised.

Activation Sequence

The activation sequence of the separations switches is as follows:

- Remove RBF Connection
- Remove Separation Switch connection on either J1 or J2

Table 8-15 shows the truth table for operation of the flight switches, assuming power is available on Battery Voltage.

Pin	RBF Connection	SepSwitch Connection1	SepSwitch Connection2	Bat POS	BCR OUT	PCM IN
1	Short	Short	Short	Battery Voltage	0V	0V
2	Short	Short	Open	Battery Voltage	0V	0V
3	Short	Open	Short	Battery Voltage	0V	0V
4	Short	Open	Open	Battery Voltage	0V	0V
5	Open	Short	Short	Battery Voltage	Battery Voltage	0V
6	Open	Open	Short	Battery Voltage	Battery Voltage	Battery Voltage
7	Open	Short	Open	Battery Voltage	Battery Voltage	Battery Voltage
8	Open	Open	Open	Battery Voltage	Battery Voltage	Battery Voltage

Table 8-15 Flight Switch Configuration Truth Table

Remove Before Flight Switch

The Remove Before Flight Switch allows a physical interface to isolate the battery from the Buses during ground testing, storage transportation and integration.

On the EPS there are two methods of interfacing to the RBF switch.

- via the dedicated RBF Connector J3
- the second is via the CubeSat Kit header H2, pins 37-38 and any ground pins.

In both instances shorting the connections together will isolate the battery from the circuit. Removal of this connection will connect the battery to the system.

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Glasgow G20 0SP, UK

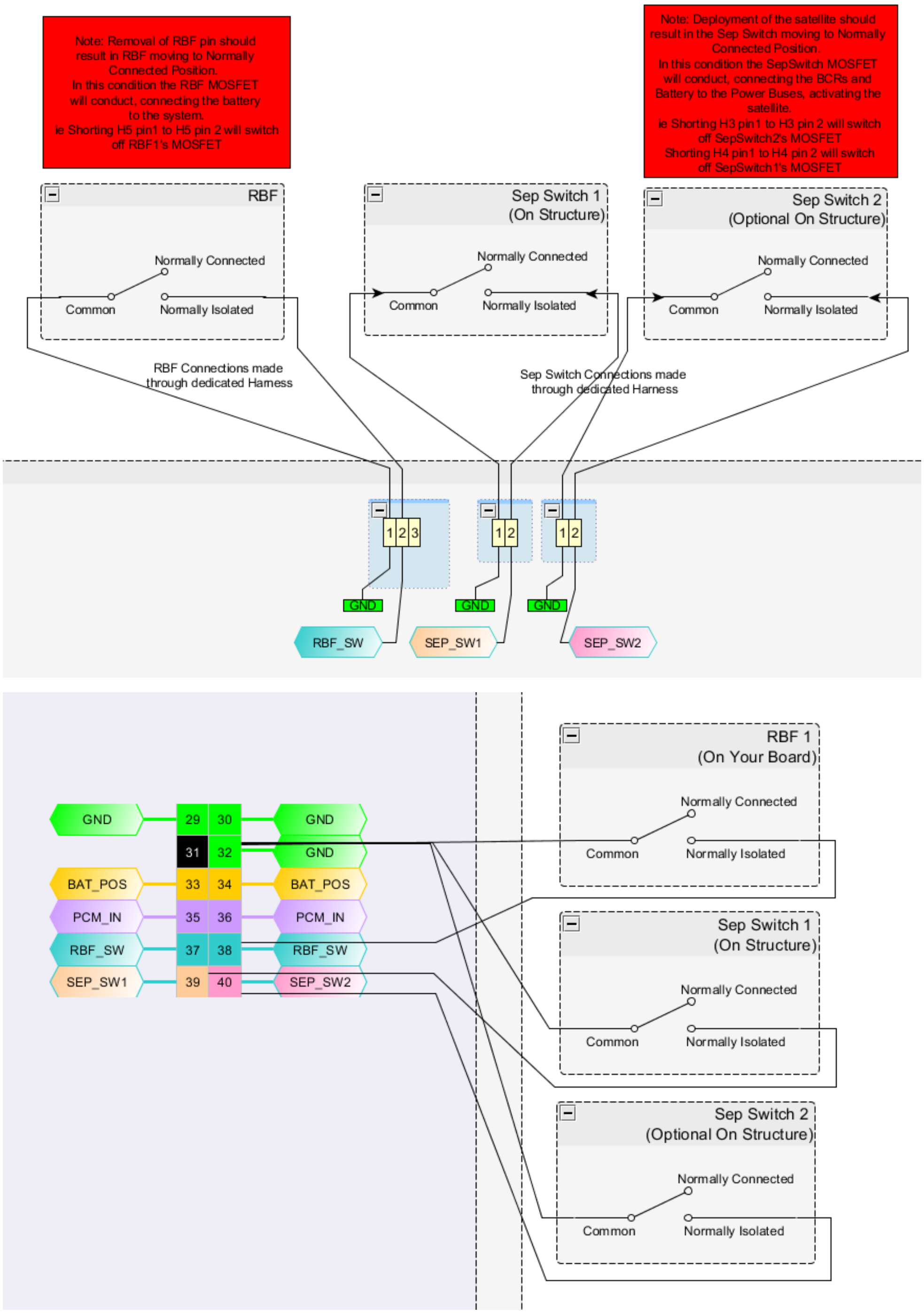

Figure 8-5 Remove Before Flight and Separation Switch Flight Switch Configuration (using example GND pins)

Pin	Name	Use	Notes
1	GND	Ground Line	RTN reference for switch connection
2	RBF_SW	Remove Before Flight Switch	Signal connection to physical remove before flight switch
3	NC	N/A	N/A

Table 8-16 Pin out for Header J3

Separation Switch

As standard the board is configured for one separation switch. In this case either J1 or J2 can be used for separation switch connection. If two separation switches are to be used please contact Clyde Space.

The Separation Switch isolates the BCRs and battery from the Satellite power buses effectively switching the satellite off. Normally a structure will have one or two foot-switches. When in the launch vehicle the switch will be compressed and the satellite will remain off - usually a requirement of the launch provider. When the satellite is deployed the Separation Switch is depressed and the BCRs and battery are connected to the satellite buses and operations commence. The EPS has two separation circuits - one for each possible physical switch. These switches are set up to have an "OR" configuration - only one switch need activate for the satellite to become operational.

There are two methods of interfacing to the Separation switches. The first is via the dedicated SepSw Connectors and the second is via the CubeSat Kit header H2, pins 39 for SepSw1 and H2 pin 40 for SepSw2 and the Ground pins on H2 pins 29,30,32. In both instances shorting the connections together (SepSw connector pins together, H2.40 to H2.29,30,32 or H2.41 to H2.29,30,32) will isolate the BCR and battery from the system. Removal of these connections will connect the BCR and battery to the system.

Pin	Name	Use	Notes
1	GND	Ground Line	RTN reference for switch connection
2	SEP_SW1	Separation Switch 1	Signal connection to physical separation switch 1

Table 8-17 Pin out for Header J1

Pin	Name	Use	Notes
1	GND	Ground Line	RTN reference for switch connection
2	SEP_SW2	Separation Switch 2	Signal connection to physical separation switch 2

Table 8-18 Pin out for Header J2

8.8 Battery connection

Connection of the battery systems on the 3U EPS is via the CubeSat kit bus. Ensure that the pins are aligned, and located in the correct position, as any offset can cause the battery to be shorted to ground, leading to catastrophic failure of the battery and damage to the EPS. **Failure to observe these precautions will result in the voiding of any warranty.**

When a battery board is connected to the CubeSat Kit header, there are live, unprotected battery pins accessible (H2.33-34). These pins should not be routed to any connections other than the Clyde Space EPS, otherwise all protections will be bypassed and significant battery damage can be sustained.

9. Technical Description

This section gives a complete overview of the operational modes of the EPS. It is assumed that a complete Clyde Space system (EPS, Batteries and Solar panels) is in operation for the following sections.

9.1 Charge Method

The BCR charging system has two modes of operation: Maximum Power Point Tracking (MPPT) mode and End of Charge (EoC) mode. These modes are governed by the state of charge of the battery.

MPPT Mode

If the battery voltage is below the preset EoC voltage the system is in MPPT mode. This is based on constant current charge method, operating at the maximum power point of the solar panel for maximum power transfer.

EoC Mode

Once the EoC voltage has been reached, the BCR changes to EoC mode, which is a constant voltage charging regime. The EoC voltage is held constant and a tapering current from the panels is supplied to top up the battery until at full capacity. In EoC mode the MPPT circuitry moves the solar array operation point away from the maximum power point of the array, drawing only the required power from the panels. The excess power is left on the arrays as heat, which is transferred to the structure via the array's thermal dissipation methods incorporated in Clyde Space panels.

The operation of these two modes can be seen in Figure 9-1

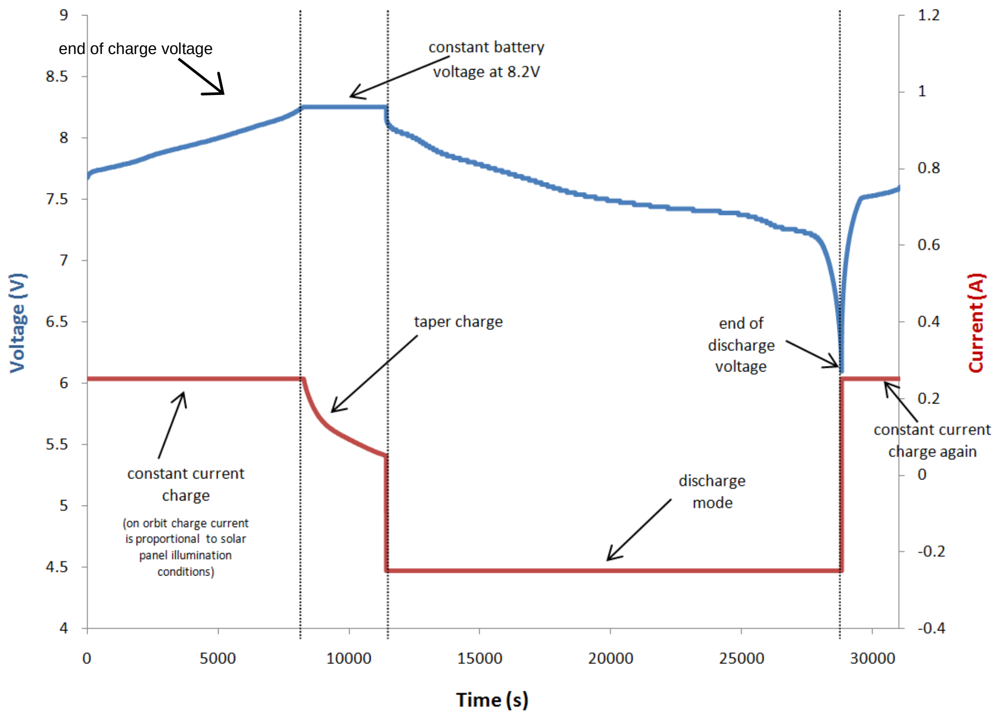

Figure 9-1 Tapered charging method

The application of constant current/constant voltage charge method on a spacecraft is described in more detail in RD-6. In this document there is on-orbit data showing the operation and how the current fluctuates with changing illumination conditions and orientation of the spacecraft with respect to the Sun.

9.2 BCR Power Stage Overview

The EPS has nine separate, independent BCRs, each designed to interface to two parallel solar arrays on opposing faces of the satellite. BCRs 1,2, 4, 5, 6, 7, 8 and 9 interface to the panels in the X and Y axes, and a third, smaller BCR (3) interfaces to the panel on the Z axis.

Each design offers a highly reliable system that can deliver 90% (1,2, 4, 5, 6, 7, 8 and 9) or 80% (3) of the power delivered from the solar array network at full load.

BCRs 1,2,4,5,6,7,8 and 9 power stage

These BCRs are BUCK converters, allowing the BCR to interface to strings of four to eight cells in series. This will deliver up to 90% output power at full load. The design will operate at peak efficiency with input voltages between 10V and 24V (can operate down to 7.4V) and a maximum output of 8.26V (7.7V nominal).

3W BCR Power Stage Design

BCR3 uses a SEPIC converter, interfacing to solar arrays of two triple junction cells in series. This will deliver up to 80% output power at full load. The BCR will operate with an input of between 3V and 6V and a maximum output of 8.26V (7.4V nominal).

9.3 MPPT

Each of the BCRs can have two solar arrays connected at any given time; only one array can be illuminated by sunlight, although the other may receive illumination by albedo reflection from earth. The dominant array is in sunlight and this will operate the MPPT for that BCR string. The MPPT monitors the power supplied from the solar array. This data is used to calculate the maximum power point of the array. The system tracks this point by periodically adjusting the BCRs to maintain the maximum power derived from the arrays. This technique ensures that the solar arrays can deliver much greater usable power, increasing the overall system performance.

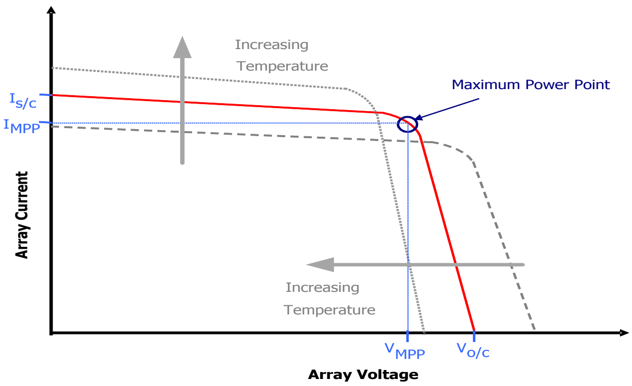

Figure 9-2 Solar Array Maximum Power Point

The monitoring of the MPP is done approximately every 2.5 seconds. During this tracking, the input of the array will step to o/c voltage, as shown in Figure 9-3.

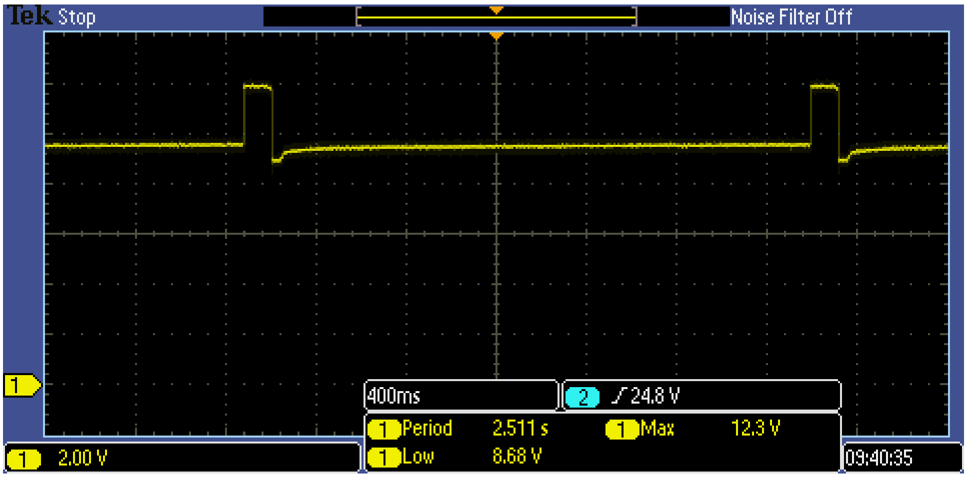

Figure 9-3 Input waveform with Maximum Power Point Tracking

9.4 5V and 3.3V PCMs with Latching Current Limiter

The 5V and 3.3V regulators both use buck switching topology regulators as their main converter stage. The regulator incorporates intelligent feedback systems to ensure the voltage regulation is maintained to +/- 1% deviation. The efficiency of each unit at full load is approximately 96% for the 5V PCM and 95% for the 3.3V PCM. Full load on each of the regulators has a nominal output current of 4.5A. Each regulator operates at a frequency of 480 kHz. The Latching Current Limiter is described in Section 9.7. If an over-current event triggers the Latching Current Limiter a retry circuit will attempt to re-enable the bus as described in section 10.1.

9.5 12V PCM with Latching Current Limiter

The 12V regulator uses a boost switching topology regulator as the main converter stage. The regulator incorporates intelligent feedback systems to ensure the voltage regulation is maintained to +/- 1% deviation. The efficiency at full load is approximately 94%. Full load on each of the regulator have a nominal output current of 1.5A. The regulator operates at a frequency of 800 kHz. The Latching Current Limiter is described in Section 9.7. If an over-current event triggers the Latching Current Limiter a retry circuit will attempt to re-enable the bus as described in section 10.1.

9.6 BatV PCM with Latching Current Limiter

The unregulated BatteryV regulator provides safe access to the battery bus of the satellite. The voltage supplied will vary directly with the battery voltage (between 6.144V and 8.26V). The Latching Current Limiter is described in Section 9.7. If an over-current event triggers the Latching Current Limiter a retry circuit will attempt to re-enable the bus as described in section 10.1.

9.7 PDMs with Latching Current Limiter

Ten independently commandable power switches have been included within the current form factor. Each switch has inbuilt overcurrent protection in the form of a latching current limiter (LCL). By utilising an LCL each switch is capable of driving loads with large inrush currents without compromising safety throughout the duration of the mission (this is of particular interest for applications such as transceivers). Once the LCL has activated, turning off the supply of power, the switch will remain off until commanded to switch on again. The switches cover the range of regulated and unregulated voltages provided by the EPS.

LCL Operation Description

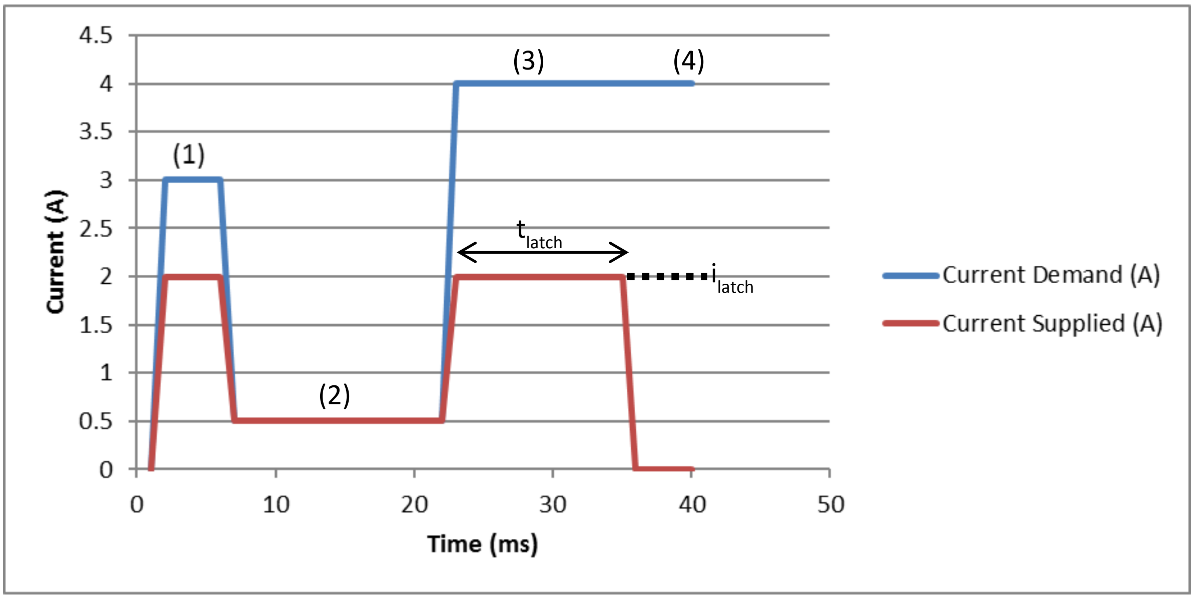

Figure 9-4 Latching Current Limiter Example Operation

In the example system shown above the events are as follows:

1. The payload demands a 3A initial current, however the switch limits the current to 2A. The time this demand is present is less than the latch time of the switch (t_{latch}), so the switch does not switch off.
2. The payload demand drops to 0.5A. This is below the current limit of the switch (i_{latch}).
3. A fault condition occurs resulting in a demand of 4A. The switch only allows 2A to pass, preventing high current damage to the switch or the payload.
4. The fault remains for longer than t_{latch} so the switch turns off preventing any current flow.

Switch characteristics:

- i_{latch}: The latching current limit is set to allow the maximum safe current the EPS can deliver. This value has been selected based on the fact that, if the current limit is set high to allow a high inrush it will result in a high current limit during normal operation too.
- t_{latch}: The latching has been set to allow for the maximum safe length of time before shutting down the bus, allowing capacitive loads to be charged safely.
- c_{latch}: This is the maximum capacitance that can be charged via the LCL before the switch automatically disables.
- t_{on}: Time delay from switch being commanded to turn on via I2C node to actual switch turn on.

Switch	Pin	Voltage (V)	i_{latch} (A)	t_{latch} (ms)	c_{latch} (mF)	t_{on} (ms)
1	H2.08	12	1	1-20	250	0.140
2	H2.10	12	1	1-20	250	0.140
3	H2.11	BAT	1	1-20	700	0.140
4	H2.13	BAT	1	1-20	700	0.140
5	H2.13	5	1	1-20	1400	0.140

6	H2.15	5	1	1-20	1400	0.140
7	H2.16	5	1	1-20	1400	0.140
8	H2.18	3.3	1	1-20	3800	0.140
9	H2.19	3.3	1	1-20	3800	0.140
10	H2.20	3.3	1	1-20	3800	0.140

Table 9-1 PDM Switch Configuration

10. General Protection

The EPS (and wider power system) has a number of inbuilt protections and safety features designed to maintain safe operation of the EPS, battery and all subsystems supplied by the EPS buses.

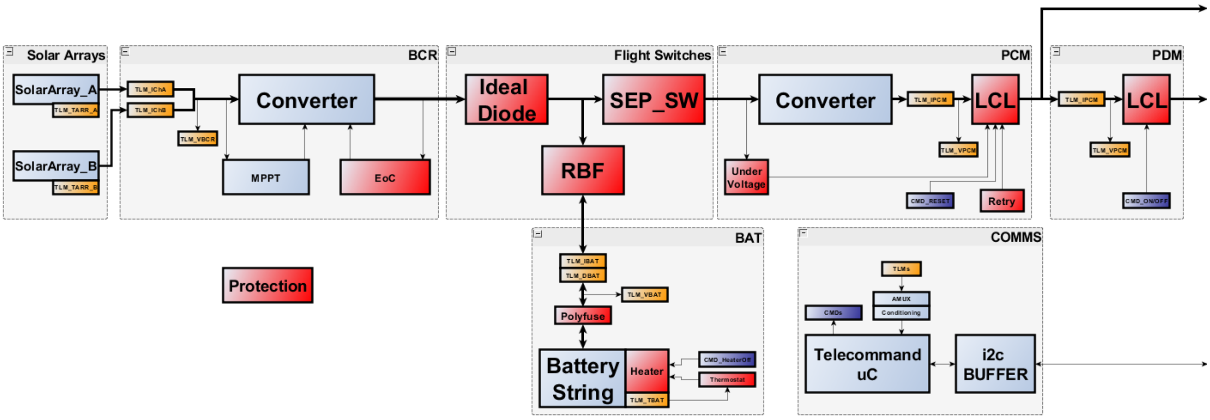

Figure 10-1 Protection Systems

10.1 Over-Current Bus Protection (LCL)

The EPS features bus protection systems to safeguard the battery, EPS and attached satellite sub-systems. This is achieved using current monitors and a shutdown network within the PCMs and PDMs.

Over-current shutdowns are present on all buses and switches for sub system protection. These are solid state switches that monitor the current and shutdown at predetermined load levels. The bus protection will then monitor the fault periodically and reset when the fault clears. The fault detection and clear is illustrated in the waveform in Figure 10-2.

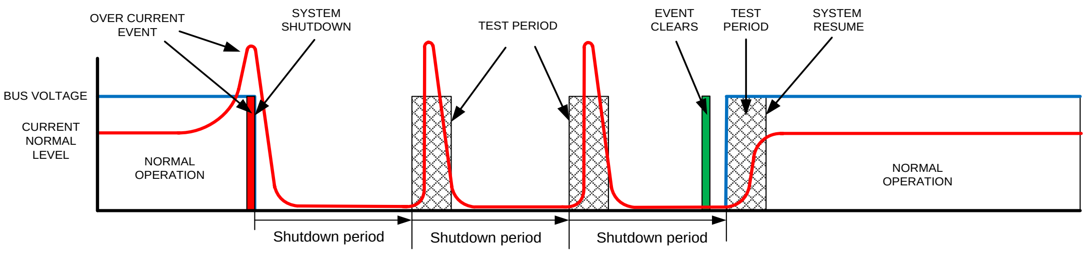

Figure 10-2 Current protection system diagram

The length of time of the test period will depend on the demand caused by the fault condition. Higher current demand results in a shorter test period. All switches and buses are protected against a short circuit fault.

10.2 Battery Under-voltage Protection

In order to prevent the over-discharge of the battery the EPS has in-built under-voltage shutdown. This is controlled by a comparator circuit with hysteresis. In the event of the battery discharging to ~6.144V (slightly above the 6.1V that results in significant battery degradation) the EPS will shut down the supply buses. This will also result in the I^2C node shutting down. When a power source is applied to the EPS (e.g. an illuminated solar panel) the battery will begin charging immediately. The buses, however, will not reactivate until the battery voltage has risen to ~7V. This allows the battery to charge to a level capable of sustaining the power lines once a load is applied.

It is recommended that the battery state of charge is monitored and loading adjusted appropriately (turning off of non-critical systems) when the battery capacity is approaching the lower limit. This will prevent the hard shutdown provided by the EPS.

Once the under-voltage protection is activated there is a monitoring circuit used to monitor the voltage of the battery. This will draw approximately 2mA for the duration of shutdown. As the EPS is designed for LEO orbit the maximum expected period in under-voltage is estimated to be ~40mins after which time the illuminated panels should bring the battery back above the 7V switch-on voltage. When ground testing this should be taken into consideration, and the battery should be recharged within 40mins of reaching under-voltage, otherwise permanent damage may be sustained.

11. TELEMETRY AND TELECOMMAND

The Telecommand and Telemetry Node (TTC) node for the EPS is based around a microcontroller. The microcontroller receives the command, processes it and acts upon the command. The commands will either be a request for telemetry or for the microcontroller to carry out an action. A block diagram representation of the TTC node is provided in Figure 11-1, below. The block diagram only shows the connections associated with the microcontroller node.

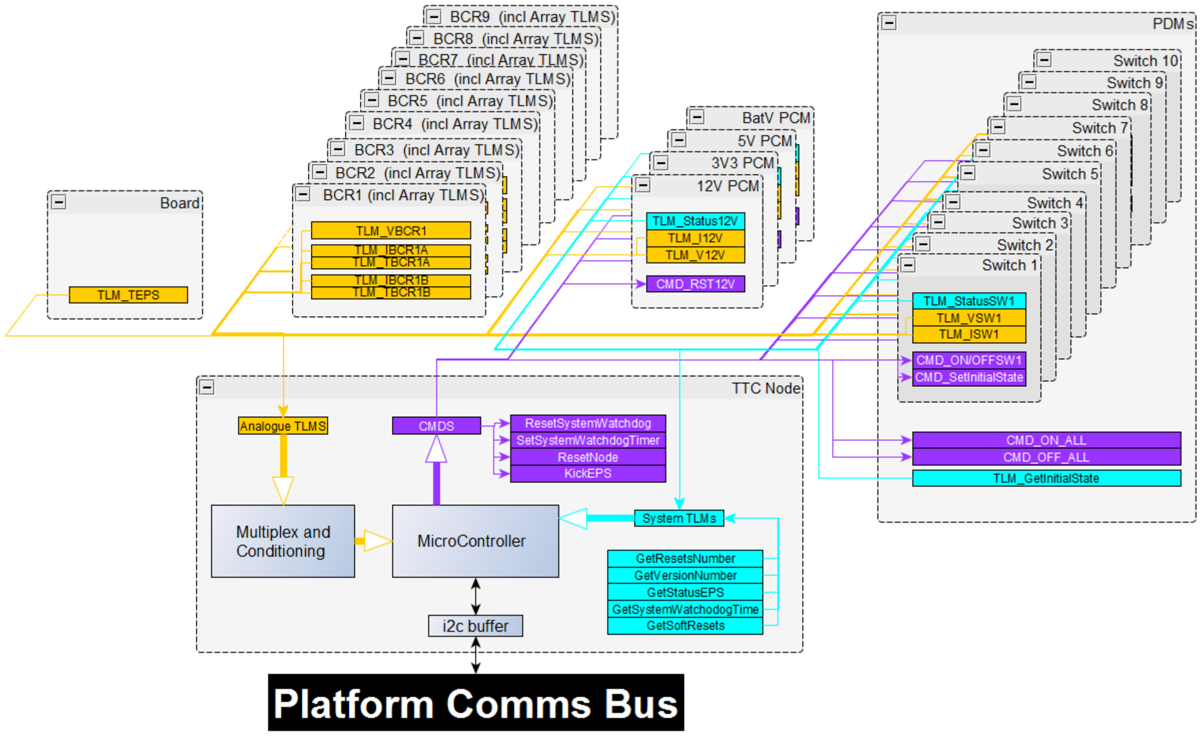

Figure 11-1 TTC node Block Diagram

All telecommand and telemetry requests should be sent with the command byte first and the data byte second. The address of the node is provided in Table 4-1. In this chapter byte 0 refers to the first byte received with byte 1 being the second received byte etc.

11.1 Commands

The commands for the node can be found in Table 11-1. A description of each command follows. The response time delay is the minimum delay which should be left between sending a command and reading the response.

Command	Value	Data	Bytes Back	Delay, ms	Type
Get Board Status	0x01	0x00	4	< 2	Discrete 16 bit
Set PCM Reset	0x02	0x01 – 0x0F	-	< 3	-
Get Version Number	0x04	0x00	4	< 2	Rev|Num
Set System Watchdog Timeout	0x06	0x01 – 0x5A	-	< 2	-
Reset System Watchdog	0x07	0x00	-	< 2	-
Get Number of System Resets	0x09	0x00	2	< 10	Uint16 0 – 255
Set PDM Initial State to OFF	0x0A	0x01 – 0x0A	-	< 20	-
Set PDM Initial State to ON	0x0B	0x01 – 0x0A	-	< 20	-
Set all PDMs ON	0x0C	0x00	-	< 2	-
Set all PDMs OFF	0x0D	0x00	-	< 2	-
Get PDM Actual Status	0x0E	0x01 – 0x0A	2	< 2	Uint16 0 – 1
Get PDM Initial State	0x0F	0x00	2	< 20	Uint16 0 – 1
Get Analogue Board Telemetry	0x10	0x00 – 0x3F	2	< 1.5	Uint16 0 - 1023
		0x40-0x7F	2	<3	Uint16 0 - 1023
Get System Watchdog Timeout	0x11	0x00	2	< 2	Uint16 1 - 90
Set PDM Switch ON	0x12	0x01 – 0x0F	-	< 2	-
Set PDM Switch OFF	0x13	0x01 – 0x0F	-	< 2	-
Get Number of Soft Resets	0x14	0x00	4	< 10	Uint16 0 – 255
Get Expected PDM Switch State	0x16	0x00	2	< 2	Discrete 10 Bit
Get Board Temperature Count Value	0x17	0x00	4	< 3	Uint16 0 – 1023
Reserved	0x40 to 0x7F				
Reset Node	0x80	0x00	-	< 1000 (TBC)	-

Table 11-1 Command Table

11.2 Command Descriptions

Get Board Status

This telemetry command retrieves the status of the firmware within the node. A breakdown of the bits is shown in Table 11-2. Once read the status bytes are cleared.

Byte	Status Bit	Description	Set to '0'	Set to '1'
0	0	Unknown Command Type	Last Command Valid	Last Command Invalid
	1	Unknown Command Value	Last Command Data in range	Last Command Data out of range
	2	-	-	-
	3	0	-	-
	4	0	-	-
	5	Watchdog Reset	Last reset Not WDT	Last Reset WDT
	6	Power On Reset	Last reset Not POR	Last Reset POR
	7	Brown Out Reset	Last reset Not BOR	Last Reset BOR
1	8	0	-	-
	9	0	-	-
	10	0	-	-
	11	0	-	-
	12	0	-	-
	13	0	-	-
	14	0	-	-
	15	0	-	-
2 (DB Node)	16	TBC	-	-
	17	TBC	TBC	TBC
	18	TBC	TBC	TBC
	19	TBC	TBC	TBC
	20	TBC	TBC	TBC
	21	TBC	TBC	TBC
	22	TBC	TBC	TBC
	23	TBC	TBC	TBC
3 (DB Node)	24	TBC	-	-
	25	TBC	TBC	TBC
	26	TBC	TBC	TBC
	27	TBC	TBC	TBC
	28	TBC	TBC	TBC
	29	TBC	TBC	TBC
	30	TBC	TBC	TBC
	31	TBC	TBC	TBC

Table 11-2 Status Bytes breakdown

If an unknown command or out of range value is sent to the board then the relevant bits within the status bit are set.

On a board reset **all** relevant reset bits are set to indicate the type of rest that occurred. Typically on power up or power reset of the board either one of (or both) POR and BOR are set. When the board undergoes a watchdog reset, either through a commanded reset or a system watchdog reset then the WDT reset is set.

Set PCM Reset

The individual power buses on the EPS can be reset using this command. Table 11-3 provides the breakdown of the data bits to reset a power bus.

Power Bus	Bit String
Battery V	0x01
5 V	0x02
3.3 V	0x04
12 V	0x08

Table 11-3 Power bus Breakdown

A combination of the bit strings can also be used. For example to reset the 5V and the Battery V bus then the data to be sent would be 0x03.

When this command is used the chosen power bus, or buses, will be held in reset for a period of approximately 500ms. This has the effect of turning off the power bus for this period of time.

It should be noted that when the 3.3V power bus is reset communication to the TTC node will be lost for the period of time the bus is held in reset. The TTC node will power up in its initial configuration.

Get Version Number

The version number of the firmware will be returned on this command. The firmware version number is encoded in the following way:

	Byte 0								Byte 1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Revision				Firmware Number											

Byte 2 (TBC)								Byte 3 (TBC)							
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Revision (DB)				Firmware Number (DB)											

Table 11-4 Version Number Breakdown

The revision number returns the current revision of the firmware that is present on the board. The firmware number returns the current firmware on the board.

Set System Watchdog Timeout

As described the EPS has a system level watchdog that trips, cycling all power buses, if it is not reset within a defined timeframe. This command sets the time out for the system level watchdog. The range that can be set is 1 to 90 minutes. As default this is set to 4 minutes.

Reset System Watchdog

Any valid command will reset the system watchdog. If the user does not require any telemetry from the board this command can be sent to reset the system watchdog.

Get Number of System Resets

This counter is designed to keep track of the number of system level resets that have occurred. This counter will roll over at 255 to 0.

[TBC] A second counter will show the number of resets on the daughter board node. – breakdown of bits to be added

Set PDM Initial State to ON

The initial power up, or reset, condition of the switches can be set. This command sets the desired switch (1 to 10) to be ON after a power up or reset has occurred.

Set PDM Initial State to OFF

The initial power up, or reset, condition of the switches can be set. This command sets the desired switch (1 to 10) to be OFF after a power up or reset has occurred.

Set all PDM's ON

When issued this commands turns all switches ON.

Set all PDM's OFF

When issued this commands turns all switches OFF.

Get PDM Actual Status

The switches have over current protection built in. As a result a switch that is expected to be on may have tripped. This command returns the actual state of the switch requested. Table 11-5 shows the definition for switches ON and OFF.

Bit	Condition
0	OFF
1	ON

Table 11-5 Switch Status Indication

Get PDM Initial State

The initial state of the switches can be returned using this command. The initial state for all the switches is returned in response to this command. The bit indication is the same as that in Table 11-5, with a 1 indicating the switch is selected to be ON at power up or reset.
The data byte switch breakdown is presented in Table 11-6.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	Sw 10	Sw 9	Sw 8
Byte 1	Sw 7	Sw 6	Sw 5	Sw 4	Sw 3	Sw 2	Sw 1	Sw 0

Table 11-6: PDM initial state result bytes

Get Analogue Board Telemetry

The TTC node has the board telemetry routed to it.

Dec	Hex (0x)	Name	Description	Uncalibrated Conversion Equation	Units
0	0x00	VBCR1	Voltage feeding BCR1	0.0249 x ADC	V
1	0x01	IBCR1A	Current BCR1, Connector SA1A	0.0009775 x ADC	A
2	0x02	IBCR1B	Current BCR1, Connector SA1B	0.0009775 x ADC	A
3	0x03	TBCR1A	Array Temp, Connector SA1A	(0.4963 x ADC) -273.15	ºC
4	0x04	TBCR1B	Array Temp, Connector SA1B	((0.4963 x ADC) -273.15	ºC
5	0x05	SDBCR1A	Sun Detector, Connector SA1A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
6	0x06	SDBCR1B	Sun Detector, Connector SA1B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
7	0x07	VBCR2	Voltage feeding BCR2	0.0249 x ADC	V
8	0x08	IBCR2A	Array Current, Connector SA2A	0.0009775 x ADC	A
9	0x09	IBCR2B	Array Current, Connector SA2B	0.0009775 x ADC	A
10	0x0A	TBCR2A	Array Temp, Connector SA2A	(0.4963 x ADC) -273.15	ºC
11	0x0B	TBCR2B	Array Temp, Connector SA2B	(0.4963 x ADC) -273.15	ºC
12	0x0C	SDBCR2A	Sun Detector, Connector SA2A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
13	0x0D	SDBCR2B	Sun Detector, Connector SA2B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
14	0x0E	VBCR3	Voltage feeding BCR3	0.00997 x ADC	V
15	0x0F	IBCR3A	Array Current, Connector SA3A	0.0009775 x ADC	A
16	0x10	IBCR3B	Array Current, Connector SA3B	0.0009775 x ADC	A
17	0x11	TBCR3A	Array Temp, Connector SA3A	(0.4963 x ADC) -273.15	ºC
18	0x12	TBCR3B	Array Temp, Connector SA3B	(0.4963 x ADC) -273.15	ºC
19	0x13	SDBCR3A	Sun Detector, Connector SA3A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
20	0x14	SDBCR3B	Sun Detector, Connector SA3B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
21	0x15	NC		-	-
22	0x16	NC		-	-
23	0x17	NC		-	-
24	0x18	NC		-	-
25	0x19	NC		-	-
26	0x1A	NC		-	-
27	0x1B	NC		-	-
28	0x1C	NC		-	-
29	0x1D	NC		-	-
30	0x1E	NC		-	-
31	0x1F	NC		-	-
32	0x20	IPCM12V	Output Current of 12V Bus	0.00207 x ADC	A
33	0x21	VPCM12V	Output Voltage of 12V Bus	0.01349 x ADC	V
34	0x22	IPCMBatV	Output Current of Battery Bus	0.005237 x ADC	A
35	0x23	VPCMBatV	Output Voltage of Battery Bus	0.009971 x ADC	V
36	0x24	IPCM5V	Output Current of 5V Bus	0.005237 x ADC	A
37	0x25	VPCM5V	Output Voltage of 5V Bus	0.005865 x ADC	V
38	0x26	IPCM3V3	Output Current of 3.3V Bus	0.005237 x ADC	A
39	0x27	VPCM3V3	Output Voltage of 3.3V Bus	0.003988 x ADC	V
40	0x28	VSW1	Output Voltage Switch1	0.01349 x ADC	V
41	0x29	ISW1	Output Current Switch 1	0.001328 x ADC	A
42	0x2A	VSW2	Output Voltage Switch2	0.01349 x ADC	V
43	0x2B	ISW2	Output Current Switch 2	0.001328 x ADC	A
44	0x2C	VSW3	Output Voltage Switch3	0.009971 x ADC	V
45	0x2D	ISW3	Output Current Switch 3	0.001328 x ADC	A
46	0x2E	VSW4	Output Voltage Switch4	0.009971 x ADC	V
47	0x2F	ISW4	Output Current Switch 4	0.001328 x ADC	A
48	0x30	VSW5	Output Voltage Switch5	0.005865 x ADC	V
49	0x31	ISW5	Output Current Switch 5	0.001328 x ADC	A
50	0x32	VSW6	Output Voltage Switch6	0.005865 x ADC	V
51	0x33	ISW6	Output Current Switch 6	0.001328 x ADC	A
52	0x34	VSW7	Output Voltage Switch7	0.005865 x ADC	V
53	0x35	ISW7	Output Current Switch 7	0.001328 x ADC	A
54	0x36	VSW8	Output Voltage Switch8	0.004311 x ADC	V
55	0x37	ISW8	Output Current Switch 8	0.001328 x ADC	A
56	0x38	VSW9	Output Voltage Switch9	0.004311 x ADC	V
57	0x39	ISW9	Output Current Switch 9	0.001328 x ADC	A
58	0x3A	VSW10	Output Voltage Switch10	0.004311 x ADC	V
59	0x3B	ISW10	Output Current Switch 10	0.001328 x ADC	A
60	0x3C	NC		-	-

61	0x3D	NC		-	-
62	0x3E	NC		-	-
63	0x3F	NC		-	-
64	0x40	VBCR4	Voltage feeding BCR4	0.0249 x ADC	V
65	0x41	IBCR4A	Current BCR4, Connector SA4	0.0009775 x ADC	A
66	0x42	IBCR4B	Current BCR4, Connector SA4	0.0009775 x ADC	A
67	0x43	TBCR4A	Array Temp, Connector SA4	(0.4963 x ADC) -273.15	ºC
68	0x44	TBCR4B	Array Temp, Connector SA4	((0.4963 x ADC) -273.15	ºC
69	0x45	SDBCR4A	Sun Detector, Connector SA4	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
70	0x46	SDBCR4B	Sun Detector, Connector SA4	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
71	0x47	VBCR5	Voltage feeding BCR5	0.0249 x ADC	V
72	0x48	IBCR5A	Current BCR5, Connector SA5	0.0009775 x ADC	A
73	0x49	IBCR5B	Current BCR5, Connector SA5	0.0009775 x ADC	A
74	0x4A	TBCR5A	Array Temp, Connector SA5	(0.4963 x ADC) -273.15	ºC
75	0x4B	TBCR5B	Array Temp, Connector SA5	((0.4963 x ADC) -273.15	ºC
76	0x4C	SDBCR5A	Sun Detector, Connector SA5	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
77	0x4D	SDBCR5B	Sun Detector, Connector SA5	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
78	0x4E	VBCR6	Voltage feeding BCR6	0.0249 x ADC	V
79	0x4F	IBCR6A	Current BCR6, Connector SA6	0.0009775 x ADC	A
80	0x50	IBCR6B	Current BCR6, Connector SA6	0.0009775 x ADC	A
81	0x51	TBCR6A	Array Temp, Connector SA6	(0.4963 x ADC) -273.15	ºC
82	0x52	TBCR6B	Array Temp, Connector SA6	((0.4963 x ADC) -273.15	ºC
83	0x53	SDBCR6A	Sun Detector, Connector SA6	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
84	0x54	SDBCR6B	Sun Detector, Connector SA6	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
85	0x55	VBCR7	Voltage feeding BCR7	0.0249 x ADC	V
86	0x56	IBCR7A	Current BCR7, Connector SA7	0.0009775 x ADC	A
87	0x57	IBCR7B	Current BCR7, Connector SA7	0.0009775 x ADC	A
88	0x58	TBCR7A	Array Temp, Connector SA7	(0.4963 x ADC) -273.15	ºC
89	0x59	TBCR7B	Array Temp, Connector SA7	((0.4963 x ADC) -273.15	ºC
90	0x5A	SDBCR7A	Sun Detector, Connector SA7	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
91	0x5B	SDBCR7B	Sun Detector, Connector SA7	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
92	0x5C	VBCR8	Voltage feeding BCR8	0.0249 x ADC	V
93	0x5D	IBCR8A	Current BCR8, Connector SA8	0.0009775 x ADC	A
94	0x5E	IBCR8B	Current BCR8, Connector SA8	0.0009775 x ADC	A
95	0x5F	TBCR8A	Array Temp, Connector SA8	(0.4963 x ADC) -273.15	ºC
96	0x60	TBCR8B	Array Temp, Connector SA8	((0.4963 x ADC) -273.15	ºC
97	0x61	SDBCR8A	Sun Detector, Connector SA8	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
98	0x62	SDBCR8B	Sun Detector, Connector SA8	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
99	0x63	VBCR9	Voltage feeding BCR9	0.0249 x ADC	V
100	0x64	IBCR9A	Current BCR9, Connector SA9	0.0009775 x ADC	A
101	0x65	IBCR9B	Current BCR9, Connector SA9	0.0009775 x ADC	A
102	0x66	TBCR9A	Array Temp, Connector SA9	(0.4963 x ADC) -273.15	ºC
103	0x67	TBCR9B	Array Temp, Connector SA9	((0.4963 x ADC) -273.15	ºC
104	0x68	SDBCR9A	Sun Detector, Connector SA9	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
105	0x69	SDBCR9B	Sun Detector, Connector SA9	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
	0x6A	RESERVED FOR ADDITIONAL DAUGHTERBOARD TELEMETRIES			
	0x7F				

Table 11-7 provides the channel details.

Dec	Hex (0x)	Name	Description	Uncalibrated Conversion Equation	Units
0	0x00	VBCR1	Voltage feeding BCR1	0.0249 x ADC	V
1	0x01	IBCR1A	Current BCR1, Connector SA1A	0.0009775 x ADC	A
2	0x02	IBCR1B	Current BCR1, Connector SA1B	0.0009775 x ADC	A
3	0x03	TBCR1A	Array Temp, Connector SA1A	(0.4963 x ADC) -273.15	ºC
4	0x04	TBCR1B	Array Temp, Connector SA1B	((0.4963 x ADC) -273.15	ºC
5	0x05	SDBCR1A	Sun Detector, Connector SA1A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
6	0x06	SDBCR1B	Sun Detector, Connector SA1B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
7	0x07	VBCR2	Voltage feeding BCR2	0.0249 x ADC	V

8	0x08	IBCR2A	Array Current, Connector SA2A	0.0009775 x ADC	A
9	0x09	IBCR2B	Array Current, Connector SA2B	0.0009775 x ADC	A
10	0x0A	TBCR2A	Array Temp, Connector SA2A	(0.4963 x ADC) -273.15	ºC
11	0x0B	TBCR2B	Array Temp, Connector SA2B	(0.4963 x ADC) -273.15	ºC
12	0x0C	SDBCR2A	Sun Detector, Connector SA2A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
13	0x0D	SDBCR2B	Sun Detector, Connector SA2B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
14	0x0E	VBCR3	Voltage feeding BCR3	0.00997 x ADC	V
15	0x0F	IBCR3A	Array Current, Connector SA3A	0.0009775 x ADC	A
16	0x10	IBCR3B	Array Current, Connector SA3B	0.0009775 x ADC	A
17	0x11	TBCR3A	Array Temp, Connector SA3A	(0.4963 x ADC) -273.15	ºC
18	0x12	TBCR3B	Array Temp, Connector SA3B	(0.4963 x ADC) -273.15	ºC
19	0x13	SDBCR3A	Sun Detector, Connector SA3A	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
20	0x14	SDBCR3B	Sun Detector, Connector SA3B	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
21	0x15	NC		-	-
22	0x16	NC		-	-
23	0x17	NC		-	-
24	0x18	NC		-	-
25	0x19	NC		-	-
26	0x1A	NC		-	-
27	0x1B	NC		-	-
28	0x1C	NC		-	-
29	0x1D	NC		-	-
30	0x1E	NC		-	-
31	0x1F	NC		-	-
32	0x20	IPCM12V	Output Current of 12V Bus	0.00207 x ADC	A
33	0x21	VPCM12V	Output Voltage of 12V Bus	0.01349 x ADC	V
34	0x22	IPCMBatV	Output Current of Battery Bus	0.005237 x ADC	A
35	0x23	VPCMBatV	Output Voltage of Battery Bus	0.009971 x ADC	V
36	0x24	IPCM5V	Output Current of 5V Bus	0.005237 x ADC	A
37	0x25	VPCM5V	Output Voltage of 5V Bus	0.005865 x ADC	V
38	0x26	IPCM3V3	Output Current of 3.3V Bus	0.005237 x ADC	A
39	0x27	VPCM3V3	Output Voltage of 3.3V Bus	0.003988 x ADC	V
40	0x28	VSW1	Output Voltage Switch1	0.01349 x ADC	V
41	0x29	ISW1	Output Current Switch 1	0.001328 x ADC	A
42	0x2A	VSW2	Output Voltage Switch2	0.01349 x ADC	V
43	0x2B	ISW2	Output Current Switch 2	0.001328 x ADC	A
44	0x2C	VSW3	Output Voltage Switch3	0.009971 x ADC	V
45	0x2D	ISW3	Output Current Switch 3	0.001328 x ADC	A
46	0x2E	VSW4	Output Voltage Switch4	0.009971 x ADC	V
47	0x2F	ISW4	Output Current Switch 4	0.001328 x ADC	A
48	0x30	VSW5	Output Voltage Switch5	0.005865 x ADC	V
49	0x31	ISW5	Output Current Switch 5	0.001328 x ADC	A
50	0x32	VSW6	Output Voltage Switch6	0.005865 x ADC	V
51	0x33	ISW6	Output Current Switch 6	0.001328 x ADC	A
52	0x34	VSW7	Output Voltage Switch7	0.005865 x ADC	V
53	0x35	ISW7	Output Current Switch 7	0.001328 x ADC	A
54	0x36	VSW8	Output Voltage Switch8	0.004311 x ADC	V
55	0x37	ISW8	Output Current Switch 8	0.001328 x ADC	A
56	0x38	VSW9	Output Voltage Switch9	0.004311 x ADC	V
57	0x39	ISW9	Output Current Switch 9	0.001328 x ADC	A
58	0x3A	VSW10	Output Voltage Switch10	0.004311 x ADC	V
59	0x3B	ISW10	Output Current Switch 10	0.001328 x ADC	A
60	0x3C	NC		-	-
61	0x3D	NC		-	-
62	0x3E	NC		-	-
63	0x3F	NC		-	-
64	0x40	VBCR4	Voltage feeding BCR4	0.0249 x ADC	V
65	0x41	IBCR4A	Current BCR4, Connector SA4	0.0009775 x ADC	A
66	0x42	IBCR4B	Current BCR4, Connector SA4	0.0009775 x ADC	A
67	0x43	TBCR4A	Array Temp, Connector SA4	(0.4963 x ADC) -273.15	ºC
68	0x44	TBCR4B	Array Temp, Connector SA4	((0.4963 x ADC) -273.15	ºC
69	0x45	SDBCR4A	Sun Detector, Connector SA4	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
70	0x46	SDBCR4B	Sun Detector, Connector SA4	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
71	0x47	VBCR5	Voltage feeding BCR5	0.0249 x ADC	V
72	0x48	IBCR5A	Current BCR5, Connector SA5	0.0009775 x ADC	A
73	0x49	IBCR5B	Current BCR5, Connector SA5	0.0009775 x ADC	A

74	0x4A	TBCR5A	Array Temp, Connector SA5	(0.4963 x ADC) -273.15	ºC
75	0x4B	TBCR5B	Array Temp, Connector SA5	((0.4963 x ADC) -273.15	ºC
76	0x4C	SDBCR5A	Sun Detector, Connector SA5	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
77	0x4D	SDBCR5B	Sun Detector, Connector SA5	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
78	0x4E	VBCR6	Voltage feeding BCR6	0.0249 x ADC	V
79	0x4F	IBCR6A	Current BCR6, Connector SA6	0.0009775 x ADC	A
80	0x50	IBCR6B	Current BCR6, Connector SA6	0.0009775 x ADC	A
81	0x51	TBCR6A	Array Temp, Connector SA6	(0.4963 x ADC) -273.15	ºC
82	0x52	TBCR6B	Array Temp, Connector SA6	((0.4963 x ADC) -273.15	ºC
83	0x53	SDBCR6A	Sun Detector, Connector SA6	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
84	0x54	SDBCR6B	Sun Detector, Connector SA6	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
85	0x55	VBCR7	Voltage feeding BCR7	0.0249 x ADC	V
86	0x56	IBCR7A	Current BCR7, Connector SA7	0.0009775 x ADC	A
87	0x57	IBCR7B	Current BCR7, Connector SA7	0.0009775 x ADC	A
88	0x58	TBCR7A	Array Temp, Connector SA7	(0.4963 x ADC) -273.15	ºC
89	0x59	TBCR7B	Array Temp, Connector SA7	((0.4963 x ADC) -273.15	ºC
90	0x5A	SDBCR7A	Sun Detector, Connector SA7	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
91	0x5B	SDBCR7B	Sun Detector, Connector SA7	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
92	0x5C	VBCR8	Voltage feeding BCR8	0.0249 x ADC	V
93	0x5D	IBCR8A	Current BCR8, Connector SA8	0.0009775 x ADC	A
94	0x5E	IBCR8B	Current BCR8, Connector SA8	0.0009775 x ADC	A
95	0x5F	TBCR8A	Array Temp, Connector SA8	(0.4963 x ADC) -273.15	ºC
96	0x60	TBCR8B	Array Temp, Connector SA8	((0.4963 x ADC) -273.15	ºC
97	0x61	SDBCR8A	Sun Detector, Connector SA8	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
98	0x62	SDBCR8B	Sun Detector, Connector SA8	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
99	0x63	VBCR9	Voltage feeding BCR9	0.0249 x ADC	V
100	0x64	IBCR9A	Current BCR9, Connector SA9	0.0009775 x ADC	A
101	0x65	IBCR9B	Current BCR9, Connector SA9	0.0009775 x ADC	A
102	0x66	TBCR9A	Array Temp, Connector SA9	(0.4963 x ADC) -273.15	ºC
103	0x67	TBCR9B	Array Temp, Connector SA9	((0.4963 x ADC) -273.15	ºC
104	0x68	SDBCR9A	Sun Detector, Connector SA9	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
105	0x69	SDBCR9B	Sun Detector, Connector SA9	<512 Illuminated, >512 Unilluminated (TBC)	Illuminated/ Unilluminated
	0x6A	RESERVED FOR ADDITIONAL DAUGHTERBOARD TELEMETRIES			
	0x7F				

Table 11-7 Telemetry Channels

The format of the returned bytes is:

	Byte 0								Byte 1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	ADC Result										

Get System Watchdog Timeout

This command provides the user with the current system watchdog timeout that is set. The returned value is indicated in minutes.

Set PDM Switch ON

This command turns on the desired switch.

Set PDM Switch OFF

This command turns off the desired switch.

Get Number of Soft Resets

This command returns the number of soft resets. Soft resets are resets that have been commanded by the user. This counter will roll over at 255 to 0.

Get Expected PDM Switch State

The expected PDM switch state will be returned using this command. This command returns the expected state of all the switches. Table 11-5 can be used to decode the data returned.

Bit	7	6	5	4	3	2	1	0
Byte 0	0	0	0	0	0	Sw 10	Sw 9	Sw 8
Byte 1	Sw 7	Sw 6	Sw 5	Sw 4	Sw 3	Sw 2	Sw 1	Sw 0

Get Board Temperature Count Value

This command returns a count value representing the temperature of the board.

The format of the returned bytes is:

	Byte 0								Byte 1							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	ADC Result										

$$\boldsymbol{TEMP}(°\mathrm{C}) = \mathbf{0.3724} \times \boldsymbol{Count_{ADC}} - \mathbf{273.15}$$

Reset Node

If required the user can reset the TTC node using this command. On issue the board will reset within 1s. This command will result in the board being brought up in its defined initial condition.

12. TEST

All EPS are fully tested prior to shipping, and test reports are supplied. In order to verify the operation of the EPS please use the following outlined instructions.

12.1 Required Equipment

- Solar Arrays (or simulated solar array supply)
- EPS
- Remove Before Flight Pin (or shorting harness)
- Separation Switch (or shorting harness)
- Battery (or simulated battery)
- Breakout Connector (with connections as per Figure 12-1)
- Oscilloscope
- Multimeter
- Electronic Load
- Method to communicate with TTC node

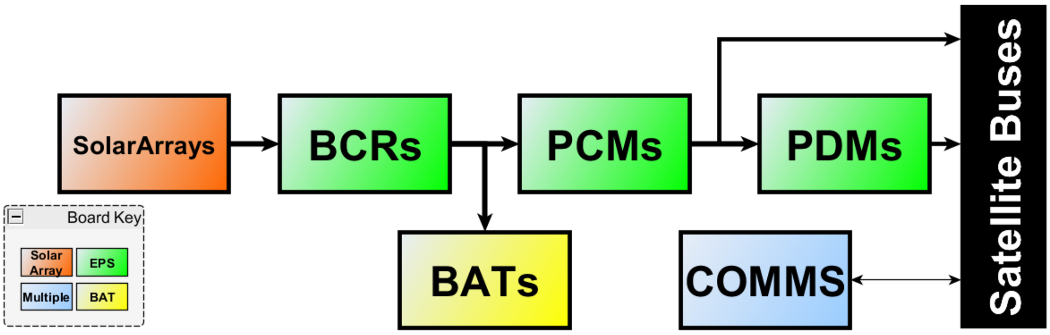

Figure 12-1 Full System Required for Test

Solar Arrays

During test phases it is not always possible to use solar arrays for testing. Other options for testing include solar array simulators or (for approximation testing) a PSU and an inline resistor.

If using a solar array simulator you should ensure the setup does not exceed the operating maximums of the EPS. Table 12-1 shows the characteristics of the different compatible panel setups for the arrays.

Series Cells	V_{oc} (V)	V_{mpp} (V)	I_{sc} (mA)	I_{mpp} (mA)	Compatible BCRs
2	5.32	4.70	453.871	433.906	BCR3
3	7.98	7.05	453.871	433.906	BCR3
4	10.64	9.40	453.871	433.906	BCRs 1,2,4,5,6,7,8,9
5	13.30	11.75	453.871	433.906	BCRs 1,2,4,5,6,7,8,9
6	15.96	14.10	453.871	433.906	BCRs 1,2,4,5,6,7,8,9
7	18.62	16.45	453.871	433.906	BCRs 1,2,4,5,6,7,8,9

8	21.28	18.80	453.871	433.906	BCRs 1,2,4,5,6,7,8,9

Table 12-1 Examples of Solar Array Configurations – Spectrolab UTJ cells @ BOL, 28°C

If a solar array simulator is not available it is possible to approximate solar array operation with a power supply and an inline power resistor.

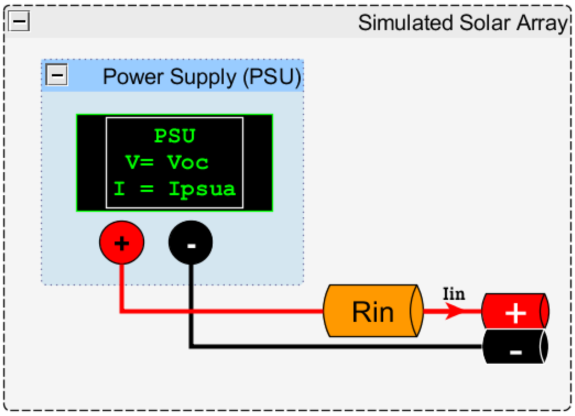

Figure 12-2 Simulated Solar Array Setup

The value of the resistor will set the current supplied and can be calculated as follows:

$$R_{in} = \frac{0.17 \times V_{oc}}{I_{in}}$$

I_{in} = the current required (normally the maximum power point current)
R_{in} = the resistance of the inline resistor selected
V_{oc} = the expected open circuit voltage of the solar array.

I_{in} is normally set, using R_{in}, to match the maximum power point current (I_{mpp}) of the expected array, but can be adjusted to simulate lower illumination conditions.

The PSU should be set using V_{oc} as the voltage setting and 2x I_{in} as the current limit (I_{psua})

Battery

During test phases it is not always possible or advisable to use a battery. For example to test End of Charge or undervoltage shutdown operation you may want to alter the battery voltage manually rather than wait for a battery to charge/discharge.

When testing without a battery the system requires a simulated battery to be attached. This can be achieved by using a PSU (to set the battery and supply current when required/discharging) and an electronic load (to simulate the battery taking current/charging) connected in parallel.

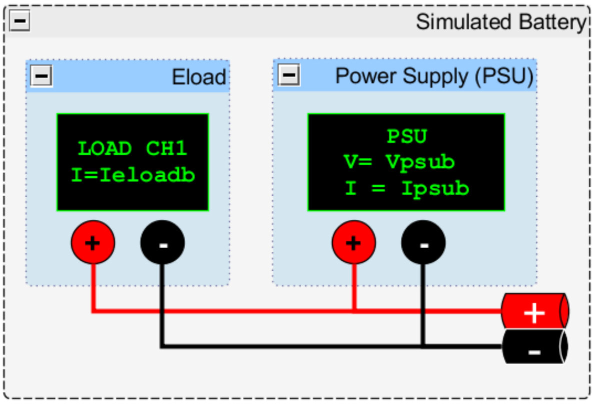

Figure 12-3 Simulated Battery Setup

The PSU should be set using the voltage as the required battery voltage (V_{psub}) and a current limit of 2C (I_{psub}) (the highest recommended discharge rate of the battery). The electronic load current (I_{eloadb}) setting should be set to approximately 1C of the battery to be used. You must also ensure the eLoad setting is higher than the supplied BCR current, otherwise the BCR will be pushed into EoC.

Flight Switches

For initial testing it is likely that the flight switches will not be wired in. In this instance it is possible to use test switches in order to operate the system by connecting them to J1 and J3 (This configuration is set up for a single separation switch, so either J1 or J2 is used). These should be wired and marked to ensure that they match the expected configuration of the satellite.

12.2 Basic System Setup

Before any testing commences all equipment described above should be used with limits set up appropriately.

All PSUs should be switched off.

Connect Flight switches to connectors J1 and J3 and ensure they are set to simulate the Remove Before Flight switch being inserted and the Separation Switches are compressed.

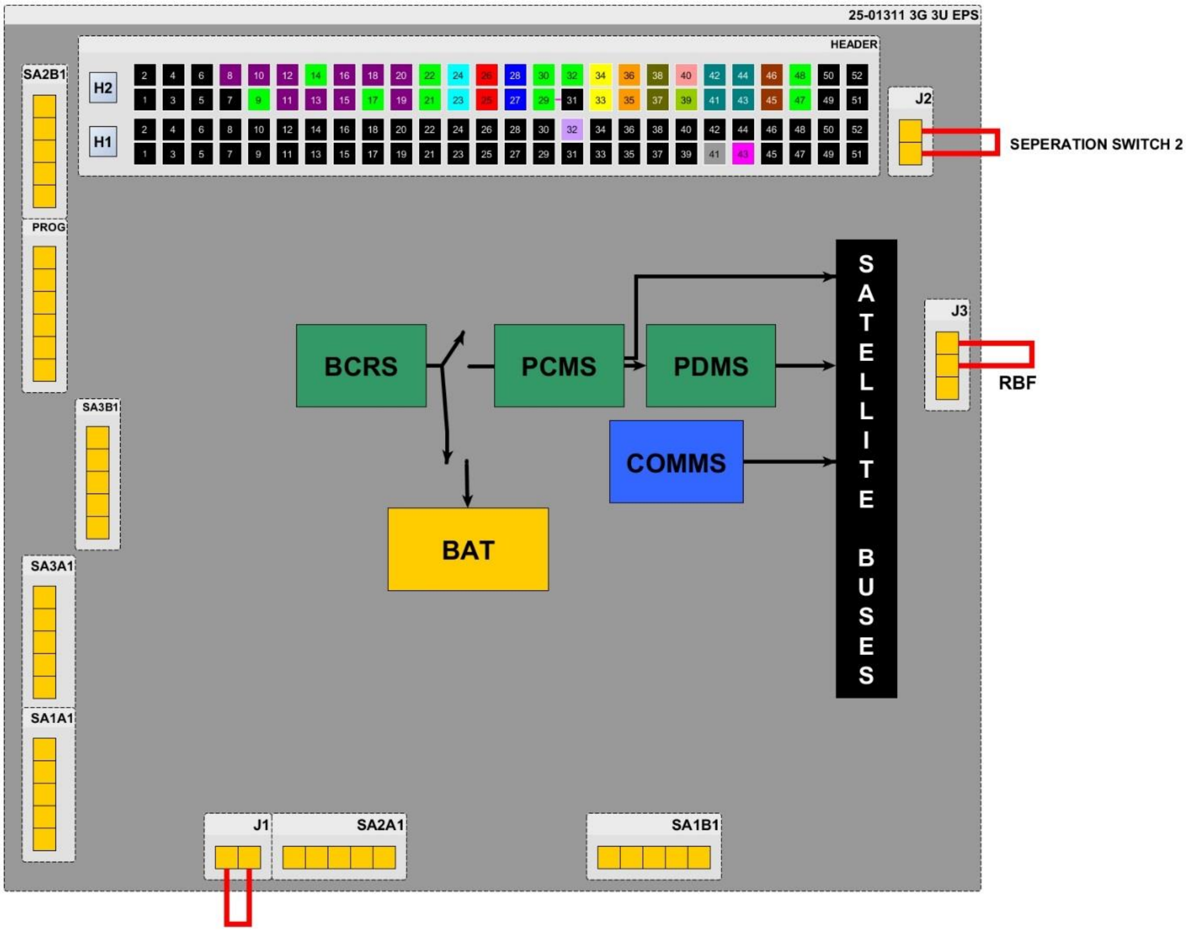

Figure 12-4 Flight Switches Isolating Battery and PCM

Connect the Battery (or simulated battery – Switch on the PSU and eLoad).

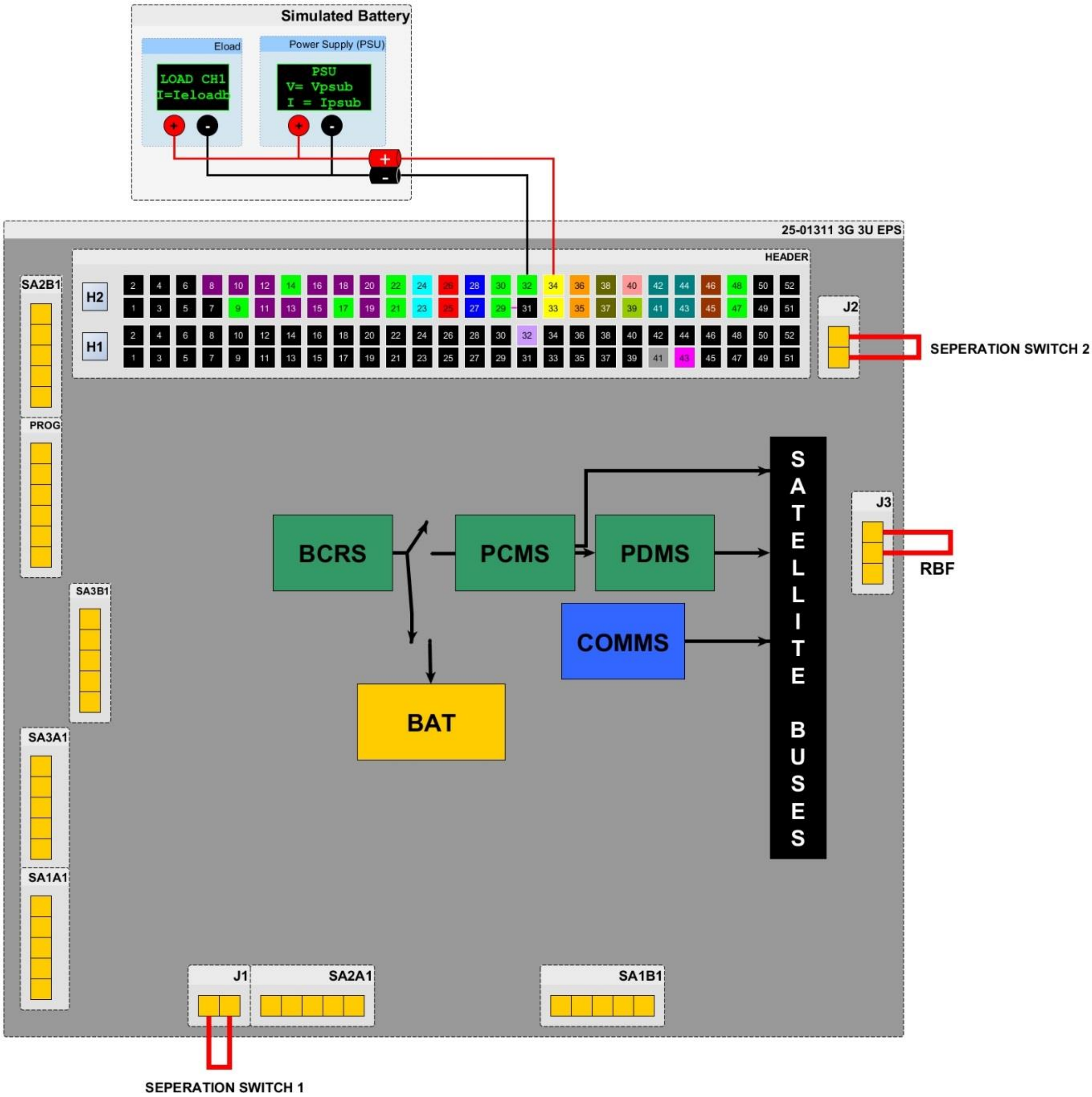

Figure 12-5 Connect Battery and Switch on PSU and eLoad

Verify that the Switches are operating correctly (i.e. there is no power supplied on the buses and no current drawn from the “battery”).

Remove the RBF switch.

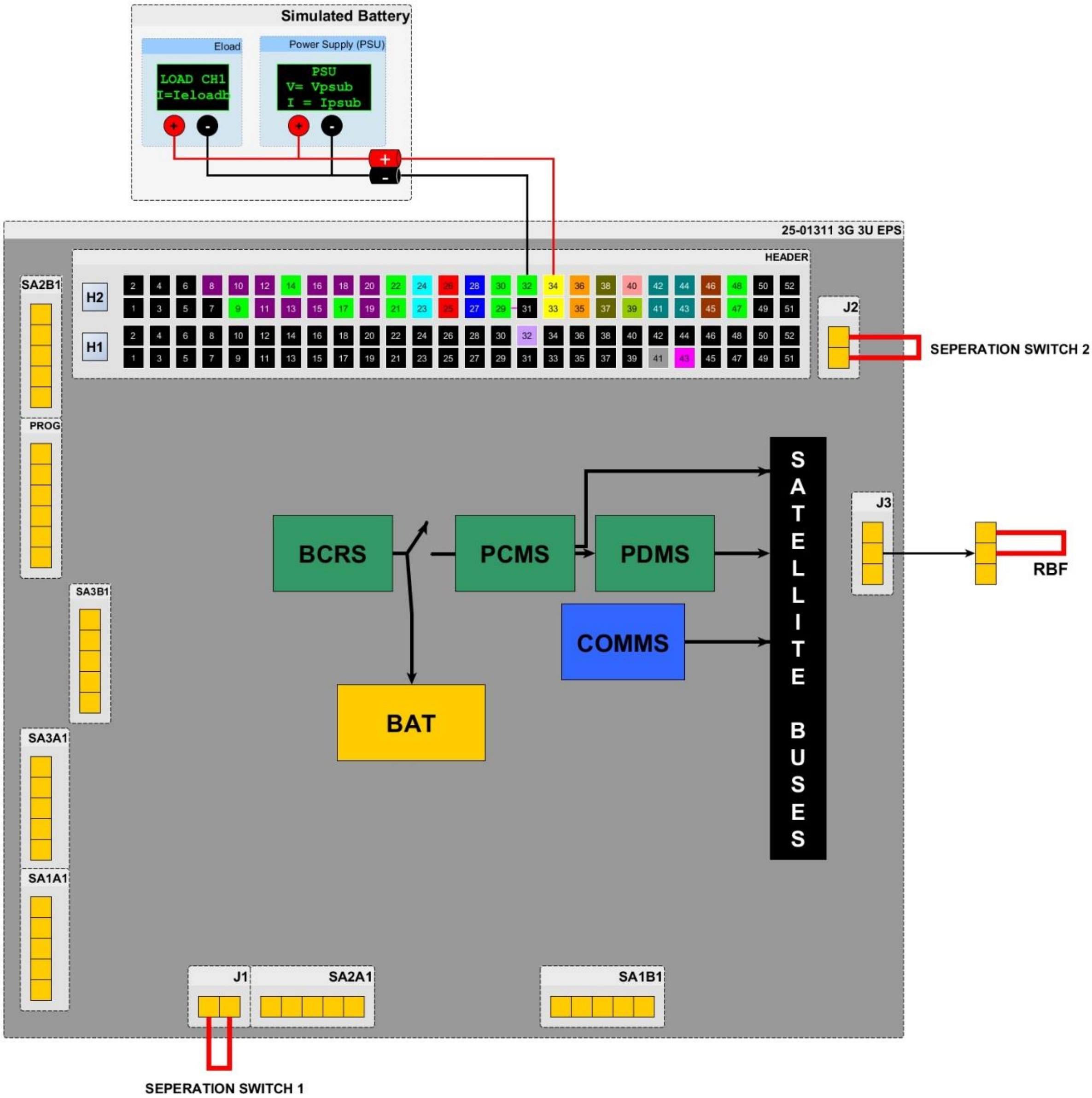

Figure 12-6 Remove RBF

The Battery voltage will now be present on the main header BCR_OUT.

Activate a separation switch.

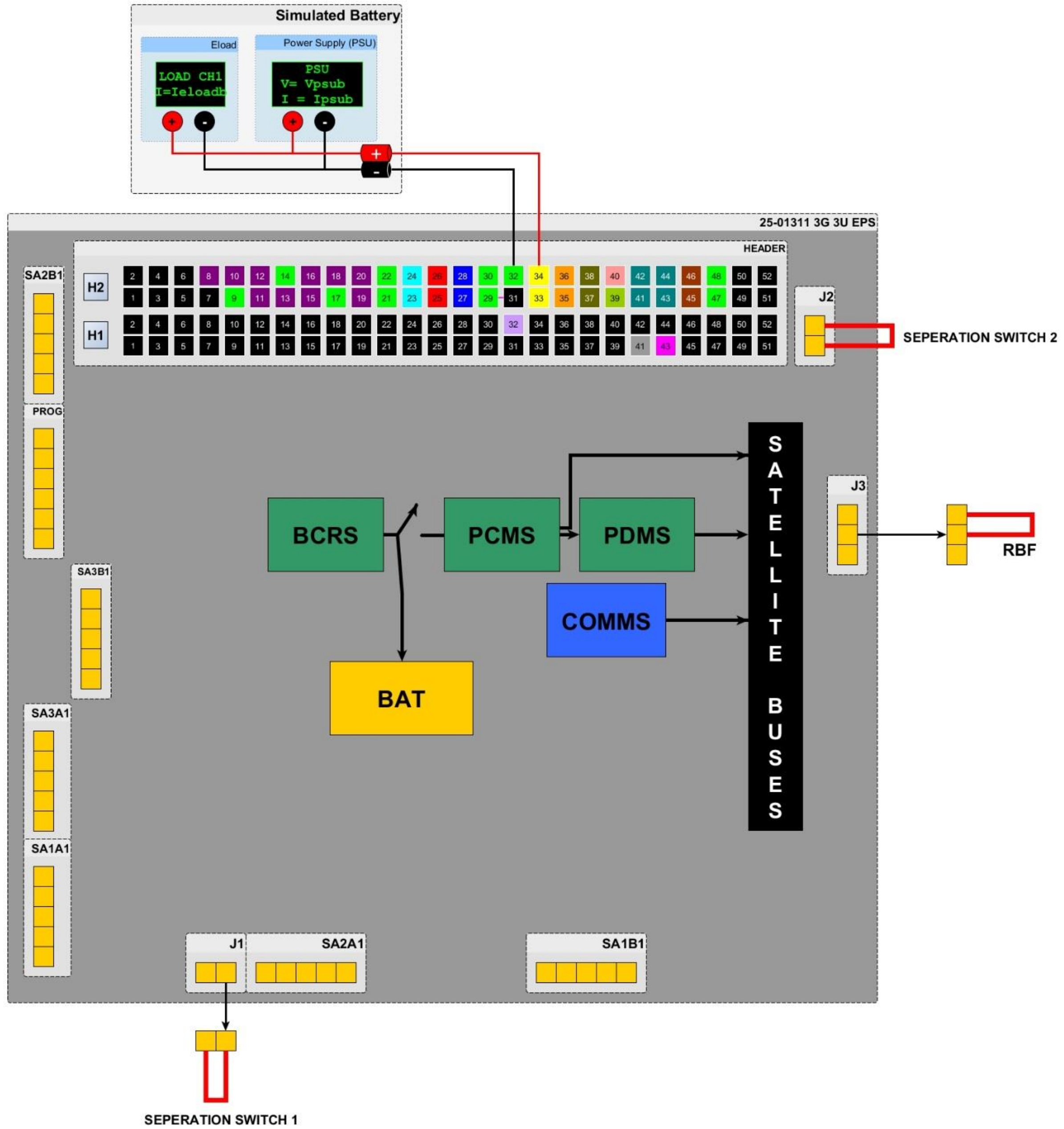

Figure 12-7 Separation Switch Activation

Check that the system is operational (all power buses at expected voltages).

Once this has been set up it is possible to test all functions of the EPS.

For more detail on the individual tests performed on the EPS refer to the test report, which includes test setups and processes.

13. Compatible Systems

	Compatibility	Notes
Stacking Connector	CubeSat Kit Bus	
Batteries	Clyde Space Battery Systems CS-SBAT2-10/-20/-30 CS-RBAT2-10	10W/hr – 30 W/hr Lithium Ion Polymer
	Lithium Polymer 8.2v	(2s1p) to (2s3p)(1) More strings can be connected in parallel to increase capacity if required
	Lithium Ion 8.2v	(2s1p) to (2s3p) (1) More strings can be connected in parallel to increase capacity if required
	Other Batteries	Please contact Clyde Space
Solar Arrays	Clyde Space 2cell solar array	Connects to BCR 3 via SA3
	Clyde Space 5-8cell solar array	Connects to BCR 1/2 via SA1/2
	Other array technologies	Any that conform to the input ratings for Voltage and Current(2)
Structure	Pumpkin	CubeSat 1/2/3U standard structure
	ISIS	CubeSat 1/2/3U standard structure
	Other structures	Please contact Clyde Space

Table 13-1 Compatibilities

(1) Refers to series and parallel connections of the cells within the battery system. e.g. 2s1p indicates a single string of two cells in series.
(2) May require some alteration to MPPT. Please contact Clyde Space.