

Description of the pipelineRegister circuit files for Labs 8 –Pipeline CPU

The pipeline registers are designated by a number indicating which stages they bridge and a descriptor indicating the information stored at that stage.

- 1 indicates the IF/ID register
 - 2 indicates the ID/EX registers
 - 3 indicates the EX/Mem registers
 - 4 indicate the Mem/WB registers
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- PC indicates the address information needed to compute branch and jump PC addresses
 - Ctrl indicate control lines
 - DP indicates the main data-path
 - ALUCtrl indicates the copy of ctrl going to the ALUControl
 - Rd indicates the destination register for write-back

The initial file is pipelineRegisters-start.circ. It includes the following completed pipeline registers which are used in PipelineARM-CPU1-start.circ:

PipeReg1 (only one pipeline register needed here for PC+4 and Instruction)

PipeReg2PC (stores PC+4)

PipeReg2Ctrl (stores all control values)

PipeReg2DP (stores data path values from A-reg, B-reg, and extended immediate)

PipeReg2ALUCtrl/Rd (stores opcode and possible destination register rd)

You need to complete this file by creating the following pipeline registers:

PipeReg3Br (stores computed branch address)

PipeReg3Ctrl (stores control values that need to pass to the Mem and WB stages)

PipeReg3DP (store the data values that pass from EX to Mem stages, namely zero line from ALU, ALU result, value from rt for possible sw instruction)

PipeReg3-4Reg (stores destination register number) Two copies of this register are used, one in the EX/Mem transfer and one in the Mem/WB transfer.

PipeReg4Ctrl (stores control values that need to pass to the WB stage)

PipeReg4DP (stores data values from ALU and memory to pass to the WB stage)