ADC 8-bit Front-End (BD)

Product Guide

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Overview

ADC_8_bits is a Block Design (BD) wrapper that exposes an **8-bit** digital stream from the FPGA's on-chip **XADC**. It includes:

- **XADC Wizard** configured for `VAUXP1/VAUXN1` single-ended channel.
- **Clock Wizard** generating a **10 MHz** DCLK for the XADC from the external `clock_i`.
- **DRP tie-offs**: `DEN` tied to `EOC` (continuous sampling), `DWE=0`, `DI=0`, `DADDR=0x11`.
- **Slice** (`xlslice`) exporting `DO[15:8]` as the 8-bit sample on `data_o`.

Key Features

- Single clock domain, active-high reset.
- Continuous conversion on `VAUX1`; samples presented as the **8 MSBs** of the 16-bit XADC result.
- Minimal interface: analog pair (`VP_i/VN_i`), `clock_i`, `reset_i`, and `data_o[7:0]`.

Ports

Name	Dir	Width	Description
`VP_i`	in	1	Analog positive input to XADC (VAUXP1).
`VN_i`	in	1	Analog negative input to XADC (VAUXN1).
`clock_i`	in	1	External reference clock. Internally used by Clock Wizard.
`reset_i`	in	1	Asynchronous reset, active-high (forwarded to XADC/Clock Wiz).
`data_o`	out	8	Sample output = `XADC.DO[15:8]` (8 MSBs of conversion result).

Clock / Reset

- **clock_i:** single external clock. Typical packaging uses `FREQ_HZ = 100 MHz`.
- **Clock Wizard:** generates **10 MHz** (`CLKOUT1`) for `XADC.DCLK` *(default BD configuration)*.
- **reset_i:** asynchronous, **active-high**; forwarded to XADC `reset_in` and Clock Wizard `reset`.

Operation (Simplified)

1. Provide a stable `clock_i`, deassert `reset_i`.
2. The Clock Wizard generates `10 MHz` for XADC `dclk_in`.
3. XADC runs continuous conversions on `VAUX1` (with `DEN` driven by `EOC`).
4. Each completed conversion updates `DO[15:0]`; the design exposes `DO[15:8]` on `data_o[7:0]`.

Data Format

- **data_o[7:0]** = *MSB[15] ... MSB-7[8]* of the XADC 16-bit result.
- This is a compact 8-bit representation (MSB-aligned). If a 12-bit sample is needed, export `DO[15:4]`.

XADC Configuration (BD Defaults)

- Channel: `VAUXP1/VAUXN1` (single channel).
- DRP: `DADDR=0x11`, `DI=0`, `DWE=0`, `DEN=EOC`.
- **Note:** XADC VAUX inputs are typically **0 V to 1.0 V** full-scale (refer to device datasheet). Use proper analog conditioning.

Integration Notes

- Constrain `clock_i` with the correct period in XDC; ensure the input frequency matches the Clock Wizard setup.
- Constrain `VP_i/VN_i` to the correct analog-capable package pins for `VAUX1`.
- If you need a different sample rate, regenerate the Clock Wizard for a new `DCLK`.

Versioning & License

- IP: `ADC_8_bits`, Version: **v1.0**.
- License: **MIT**. Produced for the AMD Open Hardware University Design Competition 2025.

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