Sky130 SRAM Macro Report

Author: Ryan Cramer

Cal Poly SLO

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I. Introduction

When working with an ASIC flow such as OpenLane2, you must select a process node. The process node will come with a process development kit, which includes the libraries and settings for a specific silicon process. Only certain nodes can be produced by certain manufacturers. One open-source node commonly used is Skywater's 130nm process, called Sky130, which has been used by Efabless. Although it has a fairly developed standard cell library (SCL), Sky130 has a limited number of reliable memory macros, with DFFRAM and SRAM of small sizes such as 256B-8kB.

For Cal Poly's CARP, our team is trying to design a small RISC-V SoC running FreeRTOS. It must be stated that FreeRTOS is marketed primarily towards small embedded systems, with 16kB-256kB being the targeted range. As a CPE student at Cal Poly, you must produce an FPGA-based implemented of the "OTTER", a single core RISC-V microcontroller. The original OTTER utilized 64kB of the Artix-7's 128kB of on-chip SRAM. We need to at least expand the macro to 16kB, which is not available, or instantiate multiple 8kB SRAM.

II. Macro Options

OpenRAM: VLSIDA/OpenRAM

- OpenRAM is a python application that creates the necessary files to use SRAMs in ASIC designs
- It is an open-source static memory compiler
    - o NCSU FreePDK 45nm
        - ▪ non-fabricable (Calibre/Klayout for DRC/LVS)
    - o MOSIS 0.35um
        - ▪ fabricable (Magic/Netgen or Calibre for DRC/LVS)
    - o Skywater 130nm (sky130)
        - ▪ fabricable (Magic/Netgen or Klayout)

1. Front End Mode:
    a. Generates SPICE, layout, timing models
        i. netlist only mode can skip physical design if FPGA implementation is desired
    b. No DRC/LVS
    c. Estimates power/delay automatically
2. Back End Mode:
    a. Generates SPICE, layout, timing models
    b. Performs DRC/LVS

SKY130-Macro-Memory-Cell-Generator: Baungarten-CINVESTAV

- A system to automate creation of varied memory arrays using custom floorplans, and capitalizing on interleaving memory.
- Allows user to get by with the 3 Sky130 SRAM macros currently available
- Supplies necessary files for OpenLane (OpenLane2 not supported, macros outdated)
- Simplified python script with command line arguments for sizing and options

USAGE: python3 imem_generator.py [mt] [wn] [ad] [p] [op1] [op2]

- [mt] = Memory Type (which Sky130 macro generate?)
- [wn] = Word Width
- [ad] = address count
- [p] = placement (g = grid, r = row, c = column, ct = custom, a = auto)
- [op1] = # of columns if p = ct, and horizontal micrometers if p = a (integer)
- [op2] = # of rows (max value of 10) if p = ct and vertical micrometers if p=a (integer)

Output Structure:

- Provides a designs folder for storing generated memory structures.
- The folder follows a specific naming convention and houses essential files and sub-folders for compatibility with OpenLane (also provides SVG and PNG schematics)