RE: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

Ciaran Lappin <ciaran.lappin@microsemi.com> Fri, Jun 30, 2017 at 2:38 AM
To: Michael John Klopfer <mklopfer@uci.edu>
Cc: Ted Marena <ted.marena@microsemi.com>, Farhad Mafie <Farhad.Mafie@microsemi.com>, Tim Mccarthy <Tim.McCarthy@microsemi.com>, "G. P. Li" <gpli@calit2.uci.edu>, Zihan Chen <zihanc3@uci.edu>, "Crystal L. Lai" <cllai1@uci.edu>, Cyril Jean <Cyril.Jean@microsemi.com>

HI Michael,

Just one or two comments on your getting started guide.

Regards,

Ciaran

From: Michael John Klopfer [mailto:mklopfer@uci.edu]
Sent: Friday, June 30, 2017 7:06 AM
To: Ciaran Lappin <ciaran.lappin@microsemi.com>
Cc: Ted Marena <ted.marena@microsemi.com>; Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Cyril Jean <Cyril.Jean@microsemi.com>
Subject: Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

EXTERNAL EMAIL

Hi Ciaran,

I had a chance to test the operation of your instructions. Everything worked perfectly. Thanks!

Quick question. For the multiple RISC-V FPGA designs that are available in the example projects for SF2 - what are the differences? For example, what are the modifications to the RISC-V base project and the one used for the Tic-Tac-Toe example? Is is just execution memory addresses?

Also, attached is a quick visual guide I put together to help teach from for students quickly getting the SF2 RISC-V Tic-Tac-Toe example working in Windows. This is just a start.

Best,

--

Michael J. Klopfer, PhD

Technical Director

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On Wed, Jun 28, 2017 at 9:04 AM, Michael John Klopfer <mklopfer@uci.edu> wrote:

> Thank you Ciran! Exactly what I was looking for.
>
> We are in the process of building out teaching documentation for RISC-V for the Future Creative Board, Attached is an old version created by Bronco (Zihan) for SoftConsole 5.0 (Linux) - you may have seen it already. As we progress, I will send you updates. Please feel free to incorporate any text into official documentation if helpful.
>
> best,
>
> --
>
> Michael J. Klopfer, PhD
>
> Technical Director
>
> CalPlug - California Plug Load Research Center
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>
>
> On Wed, Jun 28, 2017 at 8:26 AM, Ciaran Lappin <ciaran.lappin@microsemi.com> wrote:
>
> > Hi Michael,
> >
> > When debugging using SC the programming file gets loaded into the DDR at 0x80000000. At the minute to load an image into envm (at 0x60000000)
> >
> > the steps below should work, if the RISCVs reset vector should be set to 0x60000000.

- Build the project using the linker script attached.
- Open the workspace/project/Debug folder
- Copy the hex to the ihx or hex folder in the CoreRISCV project folder.
- Open the .hex file
- Remove the top line of the .hex file and save

In Libero:

- Build the design up to Generate FPGA Array Data
- Double click on Update eNVM Memory Content
- Open the RISCV_BOOT client
- Browse to the directory where the .hex is saved
- Uncheck “Use as ROM”
- Click the following Oks
- Complete the design flow and download to the board.
- Restart the board and it should boot from the envm.

The current program in the RISCV_BOOT envm client is not required it can be replaced if needed. The M3-Disable client, which is used on board with the Cortex M3 is required. It is used to setup the DDR and put the M3 into a “sleep” mode so the riscv can run. Having a small program in the example projects is a simple way of showing the system working without the need to run a debug session each time.

Regards,

Ciaran

From: Michael John Klopfer [mailto:mklopfer@uci.edu]
Sent: Wednesday, June 28, 2017 3:40 PM

To: Ciaran Lappin <ciaran.lappin@microsemi.com>
Cc: Ted Marena <ted.marena@microsemi.com>; Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Cyril Jean <Cyril.Jean@microsemi.com>
Subject: Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

EXTERNAL EMAIL

Hi Ciaran,

Just curious if you had an answer to my question:

"We have figured out the workflow for the RISC-V TicTacToe example for uploading the firmware file to the SF2 with FlashPro and using Libero SOC to update the fabric and eNVM memory for the project. Likewise we can build and execute the source code from SoftConsole 5.1 in debug executing from RAM.

The part that is hazy to me still is the generation of a production file from SoftConsole and "uploading" to the board to execute on bootup - the linker uses the production linker script, so we believe this is not the issue. Even after reviewing the current RISC-V Microsemi documentation, I am still a little unclear on the workflow for this case. Does the production binary get uploaded to the eNVM, or is the current program in the eNVM required (what is being placed there from the sample project in Libero SoC) as a bootloader? I tried uploading to eNVM in Libero, but the size is incorrect, then I remembered being told the program executes from the on board flash ROM. Is there a reparate tool to place the binary to the C program on an external ROM and the bootloader in the eNVM helps to execute on runtime? Would you mind pointing me to the workflow and procedure for uploading a generated production binary for RISC-V to run at bootup?"

Best,

--

Michael J. Klopfer, PhD

Technical Director

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On Wed, Jun 21, 2017 at 9:07 AM, Michael John Klopfer <mklopfer@uci.edu> wrote:

> Hi Ciaran,
>
> Much appreciated! Thank you for pointing out that oversight on my part. Is there a visual guide in current or planned preparation for the Future Creative board for RISC-V/SoftConsole 5.1/Libero SoC 11.8 similar to the one attached? I believe Tim Macarthy's group was involved with authoring this one. This guide was extremely helpful to teach from - from this type of guide the students can get moving quickly. Our group added some annotations at the end of the document for Semihosting based on Tim's input.
>
> On quick question. We have figured out the workflow for the RISC-V TicTacToe example for uploading the firmware file to the SF2 with FlashPro and using Libero SOC to update the fabric and eNVM memory for the project. Likewise we can build and execute the source code from SoftConsole 5.1 in debug executing from RAM.
>
> The part that is hazy to me still is the generation of a production file from SoftConsole and "uploading" to the board to execute on bootup - the linker uses the production linker script. Even after reviewing the current RISC-V Microsemi documentation, I am still a little hazy on the workflow. Does the production binary get uploaded to the eNVM, or is the current program in the eNVM required (what is being placed there from the sample project in Libero SoC) as a bootloader? I tried uploading to eNVM in Libero, but the size is incorrect, then I remembered being told the program executes from the on board flash ROM. Would you mind pointing me to the workflow and procedure for uploading a generated production binary for RISC-V to run at bootup?
>
> Best,

--

Michael J. Klopfer, PhD

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On Wed, Jun 21, 2017 at 1:31 AM, Ciaran Lappin <ciaran.lappin@microsemi.com> wrote:

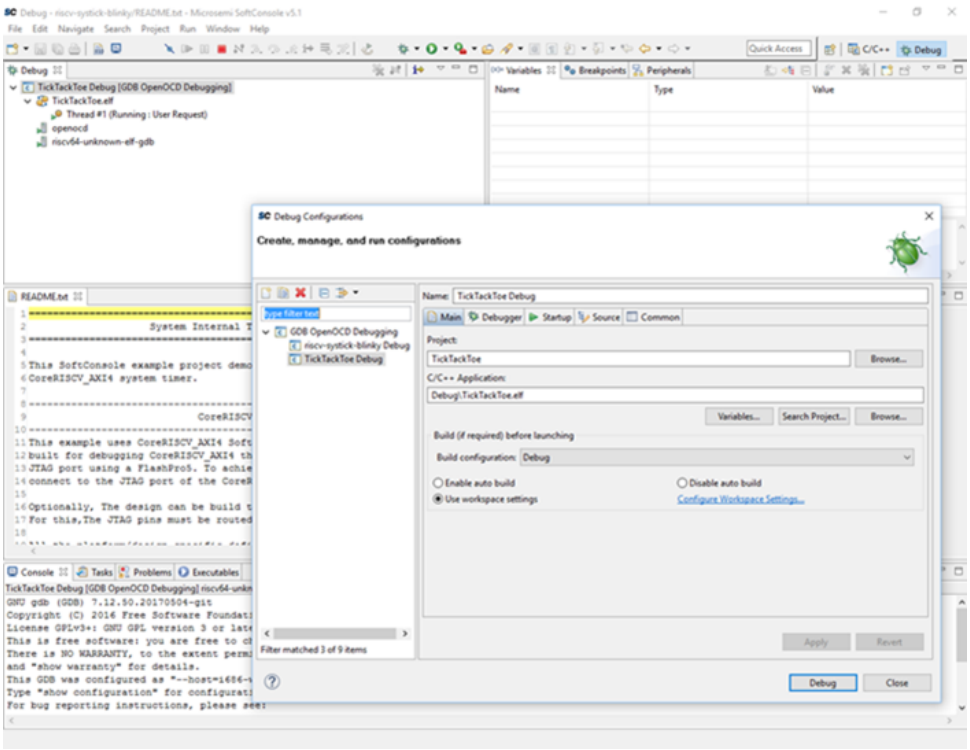
> Hi Michael,
>
> Everything you did seems correct.
>
> I believe this is one of the known issues with SoftConsole v5.1, from the Release Notes:
>
> ## Known Issues
>
> Know issues documented in this section are under active investigation to ascertain the root cause and to resolve the underlying problems with the intention that these are resolved in a future release.
>
> ### Debug launch configuration settings differ for Cortex-M and RISC-V
>
> Be aware that the debug launch configuration settings are different for Cortex-M and RISC-V targets as explained above. The default settings may not automatically match the target CPU. Care must be taken to ensure that the correct configuration settings are applied especially on the Debugger tab. The easiest way to avoid problems is to use the example workspace debug launch configurations as a guide or copy the appropriate one and then customise and specific settings.
>
> Kind Regards,
>
> Ciaran
>
> ---
>
> **From:** Michael John Klopfer [mailto:mklopfer@uci.edu]
> **Sent:** Wednesday, June 21, 2017 8:03 AM
>
> **To:** Ciaran Lappin <ciaran.lappin@microsemi.com>
> **Cc:** Ted Marena <ted.marena@microsemi.com>; Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Cyril Jean <Cyril.Jean@microsemi.com>
> **Subject:** Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

EXTERNAL EMAIL

Hi Ciaran,

Just curious, is the debugger working for the TickTackToe demo in SoftConsole 5.1 you after you imported the project?

The build configurations were present and functional but not the debug configurations. I changed the paths and used the debug configuration for the "riscv-systick-blinky" as a template. After changing paths and using default settings, I was able to get it to work properly and upload the functional program into RAM. Please see image attached. I tried to two different PCs and ran into the same problem from the default project imported with the "git clone" method - the build functioned but there were no debug configurations present. Do you see this same thing on your end?



Best,

--

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On Tue, Jun 20, 2017 at 9:11 AM, Ciaran Lappin <ciaran.lappin@microsemi.com> wrote:

> Hi Michael,
>
> Thanks you a lot of time has gone into them in the past week to get them up to scratch.
>
> I've removed the offending readme, thank you for spotting it. I'll add the link to the documents page first thing in the morning.
>
> Kind Regards,
>
> Ciaran
>
> ---
>
> **From:** Michael John Klopfer [mailto:mklopfer@uci.edu]
> **Sent:** Tuesday, June 20, 2017 4:56 PM
>
> **To:** Ciaran Lappin <ciaran.lappin@microsemi.com>
> **Cc:** Ted Marena <ted.marena@microsemi.com>; Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Cyril Jean <Cyril.Jean@microsemi.com>
> **Subject:** Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture
>
> EXTERNAL EMAIL
>
> Hi Ciaran,
>
> Thank you for the clarification. This looks great! If the structure of the folders is nearing permanence, would you mind placing links to that set of documentation in the project READMEs? This way it is easier to point students to internal help. Also, when time and priorities permit, would you mind removing bits of legacy documentation in the README. For example, the newest Tic-Tac-Toe README is titled "System Internal Timer example project". I am assuming this is the base project this example was developed from. I know this sounds totally trivial.
>
> Please let me know if you want me to beta test workflows or get direct feedback with students. We often do an internal quality control step we call the "sophomoric test" for internally created technical documentation such as app notes. We get a typical EE sophomore with some basic exposure to embedded design but no direct exposure to the task at hand and give them the documentation and all parts and observe how the progress moves forward to completing an assigned project that is supposed to be fully outlined in the documentation. We note sticking points then go back, correct and try again with the same student until the process proceeds smoothly, then we check with a new student if the issue was learning curve or documentation related. This test assesses if someone with technical capability but no specific knowledge on the topic can follow the instructions as written. If not, this typically means the author made assumptions in the instructions that may or may not be non-trivial. We are sometimes really surprised at the tings that cause issues. Sometimes information that is well intended by the author causes students to be mislead down tortured paths. I have done this too many times to students. It is safe to say, if the tested instructions are clear and work for the test students, it is safe to say upperclassmen EE students can follow the instructions with little assistance. This is our model for post graduate beginning engineers as well as an academic undergraduate audience.
>
> Best,

--

Michael J. Klopfer, PhD

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On Tue, Jun 20, 2017 at 7:58 AM, Ciaran Lappin <ciaran.lappin@microsemi.com> wrote:

> Hi Michael,
>
> That's good to hear. I hope to revert back to uploading the workspace as oppose to individual projects soon.
>
> There are two guides in the Documents sections of the Github account, that will form the base of a Getting Started Guide, FlashProExpress_RISCV_Guide_v1 and SoftConsoleV5 0_RISCV_Guide. Please note, the SoftConsole guide is for V5.0 so there may be some differences between v5.0 and v5.1.
>
> Link to documentation: https://github.com/RISCV-on-Microsemi-FPGA/Documentation
>
> Kind Regards,
>
> Ciaran
>
> ---
>
> **From:** Michael John Klopfer [mailto:mklopfer@uci.edu]
> **Sent:** Tuesday, June 20, 2017 3:44 PM
> **To:** Ciaran Lappin <ciaran.lappin@microsemi.com>
> **Cc:** Ted Marena <ted.marena@microsemi.com>; Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Cyril Jean <Cyril.Jean@microsemi.com>
>
> **Subject:** Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture
>
> EXTERNAL EMAIL
>
> Hi Ciaran and Ted,

Thank you for this update! The project opens and builds perfectly (both release and debug for Blinky and tic-tac-toe) when the "git clone" workflow for importing the project is used (from the readme), but for some reason I can not get SoftConsole to register the project when just pointing the active workspace it to the directory from the downloaded project. This was not an issue with the prior version of the M2S025 project version - the projects loaded without a project import. If the workflow is permanently changed, please note this, or others will try the default means of loading and get stuck falsely assuming equivalence. Per prior practice using SC, I also made sure there were no spaces in the project path. I noticed the the "git clone" workflow on my system does not default to a path with no spaces. If this is critical, there may be something to note in documentation for people to avoid. I will test upload and run when I get to a board today.

We teach EE/CSE undergraduate students with the Future Creative board. We see the improving documentation with each code revision, thank you! Continuing and extending this documentation work is really helpful. Most critically this includes just a general top level workflow or description of what is happening - very basic stuff about what the project and how it works at a high level and what the rolse of the tools are in the wokflow to build or modify the project. This also included a basic step by step workflow to bring up the project with notes about what each substantial step does for loading and executing the demo project.

The students we are working with have used the SF2 before, but this is the first time they are getting their feet wet with RISC-V for the SF2/Igloo2. Making sure there is clear instructions (preferably a visual PDF guide) on how to get started for the two sample projects is critical to getting them going comfortably. To hardware engineers, this may be trivial, but to students or beginning engineers on R&D projects, this is absolutely critical. If these conceptual details do not make sense out of the gate to the beginners, they will just give up and go to a competitor's solution with better documentation. I deal with this problem all the time - they seek the path of least resistance to get started because a false assumption is made about the continued steepness of the learning curve.

I would be more than happy to test documentation with students and see how effective they are to get started and understand the basic concepts. The Creative Board and RISC-V are great tools for students. Let me know how I can assist.

Best,

--

Michael J. Klopfer, PhD

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On Tue, Jun 20, 2017 at 6:26 AM, Ciaran Lappin <ciaran.lappin@microsemi.com> wrote:

> Hi Ted,
>
> Please find the latest TickTackToe project for SC v5.1 and SF2 M2S025 in the link below:
>
> https://github.com/RISCV-on-Microsemi-FPGA/M2S025-Creative-Board/tree/master/Example_Software_Projects

Kind Regards,

Ciaran

From: Michael John Klopfer [mailto:mklopfer@uci.edu]
Sent: Tuesday, June 20, 2017 12:59 AM
To: Ted Marena <ted.marena@microsemi.com>
Cc: Farhad Mafie <Farhad.Mafie@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>; G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>; Ciaran Lappin <ciaran.lappin@microsemi.com>; Cyril Jean <Cyril.Jean@microsemi.com>

Subject: Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

EXTERNAL EMAIL

Hi Ted,

This was the example Bronco and I were building from. It was last modified May 3 - this is for the SF2 on the Future Creative board. Goal was testing the blinky and tic-tac-toe example.

https://github.com/RISCV-on-Microsemi-FPGA/M2S025-Creative-Board/tree/master/ExampleSoftware

Best,

--

Michael J. Klopfer, PhD

Technical Director

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On Mon, Jun 19, 2017 at 4:29 PM, Ted Marena <ted.marena@microsemi.com> wrote:

> Hi Michael,

What specific github directory are you having an issue with? We modified the directories for SC 5.1

Ted

From: Michael John Klopfer [mailto:mklopfer@uci.edu]
Sent: Monday, June 19, 2017 4:24 PM
To: Farhad Mafie <Farhad.Mafie@microsemi.com>; Ted Marena <ted.marena@microsemi.com>; Tim Mccarthy <Tim.McCarthy@microsemi.com>
Cc: G. P. Li <gpli@calit2.uci.edu>; Zihan Chen <zihanc3@uci.edu>; Crystal L. Lai <cllai1@uci.edu>
Subject: Re: >>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

EXTERNAL EMAIL

Hi Farhad,

Thank you for letting us know about the release version. We were working with the 5.0 version compiling and testing the demos with everything OK in Linux.

We just tried the Windows release version and are getting project compiling errors. Have you tried building the RISC-V examples successfully from the Microsemi github? Bronco and I tried separately to build the example work-spaces and ran into similar issues with the new Windows release. We are looking into this further to see if it is a just a project path issue or something more.

Best,

--

Michael J. Klopfer, PhD

Technical Director

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On Sat, Jun 17, 2017 at 8:22 PM, G. P. Li <gpli@calit2.uci.edu> wrote:

> Dear Farhad,
>
> Congratulations!!
>
> Have a great weekend.
>
> Regards,
>
> G. P.

From: Farhad Mafie [mailto:Farhad.Mafie@microsemi.com]
Sent: Thursday, June 15, 2017 8:12 AM
To: Michael Klopfer; G. P. Li; Nader Bagherzadeh (UCI); Hemantha K Wickramasinghe (UCI); Mohammad Al Faruque (UCI); Ender Ayanoglu (UCI); Michael M Green (UCI)
Subject: FYI:>>> Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

Microsemi Announces SoftConsole v5.1, the World's First Freely Available Windows-Hosted Eclipse Integrated Development Environment Supporting RISC-V Open Instruction Set Architecture

IDE Supporting All 32-bit RISC-V Implementations to be Presented at 54th Design Automation Conference in Austin, Texas on June 20

ALISO VIEJO, Calif., June 15, 2017 /PRNewswire/ -- **Microsemi Corporation** (Nasdaq: MSCC), a leading provider of semiconductor solutions differentiated by power, security, reliability and performance, today announced the release of its SoftConsole version 5.1, the world's first available Windows-hosted Eclipse integrated development environment (IDE) for designs utilizing RISC-V open instruction set architectures (ISAs) such as RV32I. SoftConsole, Microsemi's free software development environment enabling rapid production of C and C++ programming language designs for its field programmable gate arrays (FPGAs), will be showcased at the Design Automation Conference (DAC) in a presentation highlighting its open architecture, low power and development capabilities using RISC-V soft central processing unit (CPU) cores.

"With the majority of Microsemi FPGA designers utilizing a Windows platform for their development efforts, SoftConsole v5.1 not only supports our RISC-V soft CPU cores to enable designs with our highly secure and reliable FPGAs, but it can also be used for any RV32I standard ISA extensions," said Tim Morin, director of marketing at Microsemi, who will be presenting on the subject at DAC on June 20. "This product release broadens the RISC-V ecosystem for those developing on Windows machines, and leverages our leadership position as we continue investing in this architecture to provide customers dependable, long-term roadmap support."

Microsemi's SoftConsole v5.1, a GNU compiler collection (GCC), now supports both Windows and Linux for RISC-V designs and can be used for RV32I implementations including extensions to the baseline RV32I architecture such as M,A,F,D,G and C. Offering low power and an open architecture, it supports Microsemi's PolarFire™, RTG4™, SmartFusion™2 and IGLOO™2 FPGA-based RISC-V soft CPUs as well as the HiFive1 Arduino kit from SiFive, a fabless semiconductor company that produces computer chips based on the RISC-V ISA. SoftConsole v5.1 is ideal for developing a wide variety of applications within the aerospace and defense, communications, data center and industrial markets.

RISC-V, an ISA which is now a standard open architecture under the governance of the RISC-V Foundation, offers numerous benefits, including enabling the open source community to test and improve cores at a faster pace than closed ISAs. As the RISC-V intellectual property (IP) core is not encrypted, it can be used to ensure trust and certifications not possible with closed architectures. Portability is another benefit of the technology. For example, designers can begin development with Microsemi's RISC-V core in its FPGAs and then move to an application-specific integrated circuit (*ASIC*) royalty-free.

"Rumble Development is excited Microsemi is investing in RISC-V with its IP core and the new version of the SoftConsole IDE," said Michael Aronson, president of Rumble Development, a customer of Microsemi which provides custom logic solutions to original equipment manufacturers (OEMs). "We believe the portability, stability and openness of this ISA combined with Microsemi's ecosystem will enable us to innovate faster and deliver best-in-class solutions."

As a free software development environment supporting quick development of C and C++ executables for Microsemi's FPGAs using RISC-V soft CPU cores, SoftConsole v5.1 provides a flexible and easy-to-use graphical interface for managing embedded software development projects. Customers can quickly develop and debug software programs and implement them in Microsemi FPGAs, with a fully integrated debugger offering easy access to memory contents, registers and single-step execution. SoftConsole also enables users to configure project settings and organize files, provides simultaneous access to multiple tool windows, and delivers the ability to quickly switch editing and debug views. In addition, Libero SoC, Microsemi's comprehensive suite of FPGA design tools, includes the Firmware Catalog to export firmware for soft CPU FPGA designs which can be imported into SoftConsole.

The RISC-V ISA was named Best Technology of 2016 by The Linley Group at its annual Analysts' Choice Awards in January 2017, where its principal analyst Linley Gwennap expressed support of the emerging technology.

"RISC-V is a modern take on the classic RISC instruction set, providing a clean and extensible approach suitable for a broad range of microprocessor implementations. More significantly, the open source, royalty-free RISC-V instruction set creates a new business model for CPU designers," said Gwennap. "This combination has generated sizable industry interest in RISC-V, which will lead to several commercial deployments this year and beyond."

Through Microsemi's early involvement in the creation of the RISC-V Foundation, the company has an established leadership role in the emerging standard and ecosystem and is working closely with the nonprofit to ensure the ISA becomes an industry standard for a wide variety of computing devices. Ted Speers, head of product architecture and planning for Microsemi's SoC business unit, was appointed to the inaugural board of directors of the RISC-V Foundation in July 2016, and Ted Marena, director of SoC FPGA marketing, was elected as vice-chair of the RISC-V Marketing Committee in August 2016.

DAC Presentation on SoftConsole and RISC-V at 1:30 p.m. June 20
Microsemi's new SoftConsole v5.1 will be showcased by Morin in a presentation titled, "RISC-V Tool Chain—An Example Implementation" as part of the RISC-V educational sessions at the DAC in Austin, Texas on Tuesday, June 20 at 1:30 p.m. local time. For more information, visit http://www2.dac.com/events/eventdetails.aspx?id=223-23.

Product Availability
Microsemi's SoftConsole v5.1 is available now. For more information, visit http://www.microsemi.com/products/fpga-soc/soc-processors/risc-v and https://www.microsemi.com/products/fpga-soc/design-resources/design-software/softconsole or contact sales.support@microsemi.com.

About Microsemi's FPGAs
Microsemi's new cost-optimized PolarFire FPGAs deliver the industry's lowest power at mid-range densities with exceptional security and reliability. The product family features 12.7 Gbps SerDes transceivers at up to 50 percent lower power than competing FPGAs. With densities spanning from 100K to 500K logic elements (LEs), the non-volatile PolarFire product family consumes 10 times less static power than competitive devices and features an even lower standby power referred to as Flash*Freeze. The company's IGLOO™2 FPGAs and SmartFusion™2 SoC FPGAs deliver more resources in low density devices, with the lowest power, proven security and exceptional reliability. The devices offer 30-50 percent more power efficiency and are ideal for general purpose functions such as Gigabit Ethernet or dual PCI Express control planes, bridging functions, input/output (I/O) expansion and conversion, video/image processing, system management and secure connectivity. Microsemi's RTG4 FPGAs bring new capabilities to the market and combine a wealth of features with the highest quality and reliability to meet the increasing demands of modern satellite payloads. RTG4's reprogrammable flash technology offers complete immunity to radiation-induced configuration upsets in the harshest radiation environments, without the configuration scrubbing required with SRAM FPGA technology.

About Microsemi
Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

"Safe Harbor" Statement under the Private Securities Litigation Reform Act of 1995: Any statements set forth in this news release that are not entirely historical and factual in nature, including statements related to the release of its SoftConsole version 5.1, the world's first available Windows-hosted Eclipse IDE for designs utilizing RISC-V open ISAs such as RV32I, and its potential effects on future business, are forward-looking statements. These forward-looking statements are based on our current expectations and are inherently subject to risks and uncertainties that could cause actual results to differ materially from those expressed in the forward-looking statements. The potential risks and uncertainties include, but are not limited to, such factors as rapidly changing technology and product obsolescence, potential cost increases, variations in customer order preferences, weakness or competitive pricing environment of the marketplace, uncertain demand for and acceptance of the company's products, adverse circumstances in any of our end markets, results of in-process or planned development or marketing and promotional campaigns, difficulties foreseeing future demand, potential non-realization of expected orders or non-realization of backlog, product returns, product liability, and other potential unexpected business and economic conditions or adverse changes in current or expected industry conditions, difficulties and costs of protecting patents and other proprietary rights, inventory obsolescence and difficulties regarding customer qualification of products. In addition to these factors and any other factors mentioned elsewhere in this news release, the reader should refer as well to the factors, uncertainties or risks identified in the company's most recent Form 10-K and all subsequent Form 10-Q reports filed by Microsemi with the SEC. Additional risk factors may be identified from time to time in Microsemi's future filings. The forward-looking statements included in this release speak only as of the date hereof, and Microsemi does not undertake any obligation to update these forward-looking statements to reflect subsequent events or circumstances.

Regards,

Farhad Mafie

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To view this release online and get more information about Microsemi Investors visit: http://investor.microsemi.com/2017-06-15-Microsemi-Announces-SoftConsole-v5-1-the-Worlds-First-Freely-Available-Windows-Hosted-Eclipse-Integrated-Development-Environment-Supporting-RISC-V-Open-Instruction-Set-Architecture