# PIC18F6627/6722/8627/8722

## 64/80-Pin High-Performance, 1-Mbit Enhanced Flash Microcontrollers with A/D and nanoWatt Technology

### Power Managed Modes:

- Run: CPU on, peripherals on
- Idle: CPU off, peripherals on
- Sleep: CPU off, peripherals off
- Idle mode currents down to 15 µA typical
- Sleep current down to 0.2 µA typical
- Timer1 Oscillator: 1.8 µA, 32 kHz, 2V
- Watchdog Timer: 2.1 µA
- Two-Speed Oscillator Start-up

### Flexible Oscillator Structure:

- Four Crystal modes, up to 25 MHz
- 4x Phase Lock Loop (available for crystal and internal oscillators)
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal oscillator block:
  - 8 user selectable frequencies, from 31 kHz to 8 MHz
  - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
  - User tunable to compensate for frequency drift
- Secondary oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if peripheral clock stops

### External Memory Interface (PIC18F8627/8722 only):

- Address capability of up to 2 Mbytes
- 8-bit or 16-bit interface

### Peripheral Highlights:

- High current sink/source 25 mA/25 mA
- Four programmable external interrupts
- Four input change interrupts
- Two Capture/Compare/PWM (CCP) modules

### Peripheral Highlights (Continued):

- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-Shutdown and Auto-Restart
- Two Master Synchronous Serial Port (MSSP) modules supporting 2/3/4-wire SPI™ (all 4 modes) and $I^2C$™ Master and Slave modes
- Two Enhanced Addressable USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - RS-232 operation using internal oscillator block (no external crystal required)
  - Auto-wake-up on Start bit
  - Auto-baud detect
- 10-bit, up to 16-channel Analog-to-Digital Converter module (A/D)
  - Auto-acquisition capability
  - Conversion available during Sleep
- Dual analog comparators with input multiplexing

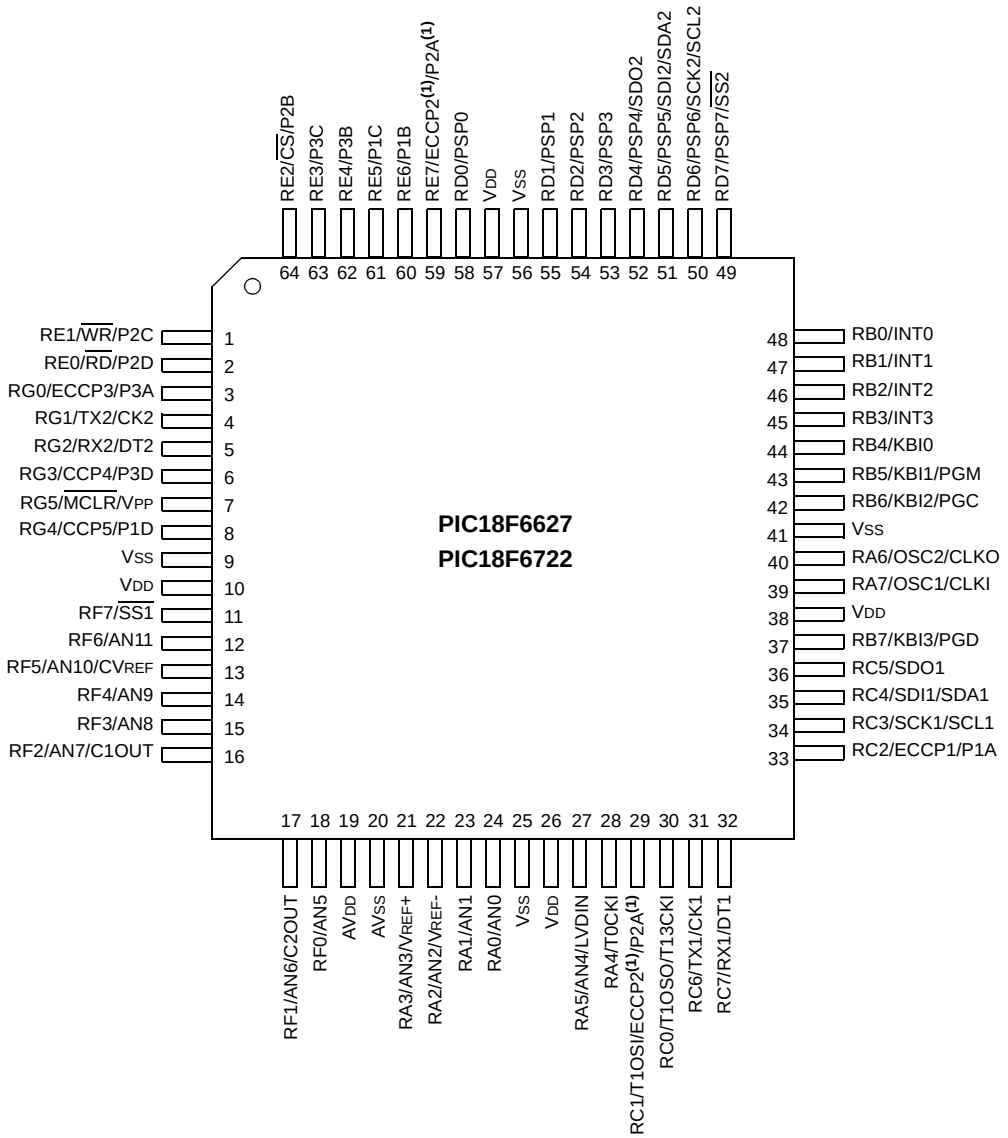
### Special Microcontroller Features:

- C compiler optimized architecture:
  - Optional extended instruction set designed to optimize re-entrant code
- 100,000 erase/write cycle Enhanced Flash program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- Flash/Data EEPROM Retention: 100 years typical
- Self-programmable under software control
- Priority levels for interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) via two pins
- Wide operating voltage range: 2.0V to 5.5V

| Device | Program Memory | | Data Memory | | I/O | 10-bit A/D (ch) | CCP/ ECCP (PWM) | MSSP | | | EUSART | Comparators | Timers 8/16-bit | External Bus |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Flash (bytes) | # Single-Word Instructions | SRAM (bytes) | EEPROM (bytes) | | | | | SPI™ | Master $I^2C$™ | | | | |
| PIC18F6627 | 96K | 49152 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F6722 | 128K | 65536 | 3936 | 1024 | 54 | 12 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | N |
| PIC18F8627 | 96K | 49152 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |
| PIC18F8722 | 128K | 65536 | 3936 | 1024 | 70 | 16 | 2/3 | 2 | Y | Y | 2 | 2 | 2/3 | Y |

## Pin Diagrams

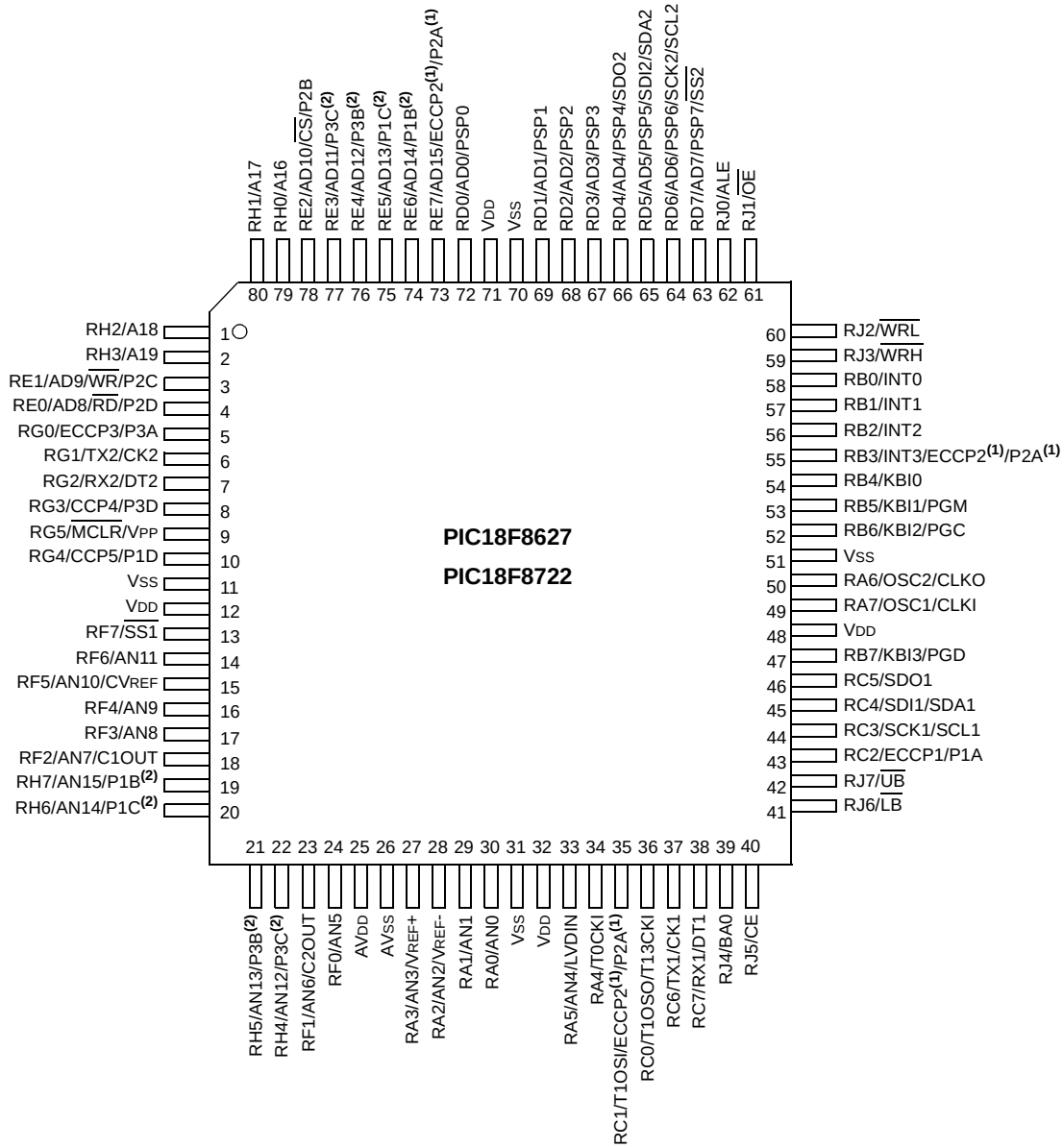
**64-Pin TQFP**




**Note 1:** RB3 is the alternate pin for ECCP2/P2A multiplexing.

## Pin Diagrams (Continued)

**80-Pin TQFP**




**Note 1:** The ECCP2/P2A pin placement is determined by the CCP2MX configuration bit and Processor mode settings.
**2:** P1B, P1C, P3B and P3C pin placement is determined by the ECCPMX configuration bit.

**NOTES:**

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08/24/04

 