Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ROHM GROUP
LAPIS SEMICONDUCTOR

FEDL620Q416A-01
Issue Date: Jan. 5, 2017

ML620Q416A/Q418A

Ultra Low Power 16-bit Microcontroller

■ GENERAL DESCRIPTION

This LSI family is a high-performance 16bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface, supply voltage level detect circuit, RC oscillation type A/D converter, successive approximation type A/D converter, and LCD driver are incorporated around 16bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications. And, this LSI has a writable data flash memory area by the software and a function to re-writing program area from software.
The on-chip debug function that is installed enables program debugging and programming.

■ FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on.
  - Build-in On-Chip debug function
  - Minimum instruction execution time
    30.5 µs (@32.768 kHz system clock)
    62.5ns (@16 MHz system clock)

- Built-in coprocessor for multiplication, division, and multiply-accumulate operations
  - Signed or unsigned operation setting
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Internal memory
  - Supports ISP function (re-writing the program memory area by software)
  - Number of segments

Product name	Flash memory		SRAM
	Program area*	Data area	
ML620Q416A	128KB (64K × 16bit)	4KB (2K × 16bit)	16KB (8K × 16bit)
ML620Q418A	256KB (128K × 16bit)	4KB (2K × 16bit)	16KB (8K × 16bit)

*: including 1KB of unusable test area

- Interrupt controller (INTC)
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 46 maskable interrupt sources (Internal sources: 38, External sources: 8)
  - Software interrupt (SWI): maximum 64 sources
  - External interrupt and comparator allow edge selection and sampling selection
  - Priority level (4-level) can be set for each interrupt

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- Time base counter (TBC)
  – Low-speed time base counter × 1 channel

- 1 kHz Timer
  – 10 Hz / 1 Hz interrupt function

- Timers (TMR)
  – 8 bit × 8 channels
    (Timer0-7: 16bit × 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  – Selection of one shot timer mode is possible
  – External clock can be selected as timer clock.

- Function Timers (FTM)
  – 16bit × 4 channels
  – Equipped with the timer/capture/PWM functions using a 16bit counter
  – An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3)
  – 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
  – Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Real Time Clock (RTC)
  – 3 channels (99 years calendar, alarm, revision of the clock)

- Watchdog timer (WDT)
  – Non-maskable interrupt and reset
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/ SSIO)
  – without FIFOs (SSIO) : 1 channel
  – with 16-byte transmits and receives FIFOs (SSIOF) : 1 channel
  – Master/slave are selectable
  – LSB first/MSB first are selectable
  – Clock polarity (data out at rising edge and data in at falling edge/data out at falling edge and data in at rising edge) selectable
  – 8bit length/16bit length are selectable
  – Initial clock level (High start/Low start) selectable
  – supports slave-select signal (only SSIOF)

- UART (UARTF/ UART)
  – without FIFOs (UART) : 1channel
  – with 16-byte transmits and receives FIFOs (UARTF) : 2channel
  – Full duplex buffer system
  – Communication speed: Settable within the range of 2400bps to 460800bps.
  – Programmable interface (data length, parity, stop bits are selectable)

- I^2C bus interface (I^2CF/ I^2C)
  – without FIFOs(I^2C) :1 channel
  – with 16-byte transmits and receives FIFOs(I^2CF): 2 channel
  – Master/Slave function
  – Fast mode (400 kHz), standard mode (100 kHz)

- General-purpose ports (PORT)
  - Input/output port × 52 channels(including secondary or tertiary or fourthly functions)
  - 8-External interrupt factors selectable with single port or Port Group.

- Melody driver (MELODY)
  - Tempo: 15 types
  - Scale: 29 types (Melody sound frequency: 508 Hz to 10.922 kHz)
  - Tone length: 63 types
  - Buzzer output mode (4 output modes, 8 buzzer frequencies, 7duty levels at 4.096kHz/15 duty levels at other buzzer frequencies)

- RC oscillation type A/D converter (RC-ADC)
  - Time division × 2 channels
  - 24bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2 channels
  - Common mode input voltage: 0.2V to V_{DD} - 0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages: One of 64 levels (1.200V to 3.550V)
  - Accuracy: ±3%
  - Interrupt or Reset generation are slectable
  - Voltage measurement with voltage input pin or VDD pin

- Low Level Detector(LLD)
  - Judgement Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- LCD driver
  - Maximun 2048 dots (64 segment x 32 common)
  - 1/2 to 1/32 duty supported
  - 1/3 or 1/4 or 1/5 bias(built-in bias generation circuit)
  - Frame frequency selectable
  - Bias voltage multiplying clock selectable(8 types)
  - Contrast adjustment(1/3 bias:32steps, 1/4:32steps, 1/5 bias:32steps)
  - 4 operating mode: LCD drive stop, LCD display, all LCDs on, all LCDs off

- Reset
  - Reset by the RESET_N pin input
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by threshold detection in Voltage Level Supervisor(VLS)
  - Reset by low level detection in Low Level Detector(LLD)
  - Reset by the low-speed crystal oscillation stop detection

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    - Crystal oscillation (32.768 kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - PLL (16 MHz) generated from Low-speed clock
    - Built-in RC oscillation (16MHz)

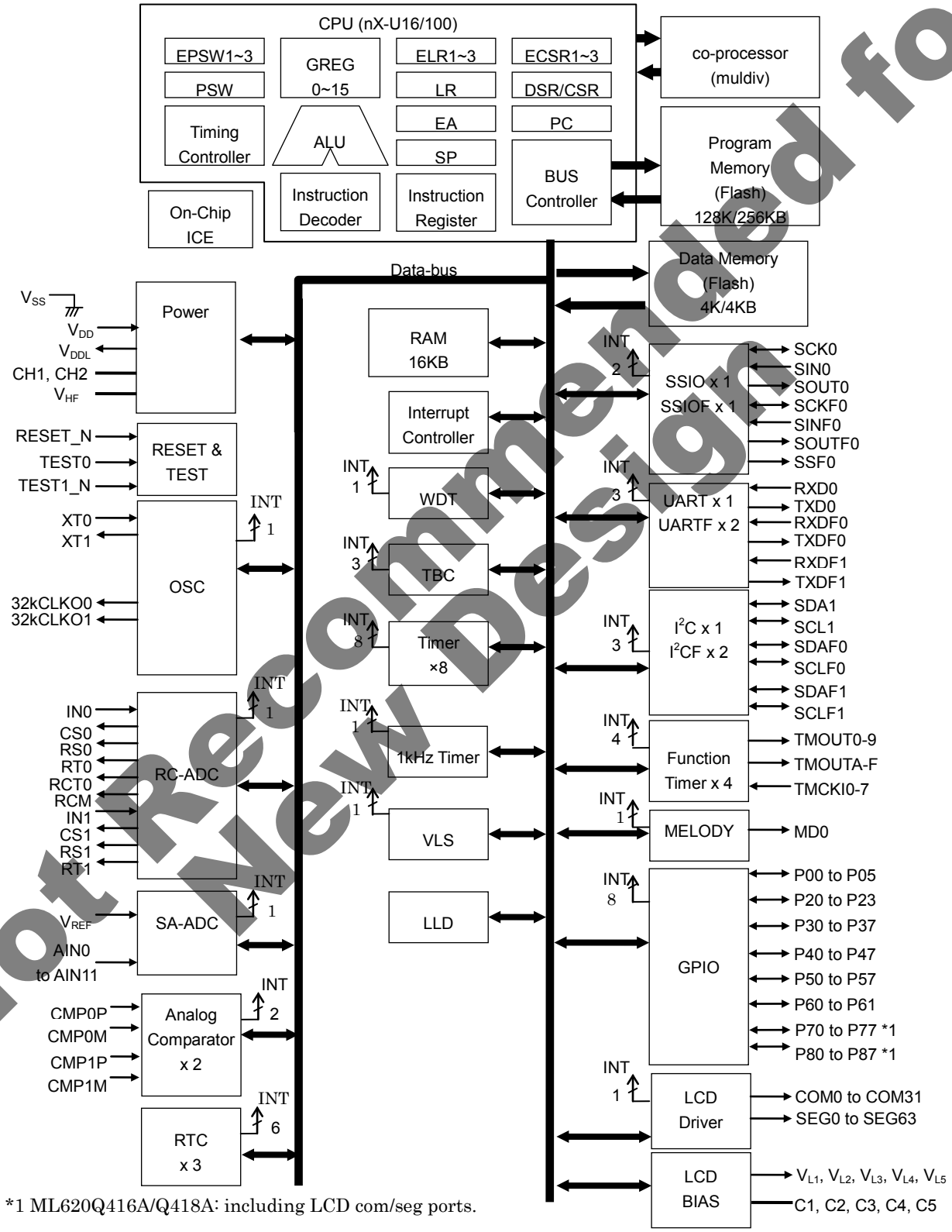
- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states. System returns it in 70µs(Typ.)
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
  - ULTRA-DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states, at VDD>2.5V.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Die *Please contact our responsible sales person for the pad layout information.

- Guaranteed operating range
  - Operating temperature (ambient) : -40°C to +85°C
  - Operating voltage: V_{DD} = 1.8V to 3.6V

■ BLOCK DIAGRAM

Block Diagram of ML620Q416A/Q418A

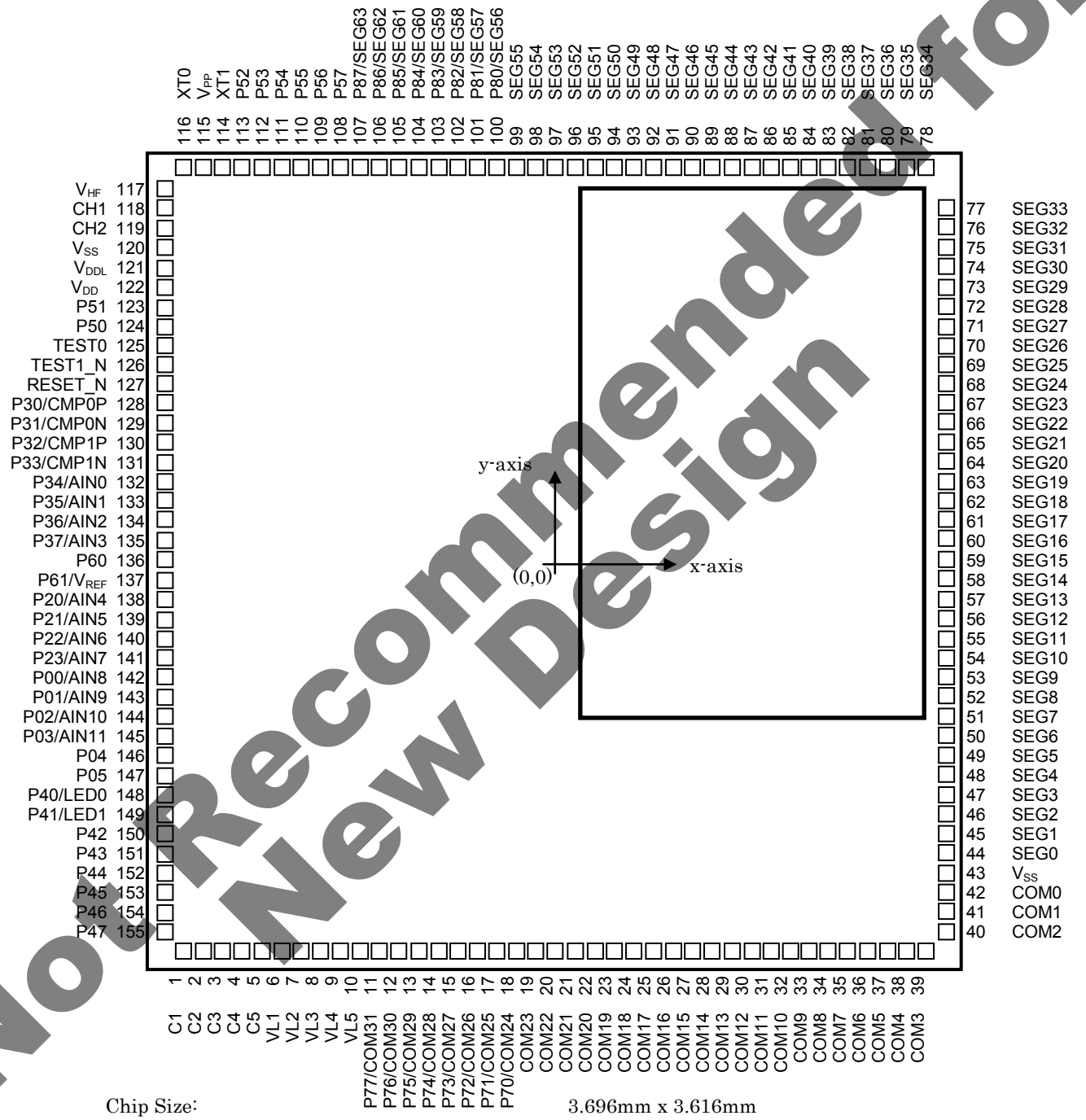


*1 ML620Q416A/Q418A: including LCD com/seg ports.

Figure 1. Block Diagram of ML620Q416A/Q418A

■ PIN CONFIGURATION

Pin Layout of ML620Q416A/Q418A Chip



Chip Size:	3.696mm x 3.616mm
PAD count:	155 pins
Minimum PAD pitch	80um
PAD aperture:	70um x 70um
Chip thickness:	350um
Voltage of the rear side of chip:	Vss level

(Top View)

Figure 2. Pin Layout of ML620Q416A/Q418A

Table 1 Pad Coordinates of ML620Q416A/Q418A (1/2)

Chip Center: X=0, Y=0

Pad No.	Pad Name	X (um)	Y (um)
1	C1	-1520	-1702
2	C2	-1440	-1702
3	C3	-1360	-1702
4	C4	-1280	-1702
5	C5	-1200	-1702
6	VL1	-1120	-1702
7	VL2	-1040	-1702
8	VL3	-960	-1702
9	VL4	-880	-1702
10	VL5	-800	-1702
11	P77/COM31	-720	-1702
12	P76/COM30	-640	-1702
13	P75/COM29	-560	-1702
14	P74/COM28	-480	-1702
15	P73/COM27	-400	-1702
16	P72/COM26	-320	-1702
17	P71/COM25	-240	-1702
18	P70/COM24	-160	-1702
19	COM23	-80	-1702
20	COM22	0	-1702
21	COM21	80	-1702
22	COM20	160	-1702
23	COM19	240	-1702
24	COM18	320	-1702
25	COM17	400	-1702
26	COM16	480	-1702
27	COM15	560	-1702
28	COM14	640	-1702
29	COM13	720	-1702
30	COM12	800	-1702
31	COM11	880	-1702
32	COM10	960	-1702
33	COM9	1040	-1702
34	COM8	1120	-1702
35	COM7	1200	-1702
36	COM6	1280	-1702
37	COM5	1360	-1702
38	COM4	1440	-1702
39	COM3	1520	-1702
40	COM2	1742	-1480
41	COM1	1742	-1400
42	COM0	1742	-1320
43	V_{SS}	1742	-1240
44	SEG0	1742	-1160
45	SEG1	1742	-1080
46	SEG2	1742	-1000
47	SEG3	1742	-920
48	SEG4	1742	-840
49	SEG5	1742	-760
50	SEG6	1742	-680
51	SEG7	1742	-600
52	SEG8	1742	-520
53	SEG9	1742	-440
54	SEG10	1742	-360
55	SEG11	1742	-280
56	SEG12	1742	-200
57	SEG13	1742	-120
58	SEG14	1742	-40
59	SEG15	1742	40
60	SEG16	1742	120
61	SEG17	1742	200
62	SEG18	1742	280
63	SEG19	1742	360
64	SEG20	1742	440
65	SEG21	1742	520
66	SEG22	1742	600
67	SEG23	1742	680
68	SEG24	1742	760
69	SEG25	1742	840
70	SEG26	1742	920
71	SEG27	1742	1000
72	SEG28	1742	1080
73	SEG29	1742	1160
74	SEG30	1742	1240
75	SEG31	1742	1320
76	SEG32	1742	1400
77	SEG33	1742	1480

Table 2 Pad Coordinates of ML620Q416A/Q418A (2/2)

Chip Center: X=0, Y=0

Pad No.	Pad Name	X (um)	Y (um)
78	SEG34	1520	1702
79	SEG35	1440	1702
80	SEG36	1360	1702
81	SEG37	1280	1702
82	SEG38	1200	1702
83	SEG39	1120	1702
84	SEG40	1040	1702
85	SEG41	960	1702
86	SEG42	880	1702
87	SEG43	800	1702
88	SEG44	720	1702
89	SEG45	640	1702
90	SEG46	560	1702
91	SEG47	480	1702
92	SEG48	400	1702
93	SEG49	320	1702
94	SEG50	240	1702
95	SEG51	160	1702
96	SEG52	80	1702
97	SEG53	0	1702
98	SEG54	-80	1702
99	SEG55	-160	1702
100	P80/SEG56	-240	1702
101	P81/SEG57	-320	1702
102	P82/SEG58	-400	1702
103	P83/SEG59	-480	1702
104	P84/SEG60	-560	1702
105	P85/SEG61	-640	1702
106	P86/SEG62	-720	1702
107	P87/SEG63	-800	1702
108	P57/TMCKI7	-880	1702
109	P56/TMCKI6	-960	1702
110	P55	-1040	1702
111	P54	-1120	1702
112	P53/TMCKI5	-1200	1702
113	P52/TMCKI4	-1280	1702
114	XT1	-1360	1702
115	V_{PP}	-1440	1702
116	XT0	-1520	1702

Pad No.	Pad Name	X (um)	Y (um)
117	V_{HF}	-1742	1560
118	CH1	-1742	1480
119	CH2	-1742	1400
120	V_{SS}	-1742	1320
121	V_{DDL}	-1742	1240
122	V_{DD}	-1742	1160
123	P51	-1742	1080
124	P50/V_{LSP}	-1742	1000
125	TEST0	-1742	920
126	TEST1_N	-1742	840
127	RESET_N	-1742	760
128	P30/CMP0P	-1742	680
129	P31/CMP0N	-1742	600
130	P32/CMP1P	-1742	520
131	P33/CMP1N	-1742	440
132	P34/AIN0	-1742	360
133	P35/AIN1	-1742	280
134	P36/AIN2	-1742	200
135	P37/AIN3	-1742	120
136	P60	-1742	40
137	P61/V_{REF}	-1742	-40
138	P20/AIN4	-1742	-120
139	P21/AIN5	-1742	-200
140	P22/AIN6	-1742	-280
141	P23/AIN7	-1742	-360
142	P00/AIN8	-1742	-440
143	P01/AIN9	-1742	-520
144	P02/AIN10	-1742	-600
145	P03/AIN11	-1742	-680
146	P04	-1742	-760
147	P05	-1742	-840
148	P40/LED0	-1742	-920
149	P41/LED1	-1742	-1000
150	P42/TMCKI0	-1742	-1080
151	P43/TMCKI1	-1742	-1160
152	P44	-1742	-1240
153	P45	-1742	-1320
154	P46/TMCKI2	-1742	-1400
155	P47/TMCKI3	-1742	-1480

■ PIN LIST

PIN No.	.Reset State	Primary Function		Secondary Function		Tertiary Function		Quaternary Function		Quinary Function	
		Pin name	I/O	Pin name	I/O	pin name	I/O	pin name	I/O	pin name	I/O
43 120	–	V_{SS}	–	–	–	–	–	–	–	–	–
122	–	V_{DD}	–	–	–	–	–	–	–	–	–
121	–	V_{DDL}	–	–	–	–	–	–	–	–	–
117	–	V_{HF}	–	–	–	–	–	–	–	–	–
116	–	XT0	–	–	–	–	–	–	–	–	–
114	–	XT1	–	–	–	–	–	–	–	–	–
127	Pull-up Input	RESET_N	I	–	–	–	–	–	–	–	–
126	Pull-up Input	TEST1_N	I	–	–	–	–	–	–	–	–
125	Pull-down Input	TEST0	I/O	–	–	–	–	–	–	–	–
142	Hi-Z output	P00/ EXI00/ AIN8	I/O	IN0	I	SOUT0	O	RXDF0	I	–	–
143	Hi-Z output	P01/ EXI01/ AIN9	I/O	CS0	O	SIN0	I	TXDF0	O	–	–
144	Hi-Z output	P02/ EXI02/ AIN10	I/O	RCT0	O	SCK0	I/O	TMOUT0	O	–	–
145	Hi-Z output	P03/ EXI03/ AIN11	I/O	RS0	O	–	–	TMOUT1	O	–	–
146	Hi-Z output	P04/ EXI04	I/O	RT0	O	–	–	–	–	–	–
147	Hi-Z output	P05/ EXI05	I/O	RCM	O	–	–	–	–	–	–
138	Hi-Z output	P20/ EXI20/ AIN4	I/O	IN1	I	SOUTF0	O	RXDF1	I	–	–
139	Hi-Z output	P21/ EXI21/ AIN5	I/O	CS1	O	SINF0	I	TXDF1	O	–	–
140	Hi-Z output	P22/ EXI22/ AIN6	I/O	RS1	O	SCKF0	I/O	TMOUT2	O	–	–
141	Hi-Z output	P23/ EXI23/ AIN7	I/O	RT1	O	SSF0	I/O	TMOUT3	O	–	–
128	Hi-Z output	P30/ EXI30/ CMP0P	I/O	SDAF0	I/O	SOUT0	O	RXDF0	I	RXD0	I
129	Hi-Z output	P31/ EXI31/ CMP0M	I/O	SCLF0	O	SIN0	I	TXDF0	O	TXD0	O
130	Hi-Z output	P32/ EXI32/ CMP1P	I/O	–	–	SCK0	I/O	TMOUT4	O	–	–
131	Hi-Z output	P33/ EXI33/ CMP1M	I/O	32kCLKO	O	MD0	O	TMOUT5	O	–	–
132	Hi-Z output	P34/ EXI34/ AIN0	I/O	SDAF1	I/O	SOUTF0	O	RXDF1	I	SDA1	I/O
133	Hi-Z output	P35/ EXI35/ AIN1	I/O	SCLF1	I/O	SINF0	I	TXDF1	O	SCL1	I/O
134	Hi-Z output	P36/ EXI36/ AIN2	I/O	–	–	SCKF0	I/O	TMOUT6	O	–	–
135	Hi-Z output	P37/ EXI37/ AIN3	I/O	32kCLKO	O	SSF0	I/O	TMOUT7	O	–	–
148	Hi-Z output	P40/ EXI40/ LED	I/O	SDAF0	I/O	SOUT0	O	RXDF0	I	–	–
149	Hi-Z output	P41/ EXI41/ LED	I/O	SCLF0	O	SIN0	I	TXDF0	O	–	–
150	Hi-Z output	P42/ EXI42/ TMCKI0	I/O	–	–	SCK0	I/O	TMOUT8	O	–	–
151	Hi-Z output	P43/ EXI43/ TMCKI1	I/O	32kCLKO	O	MD0	O	TMOUT9	O	–	–
152	Hi-Z output	P44/ EXI44	I/O	SDAF1	I/O	SOUTF0	O	RXDF1	I	–	–

PIN No.	.Reset State	Primary Function		Secondary Function		Tertiary Function		Quaternary Function		Quinary Function	
		Pin name	I/O	Pin name	I/O	pin name	I/O	pin name	I/O	pin name	I/O
153	Hi-Z output	P45/ EXI45	I/O	SCLF1	O	SINF0	I	TXDF1	O	–	–
154	Hi-Z output	P46/ EXI46/ TMCKI2	I/O	–	–	SCKF0	I/O	TMOUTA	O	–	–
155	Hi-Z output	P47/ EXI47/ TMCKI3	I/O	32kCLKO	O	SSF0	I/O	TMOUTB	O	–	–
124	Hi-Z output	P50/ EXI50 VLSP	I/O	SDAF0	I/O	SOUT0	O	RXDF0	I	RXD0	I
123	Hi-Z output	P51/ EXI51	I/O	SCLF0	O	SIN0	I	TXDF0	O	TXD0	O
113	Hi-Z output	P52/ EXI52/ TMCKI4/ LED	I/O	–	–	SCK0	I/O	TMOUTC	O	–	–
112	Hi-Z output	P53/ EXI53/ TMCKI5/ LED	I/O	32kCLKO	O	MD0	O	TMOUTD	O	–	–
111	Hi-Z output	P54/ EXI54	I/O	SDAF1	I/O	SOUTF0	O	RXDF1	I	SDA1	I/O
110	Hi-Z output	P55/ EXI55	I/O	SCLF1	O	SINF0	I	TXDF1	O	SCL1	I/O
109	Hi-Z output	P56/ EXI56/ TMCKI6	I/O	–	–	SCKF0	I/O	TMOUTE	O	–	–
108	Hi-Z output	P57/ EXI57/ TMCKI7	I/O	32kCLKO	O	SSF0	I/O	TMOUTF	O	–	–
136	Hi-Z output	P60/ EXI60	I/O	SDAF0	I/O	–	–	RXDF0	I	–	–
137	Hi-Z output	P61/ EXI61/ V_{REF}	I/O	SCLF0	I/O	–	–	TXDF0	O	–	–
19 to 42	Low Level Output	COM0 to COM23	O	–	–	–	–	–	–	–	–
18	Pull-down Input	P70/ EXI70	I/O	COM24	O	–	–	–	–	–	–
17	Pull-down Input	P71/ EXI71	I/O	COM25	O	–	–	–	–	–	–
16	Pull-down Input	P72/ EXI72	I/O	COM26	O	–	–	–	–	–	–
15	Pull-down Input	P73/ EXI73	I/O	COM27	O	–	–	–	–	–	–
14	Pull-down Input	P74/ EXI74	I/O	COM28	O	–	–	–	–	–	–
13	Pull-down Input	P75/ EXI75	I/O	COM29	O	–	–	–	–	–	–
12	Pull-down Input	P76/ EXI76	I/O	COM30	O	–	–	–	–	–	–
11	Pull-down Input	P77/ EXI77	I/O	COM31	O	–	–	–	–	–	–
44 to 99	Low Level Output	SEG0 to SEG55	O	–	–	–	–	–	–	–	–
100	Pull-down Input	P80/ EXI80	I/O	SEG56	O	–	–	–	–	–	–
101	Pull-down Input	P81/ EXI81	I/O	SEG57	O	–	–	–	–	–	–
102	Pull-down Input	P82/ EXI82	I/O	SEG58	O	–	–	–	–	–	–
103	Pull-down Input	P83/ EXI83	I/O	SEG59	O	–	–	–	–	–	–
104	Pull-down Input	P84/ EXI84	I/O	SEG60	O	–	–	–	–	–	–
105	Pull-down Input	P85/ EXI85	I/O	SEG61	O	–	–	–	–	–	–
106	Pull-down Input	P86/ EXI86	I/O	SEG62	O	–	–	–	–	–	–
107	Pull-down Input	P87/ EXI87	I/O	SEG63	O	–	–	–	–	–	–
6 to 10	–	VL1 to VL5	–	–	–	–	–	–	–	–	–
1 to 5	–	C1 to C5	–	–	–	–	–	–	–	–	–
118 to 119	–	CH1 to CH2	–	–	–	–	–	–	–	–	–

■ PIN DESCRIPTION

In the table below indicates the functional pin description.
The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quaternary function, 5th:quinary function)

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
System					
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	RESET_N	–	L
XT0	I	Crystal connection pin for low-speed clock.	XT0	–	–
XT1	O	Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	XT1	–	–
General-purpose input/output port					
P00-P05	I/O	General-purpose input/output port.	P00-P05	1st	–
P20-P23	I/O	General-purpose input/output port.	P20-P23	1st	–
P30-P37	I/O	General-purpose input/output port.	P30-P37	1st	–
P40-P47	I/O	General-purpose input/output port.	P40-P47	1st	–
P50-P57	I/O	General-purpose input/output port.	P50-P57	1st	–
P60-P61	I/O	General-purpose input/output port.	P60-P61	1st	–
P70-P77	I/O	General-purpose input/output port.	P70/COM24-P77/COM31	1st	–
P80-P87	I/O	General-purpose input/output port.	P80/SEG56-P87/SEG63	1st	–
External interrupt					
EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57 EXI60-61 EXI70-77 EXI80-87	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software.	P00-P05 P20-P23 P30-P37 P40-P47 P50-P57 P60-P61 P70/COM24-P77/COM31 P80/SEG56-P87/SEG63	1st	H/L
LED					
LED	O	N-channel open drain output pins to drive LED.	P40,P41,P52,P53	1st	–
Melody/Buzzer					
MD0	O	Melody/buzzer signal output pin.	P33,P43,P53	3rd	H

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
UART					
TXD1	O	UART data output pin.	P31,P51	5th	–
RXD1	I	UART data input pin.	P30,P50	5th	
TXDF0	O	UART with FIFO data output pin.	P01,P31,P41,P51, P61	4th	
RXDF0	I	UART with FIFO data input pin.	P00,P30,P40,P50, P60	4th	
TXDF1	O	UART with FIFO data output pin.	P21,P35,P45,P55	4th	–
RXDF1	I	UART with FIFO data input pin.	P20,P34,P44,P54	4th	–
I^2C bus interface					
SDA1	I/O	I^2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P34,P54	5th	–
SCL1	O	I^2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P35,P55	5th	–
SDAF0	I/O	I^2C0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P30,P40,P50	2nd	
SCLF0	O	I^2C0 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P31,P41,P51	2nd	
SDAF1	I/O	I^2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P34,P44,P54	2nd	–
SCLF1	O	I^2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P35,P45,P55	2nd	–
Synchronous serial					
SCK0	I/O	Synchronous serial(SSIO) clock input/output pin.	P02,P32,P42,P52	3rd	–
SIN0	I	Synchronous serial(SSIO) data input pin.	P01,P31,P41,P51	3rd	–
SOUT0	O	Synchronous serial(SSIO) data output pin.	P00,P30,P40,P50	3rd	–
SCKF0	I/O	Synchronous serial with FIFO(SSIOF) clock input/output pin.	P22,P36,P46,P56	3rd	–
SINF0	I	Synchronous serial with FIFO(SSIOF) data input pin.	P21,P35,P45,P55	3rd	–
SOUTF0	O	Synchronous serial with FIFO(SSIOF) data output pin.	P20,P34,P44,P54	3rd	–
SSF0	I/O	Synchronous serial with FIFO(SSIOF) select input/output pin.	P23,P37,P47,P57	3rd	L
FTM					
TMOUT0-9 TMOUTA-F	O	FTM output pin.	P02,P03,P22,P23 P32,P33,P36,P37 P42,P43,P46,P47 P52,P53,P56,P57	4th	–
TMCKI0-7	I	External clock input pin for FTM.	P42,P43,P46,P47 P52,P53,P56,P57	1st	–

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
RC oscillation type A/D converter					
IN0	I	Oscillation input pin of Channel 0.	P00	2nd	–
CS0	O	Reference capacitor connection pin of Channel 0.	P01	2nd	–
RS0	O	Reference resistor connection pin of Channel 0.	P03	2nd	–
RT0	O	Resistor sensor connection pin for measurement of Channel 0.	P04	2nd	–
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement.	P02	2nd	–
RCM	O	RC oscillation monitor pin.	P05	2nd	–
IN1	I	Oscillation input pin of Channel 1.	P20	2nd	–
CS1	O	Reference capacitor connection pin of Channel 1.	P21	2nd	–
RS1	O	Reference resistor connection pin of Channel 1.	P22	2nd	–
RT1	O	Resistor sensor connection pin for measurement of Channel 1.	P23	2nd	–
Successive approximation type A/D converter					
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	P61	–	–
AIN0-11	I	Analog input for successive approximation type A/D converter.	(AIN0-3) P34-37, (AIN4-7) P20-23, (AIN8-11) P00-03	1st	–
Analog comparator					
CMP0P	I	Comparator0 Non-inverted input pin.	P30	1st	–
CMP0M	I	Comparator0 Inverted input pin.	P31	1st	–
CMP1P	I	Comparator1 Non-inverted input pin.	P32	1st	–
CMP1M	I	Comparator1 Inverted input pin.	P33	1st	–
For testing					
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	TEST0	–	–
TEST1_N	I	Input pin for testing. A pull-up resistor is internally connected.	TEST1_N	–	–
Power supply					
V_{SS}	–	Negative power supply pin.	V_{SS}	–	–
V_{DD}	–	Positive power supply pin.	V_{DD}	–	–
V_{DDL}	–	Positive power supply pin (internally generated) for internal logic. Capacitors C_L is connected between this pin and V_{SS}.	V_{DDL}	–	–
V_{HF}	–	Positive power supply pin (internally generated) for built-in halver circuit. Capacitor C_{VH} is connected between this pin and V_{SS}.	V_{HF}	–	–
C_{H1} – C_{H2}	–	Capacitor pins of built-in halver circuit	C_{H1} – C_{H2}	–	–
LCD driver					
COM0 – COM31	–	Common pins of LCD driver	COM0 – COM23, P70/COM24- P77/COM31	1st & 2nd	–
SEG0 – SEG63	–	Segment pins of LCD driver	SEG0 – SEG55 P80/SEG56- P87/SEG63	1st & 2nd	–
C1 – C5	–	Capacitor pins of built-in generation bias circuit	C1 – C5	–	–
V_{L1} – V_{L5}	–	Reference voltage input pins of built-in bias generation circuit	V_{L1} – V_{L5}	–	–

■ TERMINATION OF UNUSED PINS

Table 1 shows methods of terminating the unused pins.

Table3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	open
TEST0	open
TEST1_N	open
P00 to P05	open
P20 to P23	open
P30 to P37	open
P40 to P47	open
P50 to P57	open
P60 to P61	open
P70 to P77	open
P80 to P87	open

[Note]
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

■ ELECTRIC CHARACTERISTICS

● ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 3	V_{L1-5}	Ta=25°C	-0.3 to +7.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage 1	V_{OUT1}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage 2 (COM0 to COM31 SEG0 to SEG63)	V_{OUT2}	Ta=25°C	-0.3 to V_{L1-5}+0.3	V
Output current 1 (Port0, 2)	I_{OUT1}	Ta=25°C	-12 to +11	mA
Output current 2 (Port3 to 8)	I_{OUT2}	Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	–	-55 to +150	°C

● RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	–	-40 to +85	°C
Operating voltage	V_{DD}	–	1.8 to 3.6	V
Reference voltage	V_{REF}	–	1.8 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	–	LSCLK:32.768k HSCLK:500k to	Hz
Low speed crystal oscillation frequency	f_{XTL}	–	32.768k	Hz
Low speed crystal oscillation external capacitor 1	C_{DL}	Using VT-200-FL(from SII)	6.8 to 12	pF
	C_{GL}		6.8 to 12	
Low speed crystal oscillation external capacitor 2	C_{DL}	Using DT-26(from Daishinku)	12 to 16	pF
	C_{GL}		12 to 16	
Low speed crystal *1 oscillation external capacitor 3	C_{DL}	Using VT-200-F(from SII)	12 to 22	pF
	C_{GL}		12 to 22	
V_{DDL} external capacitor *2	C_L	ESR ≦500mΩ	2.2 ± 30%	µF
VL1,2,3,4,5 pin external capacitor	$C_{a,b,c,d,e}$	–	1 ± 30%	µF
C1-C2, C2-C3, C4-C5 external capacitor	C_{12},C_{23} ,C_{45}	–	1 ± 30%	µF
CH1, CH2 external capacitor	C_{H12}	–	1 ± 30%	µF
V_{HF} external capacitor	C_{VH}	–	1 ± 30%	µF

*1 : Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal. Please evaluate the matching when other crystal oscillator/ceramic oscillator is used.

*2 : Please evaluate on user's conditions, put on C_{L0}(= 0.1uF) if necessary.

● Operating Conditions of Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature (Ambience)	T_{OP}	Data area : write/erase		-40 to +85	°C
		Program area : write/erase		0 to +40	°C
Operating voltage Write time	V_{DD}	Write/erase		1.8 to 3.6	V
	C_{EPD}	Data area (1,024B x 4)		10,000	times
	C_{EPP}	Program area		1000	times
Erase unit	–	Block erase	Program area	8	KB
			Data area	4	
		Sector erase		1	
Erase time(Maximum)	–	Block erase/Sector erase		100	ms
Write unit	–	–		1 word (2 byte)	–

● Operating Conditions of LCD

(V_{SS}= 0V)

Parameter	Symbol	Condition	Range	Unit
Operating voltage	V_{DD}	V_{L1} based	1.8 to 3.6	V
		V_{L2} based	2.5 to 3.6	
	V_{L1}	V_{L1}（External input）based	0.84 to 1.31	
	V_{L2}	V_{L2}（External input）based	1.68 to 2.61	

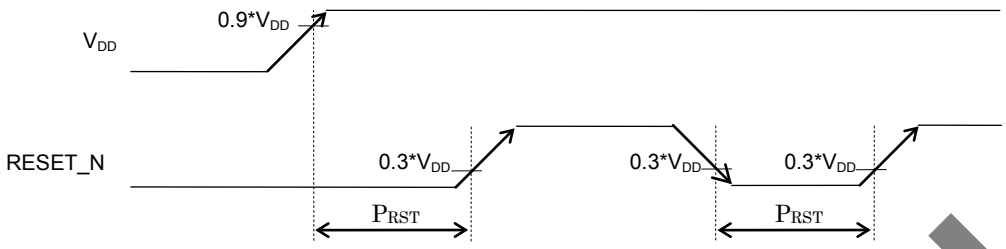
LMD1-0 of the DSPCON0 register are bits to select an LCD display mode.

● AC characteristics (Oscillation, reset)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low speed crystal oscillation start time	T_{XTL}	–	–	–	2	s	
Low speed built-in RC oscillation frequency *1*2*3	f_{LCR}	Ta=25°C	typ -1.5%	32.768	typ +1.5%	kHz	
		Ta=-40 to 85°C	typ -5%	32.768	typ +5%		
High speed build-in RC oscillation frequency *1*2	f_{HCR}	Ta=25°C	typ -1%	16	typ +1%	MHz	
		Ta=-40 to 85°C	typ -5%	16	typ +5%		
PLL frequency	f_{PLL}	f_{XTL}=32.768kHz	typ -5%	16	typ +5%	MHz	1
System return time from HALT-H	T_{HCR}	–	–	70	100	µs	
Low speed crystal oscillation stop detection time	T_{STOP}	–	–	600	–	µs	
Reset pulse width	P_{RST}	–	200	–	–	µs	
Reset noise elimination pulse width	P_{NRST}	–	–	–	0.3	µs	
Power-on reset activation power rise time	T_{POR}	–	–	–	10	ms	

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.
*3 : Except DeepHALT mode and Ultra-DeepHALT mode.



External reset sequence

Power on reset sequence

● DC Characteristics (IDD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating *1 Min.	Rating *1 Typ.	Rating *1 Max.	Unit	Measuring circuit
Power consumption 1	IDD1	CPU is Stopped Low/High-speed oscillation is stopped	Ta=25°C	–	0.3	1.2	µA	1
			Ta=-40 to 85°C	–	–	18		
Power consumption 2	IDD2-1	ULTRA-DEEP-HALT mode *3*4 (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped. 2.5V≦V_{DD}	Ta=25°C	–	0.38	2	µA	
			Ta=-40 to 85°C	–	–	20		
	IDD2-2	DEEP-HALT mode *3*4 (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped.	Ta=25°C	–	0.7	3	µA	
			Ta=-40 to 85°C	–	–	22		
Power consumption 3	IDD3	HALT mode *3*4 (LTBC function) Low-speed crystal oscillating (32.768kHz) High speed oscillation is stopped.	Ta=25°C	–	2	5	µA	
			Ta=-40 to 85°C	–	–	27		
Power consumption 4	IDD4	CPU Low-speed *2*4 Low-speed built-in RC oscillating High speed oscillation is stopped.	Ta=25°C	–	12	20	µA	
			Ta=-40 to 85°C	–	–	45		
Power consumption 5	IDD5	CPU High-speed(16MHz) *2*4 High-speed Built-in RC oscillating	Ta=25°C	–	4.3	5.5	mA	
			Ta=-40 to 85°C	–	–	6		

*1 : typ.rating is V_{DD}=3.0V

*2 : at CPU activity rate =100%（No HALT state）

*3 : using 32.768KHz crystal oscillator VT-200-FL (from SII)(C_{GL}/C_{DL}＝12pF)
using 32.768KHz crystal oscillator DT-26(from Daishinku)(C_{GL}/C_{DL}＝12pF）

*4 : BLKCON0~BLKCON5 valid bits are all “1”.

● DC Characteristics (VLS) (1/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	VLSLV5-0 = 00H*1	Typ. +3%	1.200	Typ. +3%	V	1
		VLSLV5-0 = 01H*1		1.225			
		VLSLV5-0 = 02H*1		1.250			
		VLSLV5-0 = 03H*1		1.275			
		VLSLV5-0 = 04H*1		1.300			
		VLSLV5-0 = 05H*1		1.325			
		VLSLV5-0 = 06H*1		1.350			
		VLSLV5-0 = 07H*1		1.375			
		VLSLV5-0 = 08H*1		1.400			
		VLSLV5-0 = 09H*1		1.425			
		VLSLV5-0 = 0AH*1		1.450			
		VLSLV5-0 = 0BH*1		1.475			
		VLSLV5-0 = 0CH*1		1.500			
		VLSLV5-0 = 0DH*1		1.525			
		VLSLV5-0 = 0EH*1		1.550			
		VLSLV5-0 = 0FH*1		1.575			
		VLSLV5-0 = 10H*1		1.600			
		VLSLV5-0 = 11H*1		1.625			
		VLSLV5-0 = 12H*1		1.650			
		VLSLV5-0 = 13H*1		1.675			
		VLSLV5-0 = 14H*1		1.700			
		VLSLV5-0 = 15H*1		1.725			
		VLSLV5-0 = 16H*1		1.750			
		VLSLV5-0 = 17H*1		1.775			
		VLSLV5-0 = 18H		1.800			
		VLSLV5-0 = 19H		1.825			
		VLSLV5-0 = 1AH		1.850			
		VLSLV5-0 = 1BH		1.875			
		VLSLV5-0 = 1CH		1.900			
		VLSLV5-0 = 1DH		1.925			
		VLSLV5-0 = 1EH		1.950			
		VLSLV5-0 = 1FH		1.975			
		VLSLV5-0 = 20H		2.000			
		VLSLV5-0 = 21H		2.050			
		VLSLV5-0 = 22H		2.100			
		VLSLV5-0 = 23H		2.150			
		VLSLV5-0 = 24H		2.200			
		VLSLV5-0 = 25H		2.250			
		VLSLV5-0 = 26H		2.300			
		VLSLV5-0 = 27H		2.350			
		VLSLV5-0 = 28H		2.400			
		VLSLV5-0 = 29H		2.450			

● DC Characteristics (VLS) (2/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating[*1]			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	VLSLV5-0 = 2AH	Typ. -3%	2.500	Typ. +3%	V	1
		VLSLV5-0 = 2BH		2.550			
		VLSLV5-0 = 2CH		2.600			
		VLSLV5-0 = 2DH		2.650			
		VLSLV5-0 = 2EH		2.700			
		VLSLV5-0 = 2FH		2.750			
		VLSLV5-0 = 30H		2.800			
		VLSLV5-0 = 31H		2.850			
		VLSLV5-0 = 32H		2.900			
		VLSLV5-0 = 33H		2.950			
		VLSLV5-0 = 34H		3.000			
		VLSLV5-0 = 35H		3.050			
		VLSLV5-0 = 36H		3.100			
		VLSLV5-0 = 37H		3.150			
		VLSLV5-0 = 38H		3.200			
		VLSLV5-0 = 39H		3.250			
		VLSLV5-0 = 3AH		3.300			
		VLSLV5-0 = 3BH		3.350			
		VLSLV5-0 = 3CH		3.400			
		VLSLV5-0 = 3DH		3.450			
		VLSLV5-0 = 3EH		3.500			
		VLSLV5-0 = 3FH		3.550			
V_{VLS} Hysteresis width (V_{DD}=rise)	H_{VLS}	–	V_{VLS} x 1.8%	V_{VLS} x 3.8%	V_{VLS} x 6.3%	V	1

VLSLV5-0 are bits of the VLSCON register to change detection voltage level.

[*1]: Setable only at the time of select to VLSP pin.

● DC characteristics (LLD)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD judge Voltage	VLLR	–	1.60	1.80	2.00	V	1

● DC/AC characteristics (Analog comparator)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common Input voltage range	V_{CMPIN}	–	0.2	–	V_{DD} -0.2	V	1
Input offset voltage	V_{CMPOF}	–	-30	–	30	mV	
Comparator judge time	T_{CMP}	CMPP- CMPM =40mV	–	–	2	µs	

● DC characteristics (LCD driver 1/2 V_{L1} based) (1/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD}=3.0V, Tj=25°C	LCN4-0 = 00H	0.79	0.84	0.89	V	1
			LCN4-0 = 01H	0.80	0.86	0.91		
			LCN4-0 = 02H	0.82	0.87	0.92		
			LCN4-0 = 03H	0.83	0.89	0.94		
			LCN4-0 = 04H	0.85	0.90	0.95		
			LCN4-0 = 05H	0.86	0.92	0.97		
			LCN4-0 = 06H	0.88	0.93	0.98		
			LCN4-0 = 07H	0.89	0.95	1.00		
			LCN4-0 = 08H	0.91	0.96	1.01		
			LCN4-0 = 09H	0.92	0.98	1.03		
			LCN4-0 = 0AH	0.94	0.99	1.04		
			LCN4-0 = 0BH	0.95	1.01	1.06		
			LCN4-0 = 0CH	0.97	1.02	1.07		
			LCN4-0 = 0DH	0.98	1.04	1.09		
			LCN4-0 = 0EH	1.00	1.05	1.10		
			LCN4-0 = 0FH	1.01	1.07	1.12		
			LCN4-0 = 10H	1.03	1.08	1.13		
			LCN4-0 = 11H	1.04	1.10	1.15		
			LCN4-0 = 12H	1.06	1.11	1.16		
			LCN4-0 = 13H	1.07	1.13	1.18		
			LCN4-0 = 14H	1.09	1.14	1.19		
			LCN4-0 = 15H	1.10	1.16	1.21		
			LCN4-0 = 16H	1.12	1.17	1.22		
			LCN4-0 = 17H	1.13	1.19	1.24		
			LCN4-0 = 18H	1.15	1.20	1.25		
			LCN4-0 = 19H	1.16	1.22	1.27		
			LCN4-0 = 1AH	1.18	1.23	1.28		
			LCN4-0 = 1BH	1.19	1.25	1.30		
			LCN4-0 = 1CH	1.21	1.26	1.31		
			LCN4-0 = 1DH	1.22	1.28	1.33		
			LCN4-0 = 1EH	1.24	1.29	1.34		
			LCN4-0 = 1FH	1.25	1.31	1.36		
V_{L1} temperature deviation	ΔV_{L1t}	V_{DD}=3.0V		–	-0.06	–	%/°C	
V_{L1} voltage dependency	ΔV_{L1v}	–		–	0.6	15	mV/V	

LCN4-0 of the DSPCNT register are bits to coordinate contrast of the LCD indication.

● DC characteristics (LCD driver 1/2 V_{L1} based) (2/2)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L2} voltage	V_{L2}	V_{DD} = 3.0V, Tj = 25°C BSN2-0 = 4H, 1MΩ_ load (V_{L5}−V_{SS})		Typ. −10%	V_{L1} (Typ) x 2	Typ. +10%	V	1
V_{L3} voltage	V_{L3}	V_{DD} = 3.0V, Tj = 25°C BSN2-0 = 4H, 1MΩ_ load (V_{L5}−V_{SS})	1/3 bias	Typ. −10%	V_{L1} (Typ) x 2	Typ. +10%		
			1/4 bias	Typ. −10%	V_{L1} (Typ) x 2	Typ. +10%		
			1/5 bias	Typ. −10%	V_{L1} (Typ) x 2.95	Typ. +10%		
V_{L4} voltage	V_{L4}		1/3 bias	Typ. −10%	$V_{L1(Typ)}$ x 2	Typ. +10%		
			1/4 bias	Typ. −10%	$V_{L1(Typ)}$ x 2.95	Typ. +10%		
			1/5 bias	Typ. −10%	$V_{L1(Typ)}$ x 3.9	Typ. +10%		
V_{L5} voltage	V_{L5}		1/3 bias	Typ. −10%	$V_{L1(Typ)}$ x 2.95	Typ. +10%		
			1/4 bias	Typ. −10%	$V_{L1(Typ)}$ x 3.9	Typ. +10%		
			1/5 bias	Typ. −10%	$V_{L1(Typ)}$ x 4.85	Typ. +10%		
LCD bias voltage generation time	T_{BIAS}	BSN2-0 = 4H		–	300	–	ms	

BSN2-0 of BIASCON register are bits to select a clock for multiplying the bias voltage in the bias generation circuit.

● DC characteristics (LCD driver 2/2 VL2 based) (1/2)

(V_{DD}=2.5 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L2} voltage	V_{L2}	V_{DD}=3.0V Tj=25°C	LCN4-0 = 00H	1.60	1.68	1.76	V	1
			LCN4-0 = 01H	1.63	1.71	1.79		
			LCN4-0 = 02H	1.66	1.74	1.82		
			LCN4-0 = 03H	1.69	1.77	1.85		
			LCN4-0 = 04H	1.72	1.80	1.88		
			LCN4-0 = 05H	1.75	1.83	1.91		
			LCN4-0 = 06H	1.78	1.86	1.94		
			LCN4-0 = 07H	1.81	1.89	1.97		
			LCN4-0 = 08H	1.84	1.92	2.00		
			LCN4-0 = 09H	1.87	1.95	2.03		
			LCN4-0 = 0AH	1.90	1.98	2.06		
			LCN4-0 = 0BH	1.93	2.01	2.09		
			LCN4-0 = 0CH	1.96	2.04	2.12		
			LCN4-0 = 0DH	1.99	2.07	2.15		
			LCN4-0 = 0EH	2.02	2.10	2.18		
			LCN4-0 = 0FH	2.05	2.13	2.21		
			LCN4-0 = 10H	2.08	2.16	2.24		
			LCN4-0 = 11H	2.11	2.19	2.27		
			LCN4-0 = 12H	2.14	2.22	2.30		
			LCN4-0 = 13H	2.17	2.25	2.33		
			LCN4-0 = 14H	2.20	2.28	2.36		
			LCN4-0 = 15H	2.23	2.31	2.39		
			LCN4-0 = 16H	2.26	2.34	2.42		
			LCN4-0 = 17H	2.29	2.37	2.45		
			LCN4-0 = 18H	2.32	2.40	2.48		
			LCN4-0 = 19H	2.35	2.43	2.51		
			LCN4-0 = 1AH	2.38	2.46	2.54		
			LCN4-0 = 1BH	2.41	2.49	2.57		
			LCN4-0 = 1CH	2.44	2.52	2.60		
			LCN4-0 = 1DH	2.47	2.55	2.63		
			LCN4-0 = 1EH	2.50	2.58	2.66		
			LCN4-0 = 1FH	2.53	2.61	2.69		
V_{L2} temperature deviation	ΔV_{L2t}	V_{DD}=3.0V		—	-0.06	—	%/°C	
V_{L2} voltage dependency	ΔV_{L2v}	—		—	0.9	20	mV/V	

LCN4-0 of the DSPCNT register are bits to coordinate contrast of the LCD indication.

● DC characteristics (LCD driver 2/2 V_{L2} based) (2/2)

(V_{DD}=2.5 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
V_{L1} voltage	V_{L2}	V_{DD} = 3.0V, Tj = 25°C 1MΩ_ load (V_{L5}–V_{SS})		Typ. –10%	$V_{L2(Typ)}$ x 0.5	Typ. +10%	V	1
V_{L3} voltage	V_{L3}	V_{DD} = 3.0V, Tj = 25°C BSN2-0 = 4H, 1MΩ_ load (V_{L5}–V_{SS})	1/3 bias	Typ. –10%	$V_{L2(Typ)}$	Typ. +10%		
			1/4 bias	Typ. –10%	$V_{L2(Typ)}$	Typ. +10%		
			1/5 bias	Typ. –10%	$V_{L2(Typ)}$ x 1.5	Typ. +10%		
V_{L4} voltage	V_{L4}		1/3 bias	Typ. –10%	$V_{L2(Typ)}$	Typ. +10%		
			1/4 bias	Typ. –10%	$V_{L2(Typ)}$ x 1.5	Typ. +10%		
			1/5 bias	Typ. –10%	$V_{L2(Typ)}$ x 2.0	Typ. +10%		
V_{L5} voltage	V_{L5}		1/3 bias	Typ. –10%	$V_{L2(Typ)}$ x 1.5	Typ. +10%		
			1/4 bias	Typ. –10%	$V_{L2(Typ)}$ x 2.0	Typ. +10%		
			1/5 bias	Typ. –10%	$V_{L2(Typ)}$ x 2.5	Typ. +10%		
LCD bias voltage generation time	T_{BIAS}	BSN2-0 = 4H		–	100	–	ms	

BSN2-0 of BIASCON register are bits to select a clock for multiplying the bias voltage in the bias generation circuit.

● DC characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P61, P70-P77, P80-P87)	VOH1	IOH=-1.0mA	V_{DD} -0.5	–	–	V	2
	VOL1	IOL=+0.5mA	–	–	0.4		
Output voltage 2 (P40, P41, P52, P53) (LED mode is selected)	VOL2	2.7V ≤ V_{DD} ≤ 3.6V IOL=+5.0mA	–	–	0.6		
		IOL=+2.0mA	–	–	0.4		
Output voltage 3 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55, P60, P61) (I^2C mode is selected)	VOL3	IOL3= +3mA (I^2Cspec) (V_{DD} ≥ 2V)	–	–	0.4		
Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55, P60, P61) (I^2C mode is selected)	VOL4	IOL4= +2mA(I^2Cspec) (V_{DD} < 2V)	–	–	V_{DD} ×0.2		
Output voltage 5 (P70-P77,P80-P87, COM0-23 SEG0-55) (LCD mode is selected)	VOH5	IOH5=-0.03mA / +0.03mA、Output:V_{L1}=1.0V	V_{L1} -0.2	–	V_{L1} +0.2		
		IOH5=-0.03mA / +0.03mA、Output:V_{L2}=2.0V	V_{L2} -0.2	–	V_{L2} +0.2		
		IOH5=-0.03mA / +0.03mA、Output:V_{L3}=3.0V	V_{L3} -0.2	–	V_{L3} +0.2		
		IOH5=-0.03mA / +0.03mA、Output:V_{L4}=4.0V	V_{L4} -0.2	–	V_{L4} +0.2		
		IOH5=-0.03mA / +0.03mA、Output:V_{L5}=5.0V	V_{L5} -0.2	–	V_{L5} +0.2		
	VOL5	IOL=+0.03mA、Output:V_{SS}	–	–	+0.2		
Output leak 1 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P61, P70-P77, P80-P87, COM0-23 SEG0-55)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	+1	μA	3
	IOOL1	VOL=V_{SS} (at high impedance)	-1	–	–		

● DC characteristics (IIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating *1			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	–	–	1	μA	4
	IIL1	VIL1=V_{SS}	-900	-300	-20		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	20	300	900		
	IIL2	VIL2=V_{SS}	-1	–	–		
Input current 3 (P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P61, P70-P77, P80-P87)	IIH3	VIH3=V_{DD} (at pull down)	1	15	200		
	IIL3	VIL3=V_{SS} (at pull up)	-200	-15	-1		
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1		
	IIL3Z	VIL3=V_{SS} (at high impedance)	-1	–	–		

*1 : typ.rating is Ta=25°C , V_{DD}=3.0V

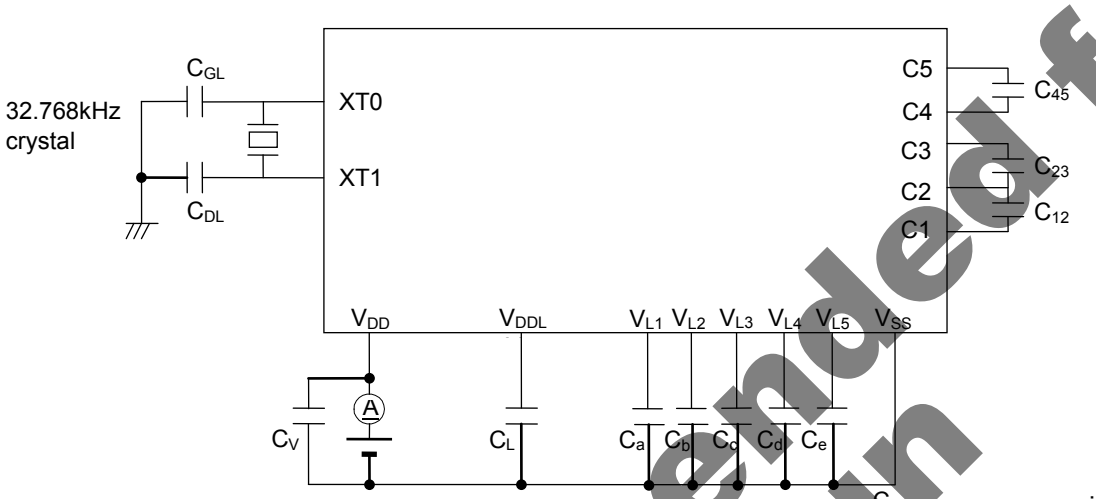
● DC characteristics (VIHL)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, TEST0, TEST1_N, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P61, P70-P77, P80-P87)	VIH1	–	0.7 ×V_{DD}	–	V_{DD}	V	5
	VIL1	–	0	–	0.3 ×V_{DD}		
Input terminal capacitance (RESET_N, TEST0, TEST1_N, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57, P60-P61, P70-P77, P80-P87)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	–	–	10	pF	–

● MEASURING CIRCUITS

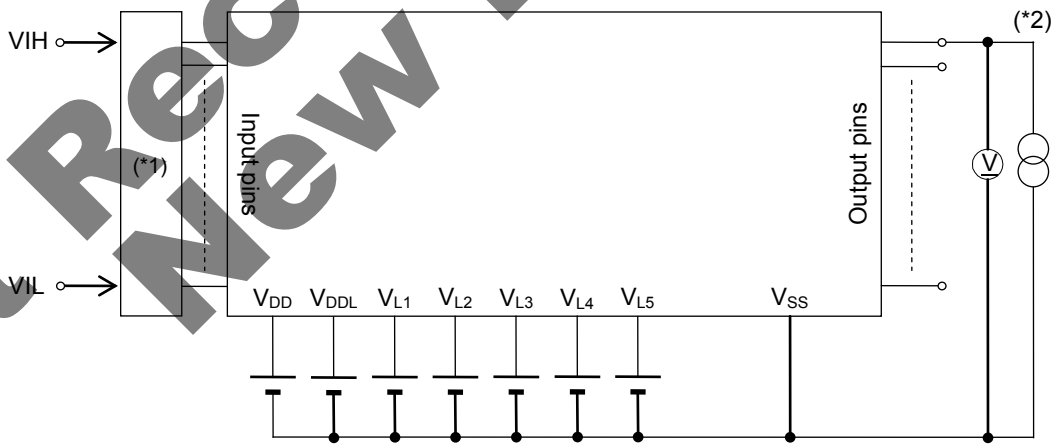
MEASURING CIRCUIT1



C_V	: 1μF
C_L	: 2.2μF
C_a,C_b,C_c,C_d,C_e	: 1μF
C_{12},C_{23},C_{45}	: 1μF
C_{GL}	: 12pF
C_{DL}	:12pF

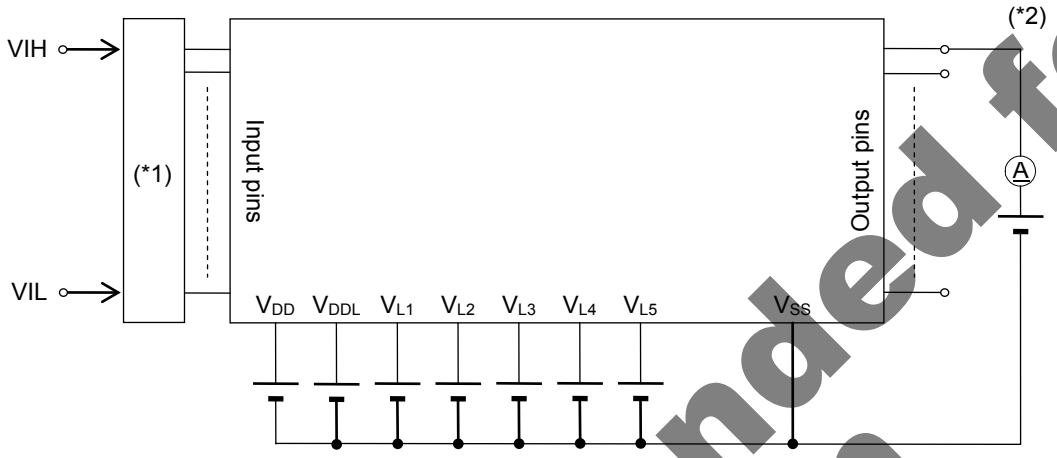
32.768kHz crystal oscilation:
(DT-26 from Daishinku)

MEASURING CIRCUIT 2



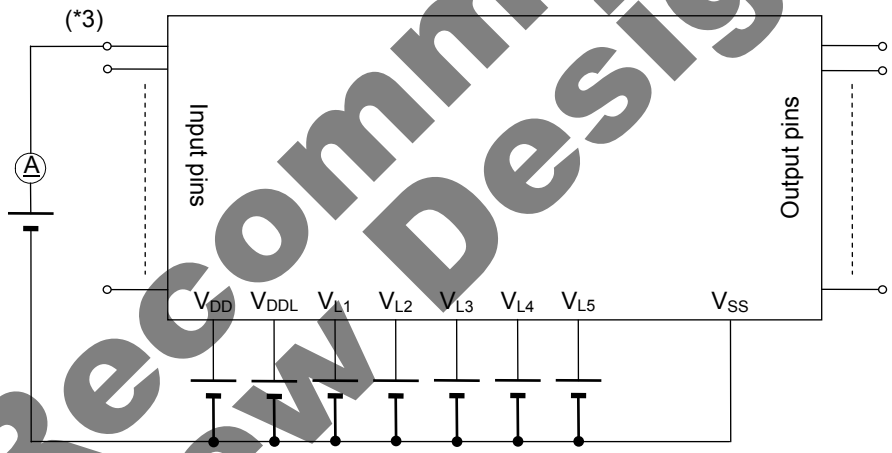
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



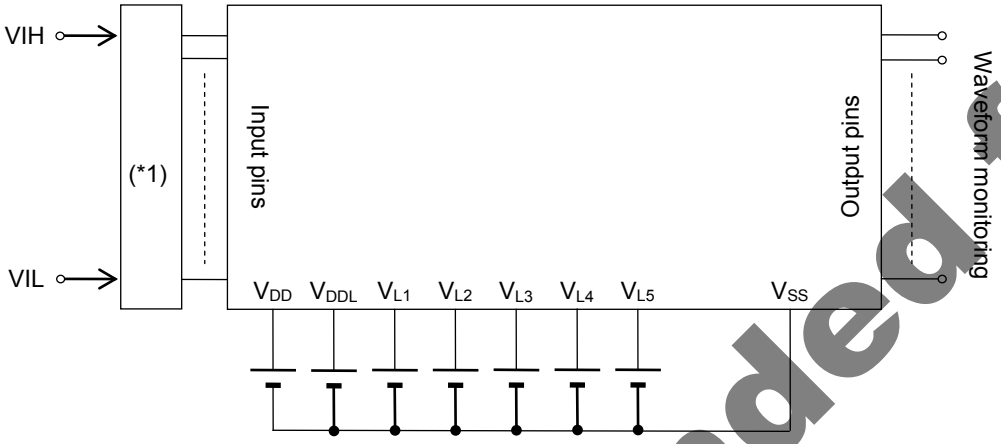
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

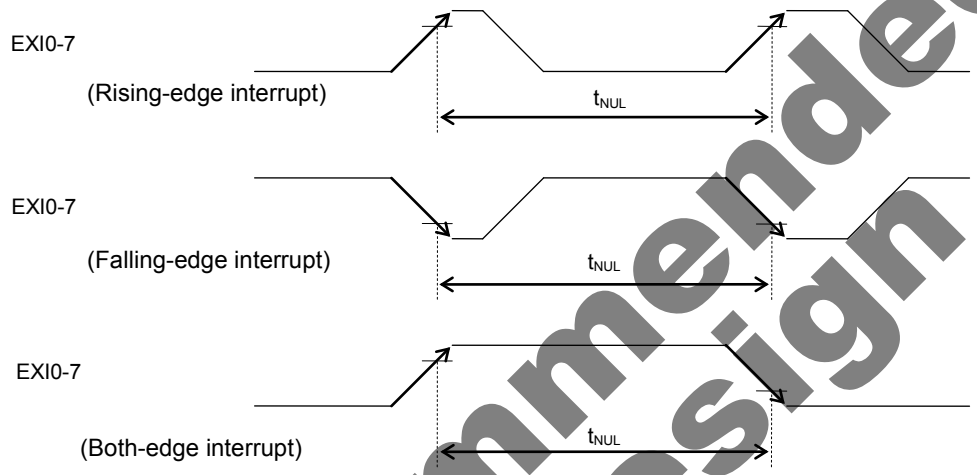


*1: Input logic circuit to determine the specified measuring conditions.

● AC characteristics（external interrput）

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	t_{NUL}	Interruput enable (MIE=1) CPU : NOP operation	2.5 x sysclk	–	3.5 x sysclk	φ

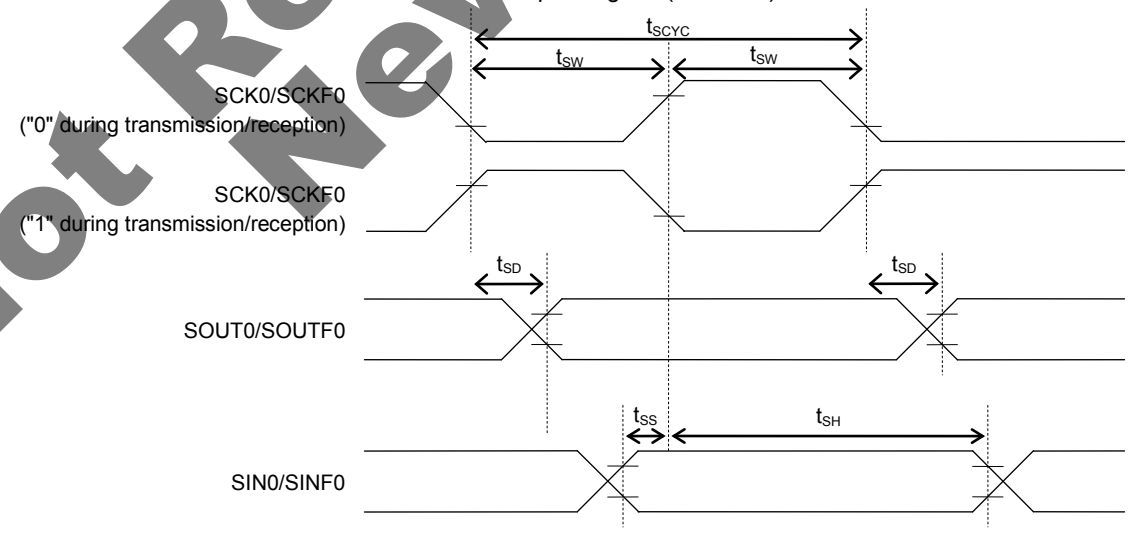


● AC charctoristics (synchronous serial port)

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Conditon	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation is not active	10	–	–	µs
		High-speed oscillation is active	500	–	–	ns
SCK output cycle (master mode)	t_{SCYC}	–	–	SCK*1	–	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation is not active	4	–	–	µs
		High-speed oscillation is active	200	–	–	ns
SCK output pulse width (master mode)	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	–	–	–	180	ns
SOUT output delay time (master mode)	t_{SD}	–	–	–	80	ns
SIN input Setup time (slave mode)	t_{SS}	–	50	–	–	ns
SINinput Hold time	t_{SH}	–	50	–	–	ns

*1 : The clock period which is selected by the below registers(min:250ns@ regularly, min:500ns@P02,P22 is used)
In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).
In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



● AC characteristics（I^2C Bus interface : Standard mode 100kHz）

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

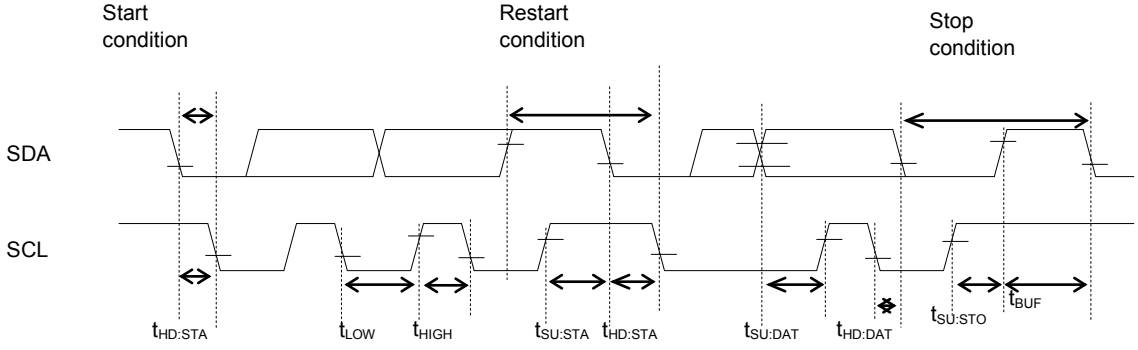
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	100	kHz
SCL hold time (Start/restart condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL"L" level time	t_{LOW}	–	4.7	–	–	µs
SCL"H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA hold time	$t_{HD:DAT}$	–	0	–	3.45	µs
SDA setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SDA setup time (stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus-free time	t_{BUF}	–	4.7	–	–	µs

● AC characteristics（I^2C bus interface : fast mode 400kHz）

(V_{DD}=1.8 to 3.6V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rateing			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	400	kHz
SCLhold time (start/restart condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL"L" level time	t_{LOW}	–	1.3	–	–	µs
SCL"H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA hold time	$t_{HD:DAT}$	–	0	–	0.9[*1]	µs
SDA setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SDA setup time (stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus-free time	t_{BUF}	–	1.3	–	–	µs

[*1]: Only at the time of SYSCLK=16MHz.



● AC characteristics (RC-ADC)

(V_{DD}=1.8~3.6V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

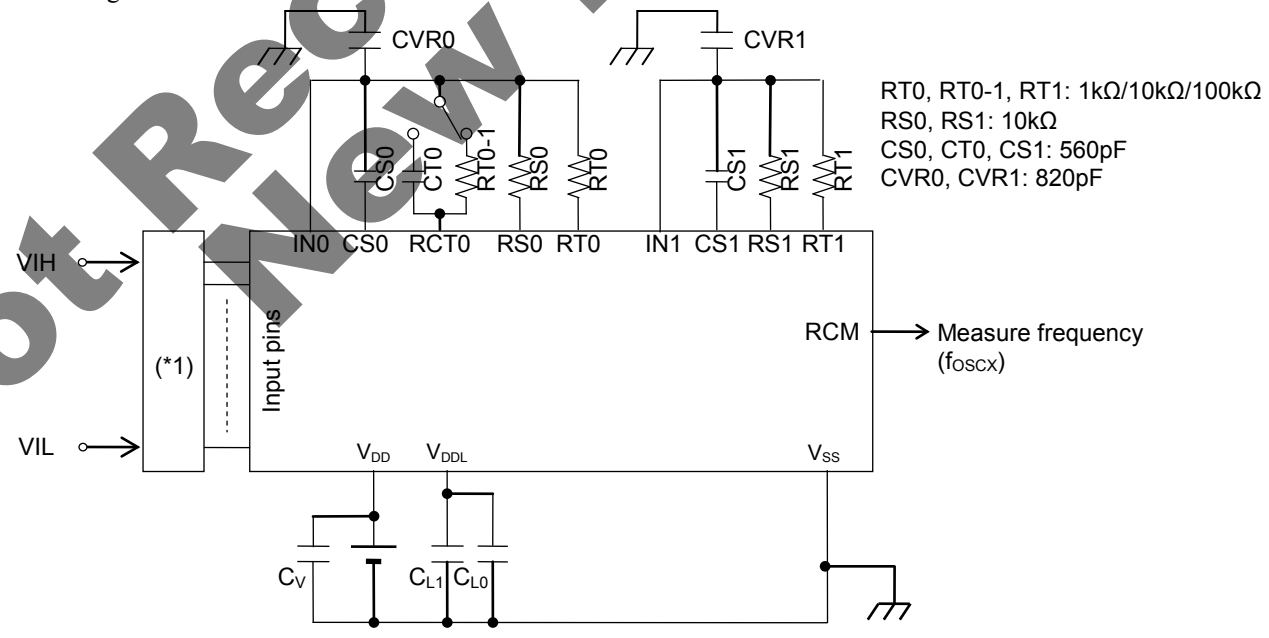
Parameter	Symbol	Condition	Rating			unit
			Min.	Typ.	Max.	
Resister for oscillation	RS0,RS1,RT0,RT0-1,RT1	–	1	–	400	kΩ
Oscillation freqency V_{DD} = 3.0V CVR=820pF CS=560pF	f_{OSC1_0}	Resister for oscillation =1kΩ	–	528	–	kHz
	f_{OSC2_0}	Resister for oscillation =10kΩ	–	59	–	kHz
	f_{OSC3_0}	Resister for oscillation =100kΩ	–	5.9	–	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V CVR=820pF CS=560pF	Kf1_0	RT0, RT0-1, RT1=1kΩ	8.225	8.94	9.655	–
	Kf2_0	RT0, RT0-1, RT1=10kΩ	0.99	1	1.01	–
	Kf3_0	RT0, RT0-1, RT1=100kΩ	0.093	0.101	0.109	–

*1 : Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}\ (\text{RT0-CS0 oscillation})}{f_{OSCX}\ (\text{RS0-CS0 oscillation})}, \frac{f_{OSCX}\ (\text{RT0-1-CS0 oscillation})}{f_{OSCX}\ (\text{RS0-CS0 oscillation})}, \frac{f_{OSCX}\ (\text{RT1-CS1 oscillation})}{f_{OSCX}\ (\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)

Measuring circuit



(*1) Input logic circuit to determine the specified measuring conditions.

【Note】

・Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

・When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by V_{SS}(GND).

・Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have

● AC characteristics (Low speed clock output)

(V_{DD}=1.8~3.6V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

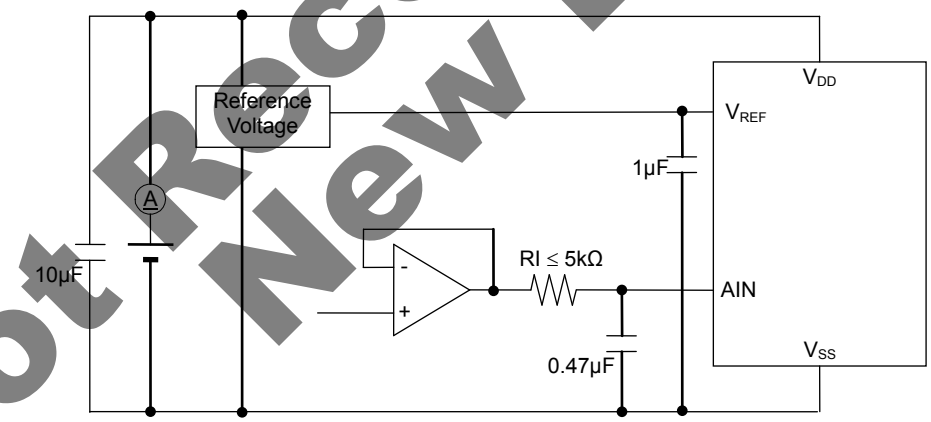
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Clock output frequency	tclk	–	–	32.768	–	kHz

● Electrical Characteristics of SA-ADC

(V_{DD}=1.8~3.6V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

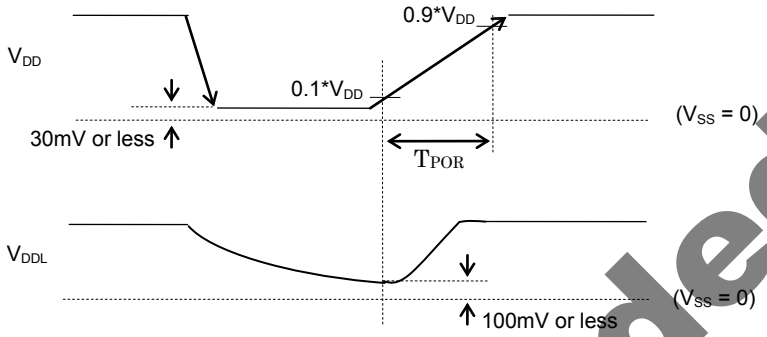
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	–	–	12	–	bit
Integral non-linearity error	INL	2.7V ≤ V_{REF} ≤ 3.6V	−4	–	+4	LSB
		2.2V ≤ V_{REF} < 2.7V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	−3	–	+3	
		2.2V ≤ V_{REF} < 2.7V	−5	–	+5	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−9	–	+9	
Zero-scale error	V_{OFF}	2.2V ≤ V_{REF} ≤ 3.6V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Full-scale error	FSE	2.2V ≤ V_{REF} ≤ 3.6V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Input impidance	RI	–	–	–	5k	Ω
Reference voltage	V_{REF}	–	1.8	–	V_{DD}	V
Conversion time	t_{CONV}	Using High-speed clock(max. 4MHz)	–	170	–	clk
		Using Low-speed clock	–	16	–	

Measuring circuit



● Power-on and shutdown Procedures

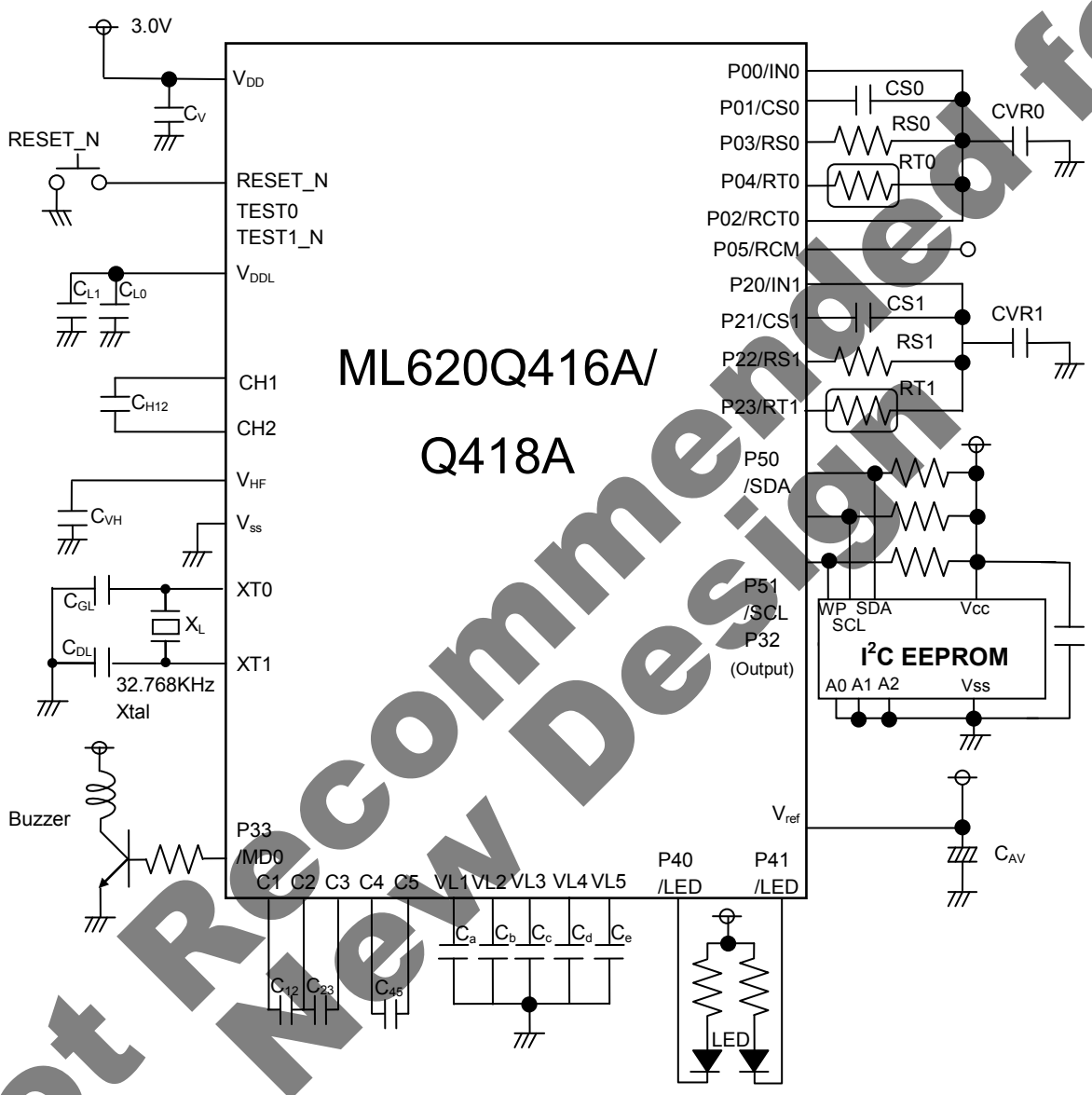
In case of power-on or shutdown of V_{DD}, the procedures and constraints are shown as following.



Power down/on and power on reset sequence

Note:
If VDDL level is 100mV or more over, reset the IC by RESET_N pin after power-on.

■ APPLICATION CIRCUIT EXAMPLE



C_V	: 1uF*		
C_{L1}	: 2.2uF	C_{L0}	: open*
C_{GL}	: 12～16pF*	C_{GH}	: 12～20pF*
C_a~C_e	: 1uF*	C_{12},C_{23},C_{45}	: 1uF*
C_{H12}	: 1uF*	C_{VH}	: 1uF*
C_{AV}	: 1uF*	RS0, RS1	: 10 KΩ
CS0, CS1	: 560 pF	CVR0, CVR1	: 820 pF
RT0, RT1	: Thermistor (103AT/Semitec)		
X_L	: DT-26, Daishinku		

*: Make a decision the parameters after evaluating on an user's conditions when designing circuits for mass production.

■ REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL620Q416A-01	Apr.22.2016	–	–	Preliminary Edition 1
FEDL620Q416A-01	Jan. 5 2017	–	–	Final Edition 1

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