Cache specification

4 way SA

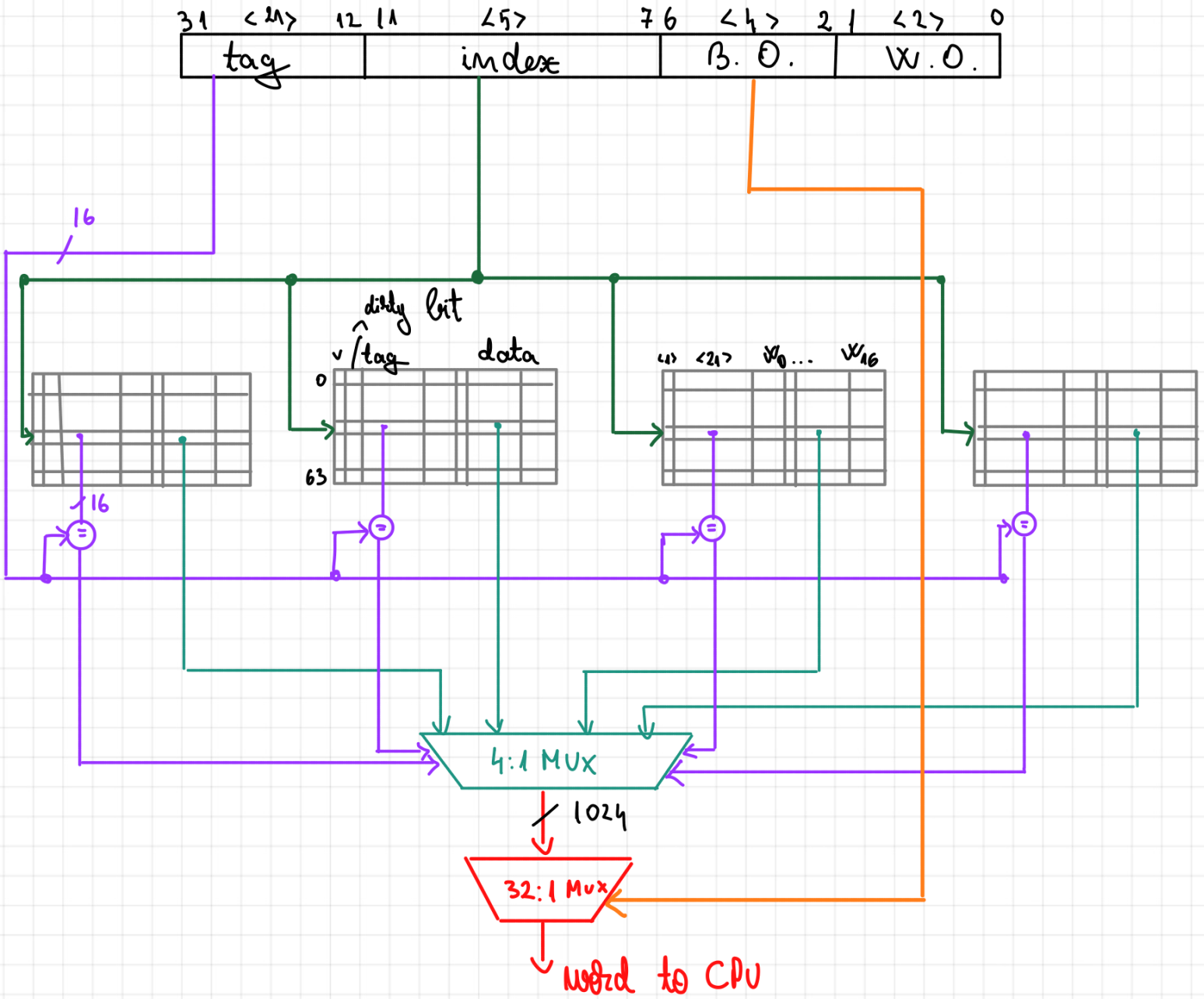
P.a = 32 bits

1 word = 4B = 2^2 B ⇒ W.O = 2

1 block = 64 B = 16 words = 2^4 words ⇒ B.O. = 4

128 sets ⇒ $\frac{128}{4}$ = 32 = 2^5 sets ⇒ index = 5

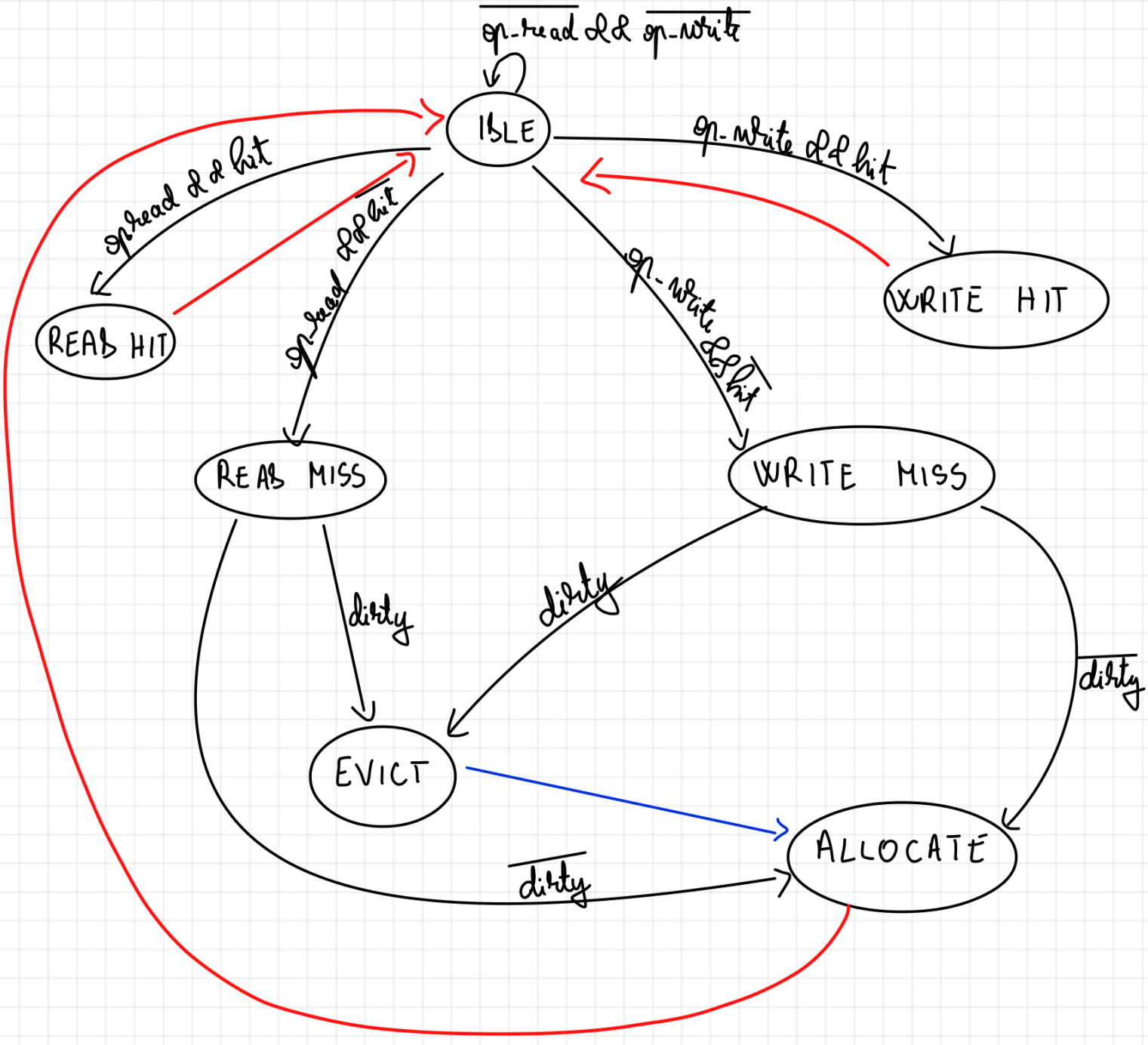
32 − 5 − 4 − 2 = 21



FSM

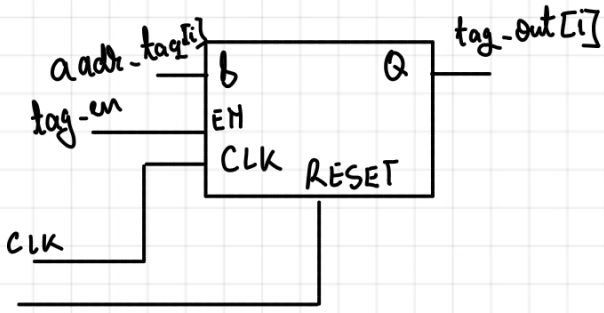
Stări + codificare

IDLE = 3'b000
READ_HIT = 3'b001
READ_MISS = 3'b010
WRITE_HIT = 3'b011
WRITE_MISS = 3'b100
EVICT = 3'b101
ALLOCATE = 3'b110



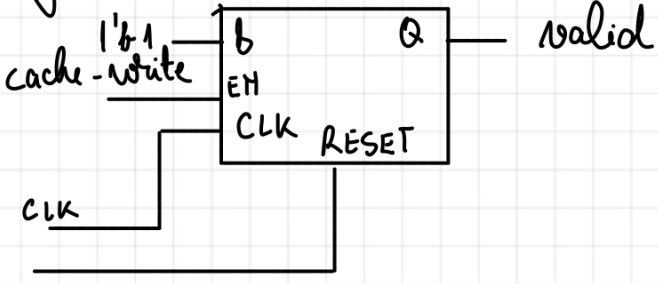
Cache line

TAG register (b-FF)



× tag_size

VALID register



-> tot cu d-ff ne calculăm și DIRTY bit și DATA register

Cache controller