EM78M612

Universal Serial Bus Microcontroller

V1.1

Specification Revision History		
Version	**Content**	**Update**
1.0	• Initial Version	2003/03/05
1.1	• Correction for some text in General Description－P2,rom size 12K→2K • Correction for Pin Configuration of EM78M612XBP－P5 • ADC Converter Channel Selector Table fixed－P16,CH1 Reserved • Added PDA Register Description－P20,IOC9 • Correction for EEPROM Function Description－P24 • Changes made to PDA Function Description－P29-32 • Revised ADC Converter ready bit for ADC Operation－P17,P34,RAS[7]	2004/04/28

SPECIFICATION

1 General Description

The EM78M612 is a series of Universal Serial Bus 8-bit RISC Multi-Time Programming (MTP) microcontrollers. It is specifically designed for USB low speed device application and to support legacy device such as PS/2 mouse. The EM78M612 also support one device address and two endpoints. With no firmware involved, these series of microcontrollers can automatically identify and decode Standard USB Command to EndPoint Zero.

The EM78M612 is implemented on a RISC architecture. It has five-level stack and eight interrupt sources. The amount of General Input/Output pins is up to 15. Each device has 112 bytes SRAM and is embedded with 4 bytes of E^{2}PROM. The ROM size of the EM78M612 is 2K.

These series of chips have special features that accommodate your needs. These features are:

■ Dual Clock mode which allows the device to run on very low power saving frequency

■ Pattern Detecting Application function which is used in a serial transmission to count waveform width

■ Width Modulation that can generate a duty-cycle-programmable signal

■ AD converter with up to 10 bits resolution.

2 Features

■ Low-cost solution for low-speed USB devices, such as mouse, joystick, and gamepad.

■ USB Specification Compliance
   ● Universal Serial Bus Specification Version 1.1
   ● USB Device Class Definition for Human Interface Device (HID), Firmware Specification Version 1.1
   ● Support 1 device address and 2 endpoints

■ USB Application
   ● USB protocol handling
   ● USB device state handling
   ● Identifies and decodes Standard USB commands to EndPoint Zero

■ PS/2 Application Support
   ● Auto-detects PS/2 or USB port
   ● Built-in PS/2 port interface

- Built-in 8-bit RISC MCU
  - 5 level stacks for subroutine and interrupt
  - 8 available interrupts
  - 8-bit real time clock/counter (TCC) with overflow interrupt
  - Built-in RC oscillator free running for WatchDog Timer and Dual clock mode
  - Two independent programmable prescalers for WDT and TCC
  - Two methods of power saving:
    1. Power-down mode (SLEEP mode)
    2. Low frequency mode.
  - Two clocks per instruction cycle
  - Multi-time programmable

- I/O Ports
  - Up to 15 general purposes I/O pins grouped into two ports (Port 6 and 7).
  - Up to 2 LED sink pins
  - Each GPIO pin of Ports 6 has an internal programmable pull-high resistor (200K Ohms)
  - Each GPIO pin wakes up the MCU from sleep mode by input state change

- Internal Memory
  - Built-in 2048K*13 bits Program ROM
  - Built-in 112 bytes general purpose registers (SRAM)
  - Built-in USB Application FIFOs.
  - Built-in 4 bytes E^{2}PROM (EM78M612∗B, EM78M612∗D)

- Operation Frequency
  - Normal Mode: MCU runs on the external oscillator frequency
  - Dual Clock Mode: MCU runs at the frequency of 256KHz (or 32KHz, 4KHz, 500Hz), emitted by the internal oscillator with the external ceramic resonator (or crystal) turned off to save power.

- Built-in Pattern Detecting Application for serial signal transmission

- Built-in Pulse Width Modulation (PWM)
  - Up to 2 channels PWM function on P.64 (PWM1) and P.65 (PWM2).
  - Up to 8-bit resolution PWM output
  - Up to 8 selections of duty cycles

- Built-in 15-Channel Analog-to-Digital Converter (ADC)
  - Built-in AD Converter with 10-bit resolution

- 4 ADC conversion rates: 256K/128K/64K/32K

■ Built-in 3.3V Voltage Regulator

- For MCU power supply
- Pull-up source for the external USB resistor on D-pin.

■ Package Type

- 16 pin PDIP/SOP (EM78M612(A/B/C/D) A P/M)
- 18 pin PDIP/SOP (EM78M612(A/B/C/D) B P/M)
- 20 pin PDIP/SOP (EM78M612(A/B/C/D) C P/M)
- 20 pin SSOP (EM78M612(A/B/C/D) EM)
- 24 pin PDIP/SOP (EM78M612(A/B/C/D) D P/M)
- 24 pin SSOP (EM78M612(A/B/C/D) FM)

3 Type Definition

The EM78M612 series has sereval types of packaging. Each type is divided into 4 modules, namely; original, with E^2PROM, with A/D converter, and with both E^2PROM and A/D converter. Hence, packaging configuration for each series is defined. The Table 3.1 below summarizes which series of the EM78M612 belong to which module.

Original	With E^2PROM	With A/D Converter	With Both
EM78M612A∗∗	EM78M612B∗∗	EM78M612C∗∗	EM78M612D∗∗

Table 3-1 Packaging Summary of EM78M612 Series IC

4 Applications

This microcontroller is designed for USB low speed device application or non-USB embedded device. It is also suitable for PS/2 mouse application.

5 Pin Configuration

P61	1●	16	P60/V_{PP}
P62	2	15	P64
P63	3	14	P65
P70	4	13	P71
V_{SS}	5	12	D+/P50
V_{NN}	6	11	D-/P51
$V_{3.3V}$	7	10	V_{DD}
OSCI	8	9	OSCO

◆**EM78M612XAP**

P60/V_{PP}	1●	20	P64
P61	2	19	P65
P62	3	18	P66
P63	4	17	P67
P70	5	16	P71
P72	6	15	P73
V_{SS}	7	14	D+/P50
V_{NN}	8	13	D-/P51
$V_{3.3V}$	9	12	V_{DD}
OSCI	10	11	OSCO

◆**EM78M612XCP**

P60/V_{PP}	1●	18	P64
P61	2	17	P65
P62	3	16	P66
P63	4	15	P67
P70	5	14	P71
V_{SS}	6	13	D+/P50
V_{NN}	7	12	D-/P51
$V_{3.3V}$	8	11	V_{DD}
OSCI	9	10	OSCO

◆**EM78M612XBP**

P60/V_{PP}	1●	24	P64
P61	2	23	P65
P62	3	22	P66
P63	4	21	P67
P70	5	20	P71
P72	6	19	P73
P74	7	18	P75
P76	8	17	P77
V_{SS}	9	16	D+/P50
V_{NN}	10	15	D-/P51
$V_{3.3V}$	11	14	V_{DD}
OSCI	12	13	OSCO

◆**EM78M612XDP**

6 Pin Description

Symbol	I/O	Function
OSCI	I	6MHz / 12MHz ceramic resonator or crystal input.
OSCO	I/O	Return path for 6-MHz / 12MHz ceramic resonator or crystal.
V_{NN}		Used in programming the on-chip ROM. During normal operation, this pin is connected to Ground.
$V_{3.3V}$	O	3.3V DC voltage output from internal regulator. This pin has to be tied to a 4.7 μ F capacitor.
$P60/V_{PP}$	I	P60 functins as an input pin only (no output) For serial signal transmission application, the Pin P60 is used as a serial signal input pin. For detailed usage and function, refer to Section 8.8, *Pattern Detecting Application* of this Spec.
P61 ~ P67	I/O	7 GIOP pins. The pull high resistors (200K Ohms) and pull low resistors (15K Ohm) are selected through pin programming. All Port6 I/O pins are used for AD function. Furthermore,P64 & P65 can also be used for PWM function.
P70 ~ P77	I/O	Port7 offers up to 8 GIOP pins. The sink current of P70 & P71 are programmable for driving LED. Each pin has pull high resistors (200K Ohm) that can be selected through pin programming. All Port7 I/O pins can be used for AD function.
D+ / P50	I/O	USB Plus data line interface or PS/2 line interface are user-defined through firmware setting. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes.
D- / P51	I/O	USB Minus data line interface or PS/2 line interface are user-defined through firmware setting. When this pin is used as a PS/2 line interface, it will generate an interrupt when its state changes.
V_{DD}	-	Connects to the USB power source or to a nominal 5V-power supply. Actual V_{DD} range can vary between 4.4V and 5.2V.
V_{SS}	-	Connects to ground.

Table 7.1   Pin Descriptions
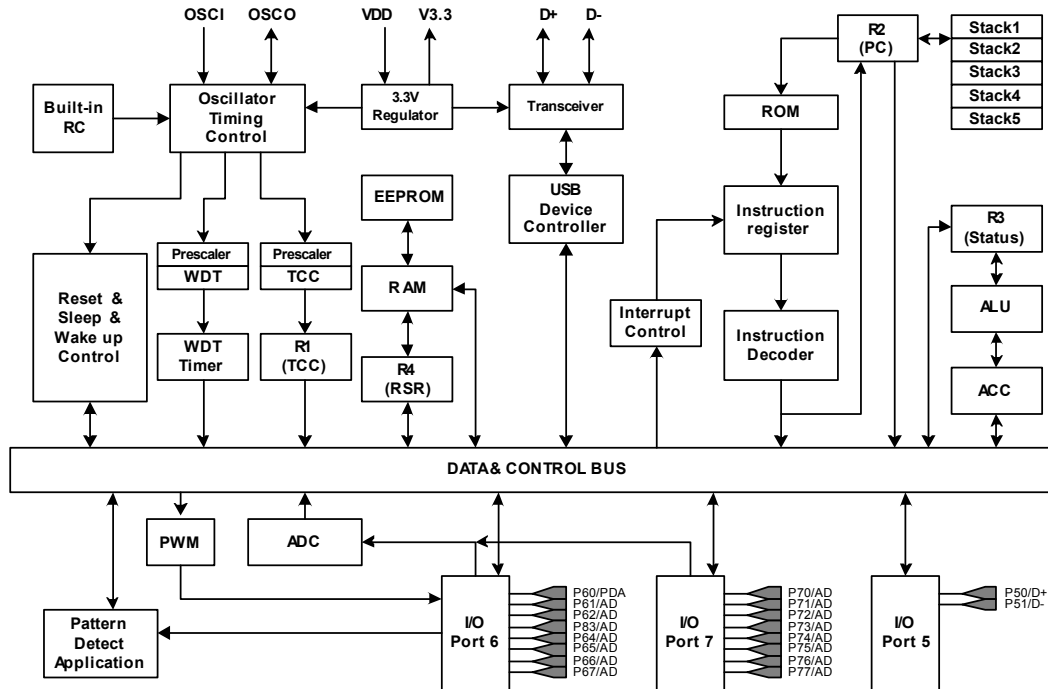
7 Function Block Diagram

Figure 7   EM78M612 Series Function Block Diagram
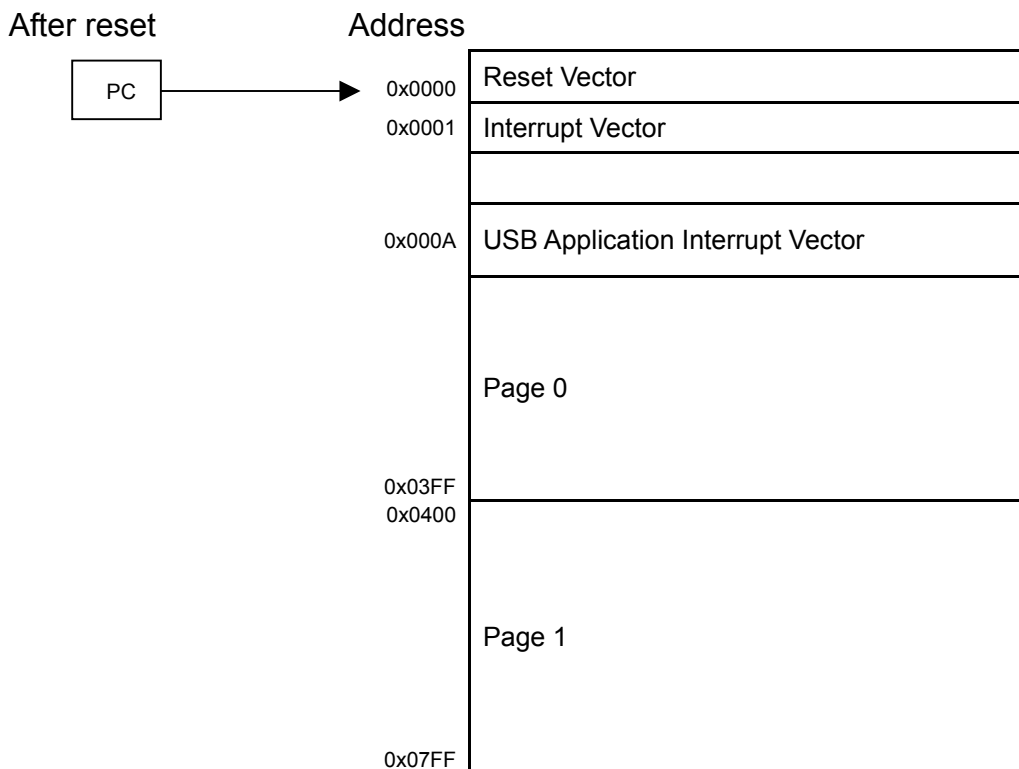
8 Function Description

The EM78M612 memory is organized into 4 spaces, namely; User Program Memory in 2048*13 bits ROM space, Data Memory in 112 bytes SRAM space, and USB Application FIFOs (for EndPoint0 and EndPoint1). Furthermore, several registers are used for special purposes.

8.1 Program Memory

The program space of the EM78M612 is 2K bytes, and is divided into two pages. Each page is 1K bytes long. After Reset, the 11-bit Program Counter (PC) points to location zero of the program space.

It has two interrupt vectors, i.e., Interrupt Vectors at 0x0001 and USB Application Interrupt Vectors at 0x000A. The Interrupt Vector applies to TCC Interrupt, High Pattern Detecting Interrupt, Low Pattern Detecting Interrupt, and Port 5 State Changed Interrupt. The USB Application Interrupt Vector is for USB EndPoint Zero Interrupt, USB Suspend Interrupt, USB Reset interrupt ,and USB Host Resume Interrupt.

After an interrupt, the MCU will fetch the next instruction from the corresponding address as illustrated in the following diagram.

After reset	Address	
PC →	0x0000	Reset Vector
	0x0001	Interrupt Vector
	0x000A	USB Application Interrupt Vector
		Page 0
	0x03FF	
	0x0400	Page 1
	0x07FF	

8.2 Data Memory

The Data Memory has 112 bytes SRAM space. It is also equipped with USB Application FIFO space for USB Application. The Figure 8.1 (next page) shows the organization of the Data Memory Space.

8.2.1   Special Purpose Registers

When the microcontroller executes instruction, specific registers are invoked for assistance, such as; Status Register which records the calculation status, Port I/O Control Registers which control the I/O pins' direction, etc. The EM78M612 series provides a lot more of other special purpose registers with different functions.

There are 23 Special Operation Registers which are located from Address 0x00 to 0x0E in Bank0, and from Address 0x08 to 0x0F in Bank1. On other hand, 17 more Special Control Registers are available to control functions or I/O direction. These are arranged from Address 0x05 to 0x0F in Bank0, and from Address 0x08 to 0x0F in Bank1.

Note that Special Control Registers can only be read or written by two instructions; IOR and IOW. To access registers from Bank1, the Special Purpose Registers Bank selector (R3[7]) should be set first.
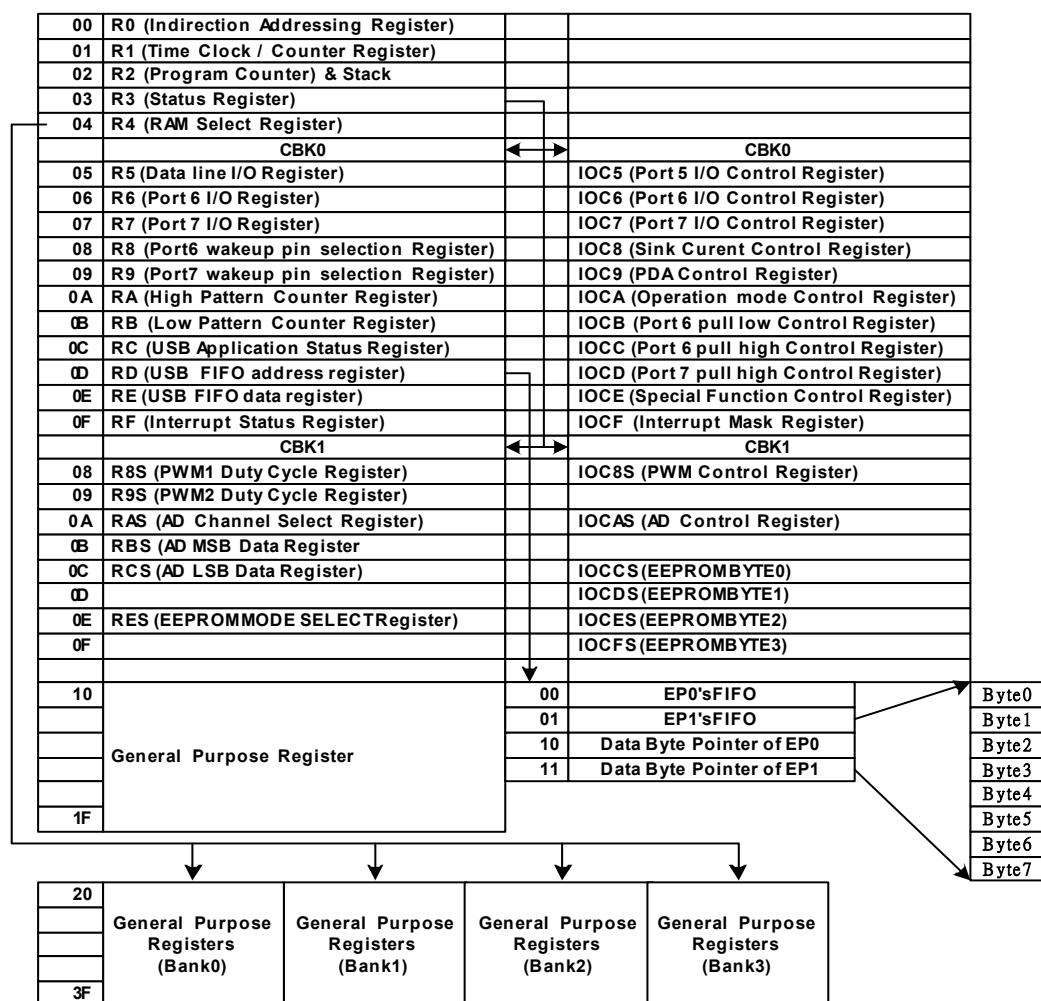
00	R0 (Indirection Addressing Register)		
01	R1 (Time Clock / Counter Register)		
02	R2 (Program Counter) & Stack		
03	R3 (Status Register)		
04	R4 (RAM Select Register)		
	CBK0		CBK0
05	R5 (Data line I/O Register)		IOC5 (Port 5 I/O Control Register)
06	R6 (Port 6 I/O Register)		IOC6 (Port 6 I/O Control Register)
07	R7 (Port 7 I/O Register)		IOC7 (Port 7 I/O Control Register)
08	R8 (Port6 wakeup pin selection Register)		IOC8 (Sink Curent Control Register)
09	R9 (Port7 wakeup pin selection Register)		IOC9 (PDA Control Register)
0A	RA (High Pattern Counter Register)		IOCA (Operation mode Control Register)
0B	RB (Low Pattern Counter Register)		IOCB (Port 6 pull low Control Register)
0C	RC (USB Application Status Register)		IOCC (Port 6 pull high Control Register)
0D	RD (USB FIFO address register)		IOCD (Port 7 pull high Control Register)
0E	RE (USB FIFO data register)		IOCE (Special Function Control Register)
0F	RF (Interrupt Status Register)		IOCF (Interrupt Mask Register)
	CBK1		CBK1
08	R8S (PWM1 Duty Cycle Register)		IOC8S (PWM Control Register)
09	R9S (PWM2 Duty Cycle Register)		
0A	RAS (AD Channel Select Register)		IOCAS (AD Control Register)
0B	RBS (AD MSB Data Register)		
0C	RCS (AD LSB Data Register)		IOCCS (EEPROM BYTE0)
0D			IOCDS (EEPROM BYTE1)
0E	RES (EEPROM MODE SELECT Register)		IOCES (EEPROM BYTE2)
0F			IOCFS (EEPROM BYTE3)

10		00	EP0's FIFO	Byte0
		01	EP1's FIFO	Byte1
	General Purpose Register	10	Data Byte Pointer of EP0	Byte2
		11	Data Byte Pointer of EP1	Byte3
				Byte4
				Byte5
				Byte6
1F				Byte7

20	General Purpose Registers (Bank0)	General Purpose Registers (Bank1)	General Purpose Registers (Bank2)	General Purpose Registers (Bank3)
3F				

Fig 8.1 The Organization of EM78M612 Data RAM

8.2.1.1 Operation Registers in Bank 0

The following introduces each of the Operation Registers under the Special Purpose Registers in Bank 0. These Operation Registers are arranged according to the order of registers' address. Note that some registers are read only, while others are both readable and writable.

R0 (Indirect Address Register)   *Default Value: (0B_0000_0000)*

R0 is not a physically implemented register. Its major function is to be an indirect address pointer. Any instruction using R0 as a pointer actually accesses the data pointed by the RAM Select Register (R4).

R1 (Time / Clock Counter)   *Default Value: (0B_0000_0000)*

This register TCC, is an 8-bit timer or counter. It is readable and writable as any other register.

After Power-on reset and WatchDog reset, the initial value of this register is 0x00.

R2 (Program Counter & Stack)   *Default Value: (0B_0000_0000)*

The EM78M612 Program Counter is an 11-bit long register that allows access to 2K bytes of Program Memory. The Program Counter is cleared after Power-on reset or WatchDog reset. The first instruction that is executed after a reset is located at Address 00h.
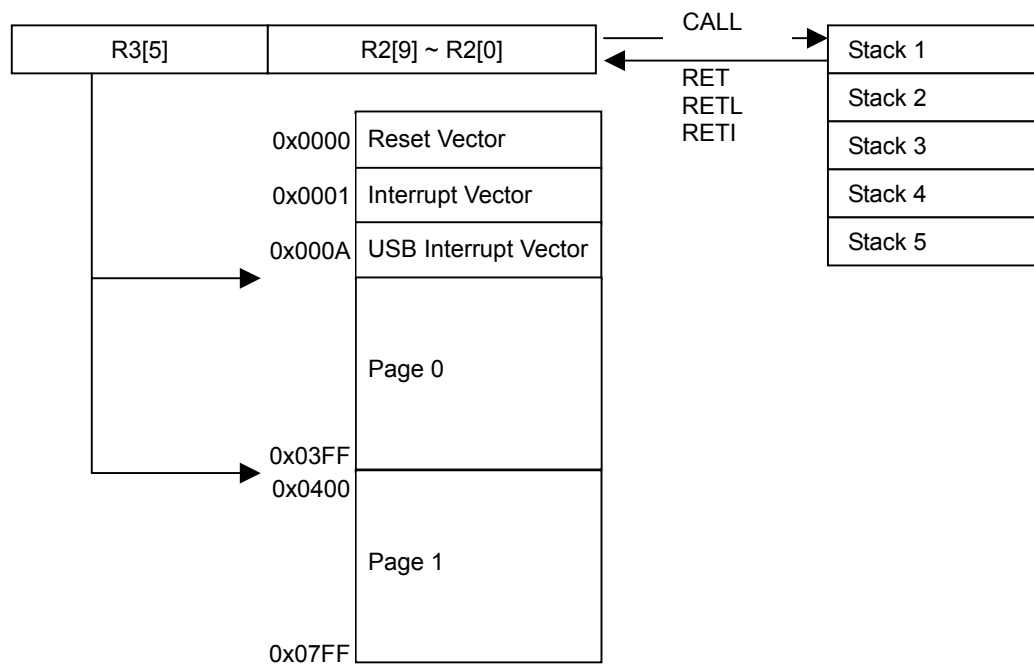
R3 (Status Register) *Default Value:(0B_0001_1000)*

7	6	5	4	3	2	1	0
SPRBS	-	PS0	T	P	Z	DC	C

R3 [0] Carry flag.

R3 [1] Auxiliary carry flag.

R3 [2] Zero flag. It will be set to 1 when the result of an arithmetic or logic operation is zero.

R3 [3] Power down flag. It will be set to 1 during Power-on phase or by "WDTC" command and cleared when the MCU enters into Power down mode. It remains in its previous state after WatchDog Reset.
1: Power-on.
0: Power down

R3 [4] Time-out flag. It will be set to 1 during Power-on phase or by "WDTC" command. It is reset to 0 by WDT time-out.
1: WatchDog timer without overflow.
0: WatchDog timer with overflow.

The various states of Power down flag and Time-out flag at different conditions are shown below:

T	P	Condition
1	1	Power-on reset
1	1	WDTC instruction
0	*P	WDT time-out
1	0	Power down mode
1	0	Wakeup caused by port change during Power down mode

*P: Previous status before WDT reset

R3 [5] Page selection bit. This bit is used to select a page of program memory (refer to R2, Program Counter).

PS0	Program Memory Page [Address]
0	Page 0 [0000-03FF]
1	Page 1 [0400-07FF]

R3 [6] General purpose registers.

R3 [7] Special purpose registers bank selector.
1: R8S ~ RFS; IOC8S ~ IOCFS
0: R5 ~ RF; IOC5 ~ IOCF

R4 (RAM Select Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
BK1	BK0	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0

R4 (RAM select register) contains the address of the registers.

R4 [0~5] are used to select registers in 0x00h~0x3Fh. The address 0x00~0x1F is common space. After 0x1Fh, SRAM is grouped into four banks.

R4 [6,7] are used to select register banks. To select a registers bank, refer to the following examples and the table below**:**

(1) R4=00001100 and R4=01001100 point to the same register 0x0Ch. Since 0x0Ch is in the common space, Bit 6 and Bit 7 are meaningless.

(2) R4=10111100 points to the register 0x3C in Bank 2.

R4[7]Bk1	R4[6]Bk0	RAM Bank #
0	0	Bank 0
0	1	Bank 1
1	0	Bank 2
1	1	Bank3

R5 (Data Line I/O Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
-	-	-	-	-	-	D- or PS/2	D+ or PS/2

R5 [0]   D+ line register or PS/2 clock interface register.
R5 [1]   D- line register or PS/2 data interface register.
These two bits are BOTH writable and readable when the MCU is operating under PS/2 mode. But under USB Mode, these two bits cannot be accessed.

R5 [2~7] General purpose registers.

R6 (Port 6 I/O Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	P60

R7 (Port 7 I/O Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

R8 (Port 6 Wake-up Pin Selection Register) *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
/Wu87	/wu86	/Wu85	/Wu84	/Wu83	/Wu82	/Wu81	/Wu80

R8 [0 ~ 7] Select which of the Port 6 pins are to be defined to wake-up the MCU from sleep
mode. When the state of the selected pins changes during sleep mode, the
MCU will wake-up and execute the next instruction automatically.
1: Disable the wake-up function
0: Enable the wake-up function

R9 (Port 7 Wake-up Pin Selection Register) *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
/Wu77	/Wu76	/Wu76	/Wu74	/Wu73	/Wu72	/Wu71	/Wu70

R9 [0 ~ 7] Select which of the Port 7 pins are to be defined to wake-up the MCU from sleep
mode. When the state of the selected pins changes during sleep mode, the
MCU will wake-up and execute the next instruction automatically.
1: Disable the wake-up function
0: Enable the wake-up function

RA (High Pattern Counter Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
HP.7	HP.6	HP.5	HP.4	HP.3	HP.2	HP.1	HP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0),
the PDA function is disabled. RA register is also used as a general-purpose register.

RB (Low Pattern Counter Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
LP.7	LP.6	LP.5	LP.4	LP.3	LP.2	LP.1	LP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0),
the PDA function is disabled. RB register is also used as a general-purpose register.

RC (USB Application Status Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
EP0_W	EP0_R	EP1_R	0	Device_Resume	Host_Suspend	EP0_Busy	Stall

RC [0] Stall flag. When MCU receives an unsupported command or invalid parameters
from host, this bit will be set to 1 by the firmware to notify the UDC to return a
STALL handshake. When a successful SETUP transaction is received, this bit is
cleared automatically. This bit is both readable and writable.

RC [1] EP0 Busy flag. When this bit is equal to "1," it indicates that the UDC is writing
data into the EP0'FIFO or reading data from it. During this time, the firmware will
avoid accessing the FIFO until UDC finishes writing or reading. This bit is only
readable.

RC [2] Host Suspend flag. If this bit is equal to 1, it indicates that USB bus has no traffic for the specified period of 3.0 ms. This bit will also be cleared automatically when a bus activity takes place. This bit is only readable.

RC [3] Device Resume flag. This bit is set by firmware to general a signal to wake-up the USB host and is cleared as soon as the USB Suspend signal becomes low. This bit can only be set by firmware and cleared by the hardware.

RC [4] Undefined Register. The default value is 0.

RC [5,6] EP0_R / EP1_R flag. These two bits inform the UDC to read the data written by firmware from the FIFO. Then the UDC sends the data to the host automatically. After UDC finishes reading the data from the FIFO, this bit is cleared automatically.

Therefore, before writing data into the FIFO, the firmware will first check this bit to prevent overwriting the existing data. These two bits can only be set by the firmware and cleared by the hardware.

RC [7] EP0_W flag. After the UDC completes writing data to the FIFO, this bit will be set automatically. The firmware will clear it as soon as it gets the data from EP0's FIFO. Only when this bit is cleared that the UDC will be able to write a new data into the FIFO.

Therefore, before the firmware can write a data into the FIFO, this bit must first be set by the firmware to prevent UDC from writing data at the same time. This bit is both readable and writable.

RD (USB Application FIFO Address Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	0	0	UAD4	UAD3	UAD2	UAD1	UAD0

RD [0~4]   USB Application FIFO address registers. These five bits are the address pointer of USB Application FIFO.

RD [5~7]   Undefined registers. The default value is zero.

RE (USB Application FIFO Data Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0

RE (USB Application FIFO data register) contains the data in the register of which address is pointed by RD.

RF (Interrupt Status Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Low Signal_IF	High Signal_IF	Port 5 State Change_IF	USB Host Resume_IF	USB Reset_IF	USB Suspend_IF	EP0_IF	TCC_IF

RF [0]   TCC Overflow interrupt flag. It will be set while TCC overflows, and is cleared by the firmware.

RF [1]   EndPoint Zero interrupt flag. It will be set when the EM78M612 receives Vender /Customer Command to EndPoint Zero. This bit is cleared by the firmware.

RF [2]   USB Suspend interrupt flag. It will be set when the EM78M612 finds the USB Suspend Signal on USB bus. This bit is cleared by the firmware.

RF [3]   USB Reset interrupt flag. It will be set when the host issues the USB Reset signal.

RF [4]   USB Host Resume interrupt flag. It is set only under Dual Clock mode when the USB suspend signal becomes low.

RF [5]   Port 5 State Change interrupt flag. It is set when the Port 5 state changes.

RF [6, 7]   High/Low signal Counter interrupt flag. These two flags are used for pattern detecting application.

R10~R1F are General purpose registers. These registers can be used no matter what Bank Selector is. There are 3 banks(BK0~BK2) **R20~R3F** General purpose registers, Select by R4 [6 7].

8.2.1.2 Operation Registers in Bank 1

The special purpose registers for special operation (R8S~RES), are located in Special Purpose Register Bank 1. To access these registers, bank selector (R3[7]) must be set first. These Bank 1 located registers serve special functions, such as; E^{2}PROM, Plus Width Modulation, and Analog to Digital Converter. These registers and special functions are described in details in Sections 8.2.3, 8.9, and 8.10 respectively in this specification.

R8S (PWM1 Duty Cycle Register) Default Value：(0B_0000_0000)

A specified values keeps the output of PWM1 stay at high in a Period.

R9S (PWM2 Duty Cycle Register) Default Value：(0B_0000_0000)

A specified values keeps the output of PWM2 stay at high in a Period.

RAS (AD Channel Select Register) Default Value：(0B_0000_0000)

7	6	5	4	3	2	1	0
ADC	Token_Bit	0	AD4	AD3	AD2	AD1	AD0

RAS [0]~[4]:AD Channel Selector

AD4	AD3	AD2	AD1	AD0	Channel	I/O Port
0	0	0	0	0	Disable AD	-
0	0	0	0	1	1	Reserved
0	0	0	1	0	2	P61
0	0	0	1	1	3	P62
0	0	1	0	0	4	P63
0	0	1	0	1	5	P64
0	0	1	1	0	6	P65
0	0	1	1	1	7	P66
0	1	0	0	0	8	P67
0	1	0	0	1	9	P70
0	1	0	1	0	10	P71
0	1	0	1	1	11	P72
0	1	1	0	0	12	P73
0	1	1	0	1	13	P74
0	1	1	1	0	14	P75
0	1	1	1	1	15	P76
1	0	0	0	0	16	P77

RAS [6]   Token_Bit will be latched to high by hardware when USB bus is transferring token packet.   This bit reset by firmware only.

RAS [7]   AD Converter ready flag.

0->1：Start AD Converting.(Bit set by Firmware)

1->0： When AD finish Converting and moving digital data into AD Data Register , this bit is Clear by Hardware.

P.S.: Hardware enable this function only at AD Channel Selector on the functional I/O port.

RBS (AD MSB Data Register)   AD Digital Data MSB 8 bits

7	6	5	4	3	2	1	0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2

This Register is Read only.

RCS (AD LSB Data Register)   AD Digital Data LSB 2 bits

7	6	5	4	3	2	1	0
Bit 1	Bit 0	-	-	-	-	-	-

This Register is Read only.

RES (EEPROM Mode Select Register)   Default Value (0B_0000_0000)

Command Value	Action	Execution Time
0B_0000_0000	Read	1ms
0B_0000_0001	Write	9ms
0B_0000_0010	Erase	128ms
0B_0000_0011	Disable	N.A.

8.2.1.3 Control Registers in Bank 0

Special purpose registers for special control purposes are also available. Except for the Accumulator (A), these registers must be read and written by special instructions. One of these registers, CONT, can only be read by the instruction "CONTR" and written by "CONTW" instruction. The remaining special control registers can be read by the instruction "IOR" and written by the instruction "IOW."

The following paragraphs only describe the general functions of the control registers. For more detailed description, refer to Sections 8.8 to 8.10 of this spec.

A (Accumulator Register)

The accumulator is an 8-bit register that holds operands and results of arithmetic calculations. It is not addressable.

CONT (Control Register)   *Default Value: (0B_0011_1111)*

7	6	5	4	3	2	1	0
0	/INT	TSR2	TSR1	TSR0	PSR2	PSR1	PSR0

[NOTE] The CONT register can be read by the instruction "CONTR" and written by the instruction "CONTW."

CONT [0~2]   WatchDog Timer prescaler bits. These three bits are used as the prescaler of WatchDog Timer.

CONT [3~5]   TCC Timer prescaler bits.

The relationship between the prescaler value and these bits are as shown below:

PSR2/TSR2	PSR1/TSR1	PSR0/TSR0	TCC Rate	WDT Rate
0	0	0	1: 2	1: 1
0	0	1	1: 4	1: 2
0	1	0	1: 8	1: 4
0	1	1	1: 16	1: 8
1	0	0	1: 32	1: 16
1	0	1	1: 64	1: 32
1	1	0	1: 128	1: 64
1	1	1	1: 256	1: 128

CONT [6]   Interrupt enable control bit. This bit toggles Interrupt function between enable and disable. It is set to 1 by the interrupt disable instruction "DISI" and reset by the interrupt enable instructions "ENI" or "RETI."

> 0: Enable the Interrupt function.
> 1: Disable the Interrupt function.

CONT [7]   Undefined register. The default value is one.

IOC5 ~IOC7 (I/O Port [Port 5 ~ Port 7] Direction Control Registers

Each bit controls the I/O direction of three I/O ports respectively. When these bits are set to 1, the relative I/O pins become input pins. Similarly, the I/O pins becomes outputs when the relative control bits are cleared.

1: Input direction.
0: Output direction.

IOC5 (Data Line I/O Control Register)   *Default Value: (0B_0000_0011)*

7	6	5	4	3	2	1	0
0	0	0	0	0	0	I/O	I/O

IOC5 [2~7]   Undefined registers. The default value is 0.

IOC6 (Port 6 I/O Control Register)   *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
P67	P66	P65	P64	P63	P62	P61	1

IOC6 [0]   This bit is always 1. This is because P60 can only be used as an input pin.

IOC7 (Port 7 I/O Control Register)   *Default Value: (0B_1111_1111)*

7	6	5	4	3	2	1	0
P77	P76	P75	P74	P73	P72	P71	P70

IOC8 (Sink Current Control Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	0	Sink1.1	Sink1.0	0	0	Sink0.1	Sink0.0

IOC8 [0,1][4,5] are P70/P71 sink current control registers. Four levels are offered for selection:

Sink0.1/1.1	Sink0.0/1.0	Sink Current
0	0	3mA±10%
0	1	6mA±10%
1	0	12mA±10%
1	1	30mA±10%

The default current after Power-on reset is 3mA.

IOC9 (Pattern Detecting Application Control Register) Default Value：(0B_0111_0000)

7	6	5	4	3	2	1	0
0	Sample Time.2	Sample Time.1	Sample Time.0	0	DB.2	DB.1	DB.0

IOC9 [0~2] Deboucing control registers. This is used for Pattern Detecting Application.

There are seven degrees available to debounce the input signal noise.

IOC9 [4~6] Sample time selection registers. This is used for Pattern Detecting Application.

The default value is 111.

Sample Time.2	Sample Time.1	Sample Time.0	Sample Rate (Divide the frequency of external oscillator by)
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	÷ 128

IOC9[3&7] Undefined register. The default value is Zero.

IOCA (Operation Mode Control Register)   *Default Value: (0B_1100_0000)*

7	6	5	4	3	2	1	0
Dual_Frq.1	Dual_Frq.0	0	0	0	0	PS/2	USB

IOCA [0,1]   These two bits are used to select the operation mode. EM78M612 can auto-detect the type of port device being attached. After identifying the port, the firmware will set these two bits to enter into a proper operation mode. The definition of these two control registers is described in the table below.

IOCA[1]	IOCA[0]	Operation Mode
0	0	Detect Mode
0	1	USB Mode
1	0	PS/2 Mode
1	1	USB Test Mode

IOCA [2~5]   Undefined registers. The default value is 0.

IOCA [6,7]   Select the operation frequency in Dual Clock mode. Four frequencies are available and can be chosen as Dual Clock mode for running the MCU program.

Dual_Frq.1	Dual_Frq.0	Frequency
0	0	500Hz
0	1	4kHz
1	0	32kHz
1	1	256kHz

IOCB (Port 6 Pull-Low Control Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
PL67	PL66	PL65	PL64	PL63	PL62	PL61	-

IOCB [0~7]   Select whether the 15K Ohm pull-low resistor of Port 6 individual pin is connected or not.

1: Enable the pull-low function.
0: Disable the pull-low function.
P60 without Pull low Resistor.

IOCC (Port 6 Pull-High Control Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
PH67	PH66	PH65	PH64	PH63	PH62	PH61	-

IOCC [0~7]   Select whether the 200K Ohm pull-high resistor of Port 6 individual pin is connected or not.

1: Enable the pull-high function.

0: Disable the pull-high function.

P60 without Pull high Resistor

IOCD (Port 7 Pull-High Control Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
PH77	PH76	PH75	PH74	PH73	PH72	PH71	PH70

IOCD [0~7]   Select whether the 200K Ohm pull-high resistor of Port 7 individual pin is connected or not.

1: Enable the pull-high function.

0: Disable the pull-high function.

IOCE (Special Function Control Register)   *Default Value: (0B_1111_0000)*

7	6	5	4	3	2	1	0
/Dual clock	/WUE	WTE	RUN	0	PDA	NA	NA

IOCE [2]   Pattern Detecting Application Enable Bit. This bit enables the Pattern Detecting function which is used in the Serial Signal Transmission. When this feature is enabled, P60 becomes a serial input pin allowing one pattern detecting block, a counter, and two comparators to function.

1: enable

0: Disable

IOCE [3]   Undefined register. The default value is zero.

IOCE [4]   Run bit. This bit can be cleared by the firmware and set during power-on, or by the hardware at the falling edge of wake-up signal. When this bit is cleared, the clock system is disabled and the MCU enters into power down mode. At the transition of wake-up signal from high to low, this bit is set to enable the clock system.

1: Run mode. The EM78M612 is working normally.

0: Sleep mode. The EM78M612 is in power down mode.

IOCE [5]   WatchDog Timer enable bit. The bit disable/enables the WatchDog Timer.

1: Enable WDT.

0: Disable WDT.

[NOTE] If the Code Option WTC bit is "0," WDT is always disabled.

IOCE [6]   Enable the wake-up function as triggered by port-change. This bit is set by UDC.

1: Disable the wake-up function.

0: Enable the wake-up function.

IOCE [7]　　Dual clock Control bit. This bit is used to select the frequency of system clock. When this bit is cleared, the MCU will run on very low frequency save power and the UDC will stop working.

　　　　　　1: Selects EM78M612 to run on normal frequency.
　　　　　　0: Selects to run on slow frequency.

IOCF (Interrupt Mask Register)　　　*Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Low Signal_IE	High Signal _IE	Port 5 State Change_IE	USB Host Resume_IE	USB Reset_IE	USB Suspend_IE	EP0_IE	TCC_IE

IOCF [0~7]　TCC / EP0 / USB Suspend / USB Reset / USB Host Resume / Port 5 State Change / High Signal / Low Signal interrupt enable bits. These eight bits respectively control the function of TCC interrupt, EP0 interrupt, USB Suspend interrupt, USB Reset interrupt, USB Host Resume interrupt, Port5 State Change interrupt, High pattern counter interrupt and Low pattern counter interrupt. Individual interrupt is enabled by setting its associated control bit in the IOCF to "1".

　　　　　　1: Enable Interrupt.
　　　　　　0: Disable Interrupt.

Only when the global interrupt is enabled by the ENI instruction that the individual interrupt will work. After DISI instruction, any interrupt will not work even if the respective control bits of IOCF are set to 1.

The USB Host Resume Interrupt works only under Dual clock mode. This is because when the MCU is under sleep mode, it will be waked up by the UDC Resume signal automatically.

8.2.1.4 Control Registers in Bank 1

Bank 1 offers more of the special purpose control registers. To write or read these registers, the bank selector (R3[7]) must be initially set to 1. For more detailed description of these registers, refer to Sections 8.8 to 8.10 of this spec.

IOC8S (PWM Control Register)   Default Value：(0B_0000_0111)

7	6	5	4	3	2	3	2
PEN2	PEN1	-	-	-	PS2	PS1	PS0

IOC8S [0~2] PWM Clock Prescaler

Fosc = 6MHz (No matter Xtal is 6MHz or 12MHz)

PS2	PS1	PS0	Clock(Hz)	Period/255
0	0	0	Fosc/3	0.5us
0	0	1	Fosc/6	1us
0	1	0	Fosc/12	2us
0	1	1	Fosc/24	4us
1	0	0	Fosc/48	8us
1	0	1	Fosc/96	16us
1	1	0	Fosc/192	32us
1	1	1	Fosc/384	64us

IOC8S [6] PWM1 Enable Bit

   0:Disable

   1:Enable

IOC8S [7] PWM2 Enable Bit

   0:Disable.

   1:Enable

IOCAS (AD Control Register) Default Value：(0B_0000_0000)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	ADPS1	ADPS0

IOCAS [0,1]:AD Clock Prescaler

ADPS1	ADPS0	AD Clock Source	Conversion Rate
0	0	RC	20K
0	1	RC/2	10K
1	0	RC/4	5K
1	1	RC/8	2.5K

8.2.2 USB Application FIFOs

For USB Application, EM78M612 provides an 8-byte First-In-First-Out (FIFO) buffer for each endpoint. The buffer cannot be accessed directly. However, a corresponding Data Byte Pointer register for each endpoint is made available to address the individual byte of the FIFO buffer. The content of the individual byte will map to a special register.

8.2.3 E^{2}PROM

Four bytes of E^{2}PROM are located in the IOCC ~ IOCF of control register Bank 1. The stored data of E^{2}PROM are not erased when the power is off and can be read and rewritten by firmware. In some special case of applications, for example, cordless mouse controller, E^{2}PROM can store important data, such as the cordless mouse's device identification number.

A control register, RES (address **:** 0x0E in Bank1) controls the E^{2}PROM, that is, to read, write, or to erase the data from E^{2}PROM. Writing a command into this register will execute an action to E^{2}PROM. The command value is defined in the following table. Note that there is an execution time lapse for each command. Before writing the next command into the control register, allow enough time for the E^{2}PROM to finish processing the previous command.

Command Value	Action	Execution Time
0B_0000_0000	Read	1ms
0B_0000_0001	Write	9ms
0B_0000_0010	Erase	128ms
0B_0000_0011	Disable	N/A

8.3 I/O Ports

The EM78M612 has up to fifteen General Purposes I/O pins, which are classifies into two port groups; Port 6 and Port 7. Each pin has an internal resistor that can be individually selected by user. Notice that Pin 60 is a input only pin.The following describes the important features of EM78M612 I/O pins.

8.3.1 Programmable Large Current

Port 7 has two pins; P70 and P71 that can drive large current of up to 30mA. The range of driving current is from 3mA to 30mA, which is programmable. Use IOC8 [0,1] and IOC8 [4,5] to control the sink current of P70/P71. The default current is 3mA.

8.3.2 Wakeup by Port Change Function

Each of the GPIO pins in Port 6 and Port 7 can wakeup the MCU through signal change from input pin. This function is used to wake-up the MCU automatically from sleep mode. It also supports the remote wake-up function for USB application.

Any of the Individual pins of Port 6 and Port 7 can be defined to wakeup the MCU by setting their respective bits, R8 and R9.

8.4 USB Application

EM78M612 is specially designed for USB device application and has many powerful functions that help the firmware to free itself from complex situation in various aspects of USB application.

8.4.1 Auto-Detect PS/2 or USB Mode

When the EM78M612 is connected to the bus, it will auto-detect and identify which type of bus (USB or PS/2) it is connected to. The conditions that influence auto-detect function are described below**:**

1. After a Power-on reset, the initial value of IOCA [0,1] is 0b00. Thus the operation mode is "Detect mode" and the D+ and D- I/O pins are internal pulled high by 200K Ohm to V_{DD}.

2. The firmware checks the state of R5 [0,1]. If the state with which these two bits is 0x00, set the IOCA [0] to "1" to define the "USB mode." Otherwise, set the IOCA [1] to "1," to define "PS/2 mode."

3. When the operation mode is defined as "USB mode," the D- I/O pin is internal pulled high by a 1.5K Ohm resistor to 3.3V, which is output from a built-in regulator.

4. If the operation mode is in "PS/2 mode," both of the PS/2 interface I/O pins are internal pulled high by a 4.7K Ohm resistor to V_{DD}.

{NOTE] If the auto-detect function is not used, the firmware should set the operation mode, either in USB mode or PS/2 mode, at the beginning of program.

An additional mode, "USB Test Mode" is also available. This mode has no load on D+ and D- I/O pins, and can only be used in USB Application case. Therefore, an external 1.5K Ohm resistor is needed to pull up D- I/O pin to 3.3V.

Under "PS/2 mode," both PS/2 pins are programmed to generate an interrupt. After setting the Port 5 State change to Interrupt Enable bit, the MCU will interrupt while the state of these two pins changes.

8.4.2 USB Device Controller

The USB Device Controller (UDC) built-in in the EM78M612 can interpret the USB Standard Command and response automatically without involving firmware. The embedded Series Interface Engine (SIE) handles the serialization and deserialization of actual USB transmission. Thus, a developer can concentrate his efforts more in perfecting the device actual functions and spend less energy in dealing with USB transaction.

The UDC handles and decodes most Standard USB commands defined in the USB Specification Rev1.1. If UDC receives an unsupported command, it will set a flag to notify MCU the receipt of such command. The Standard Commands that EM78M612 supports includes; **Clear Feature**, **Get Configuration**, **Get Interface**, **Get Status**, **Set Address**, **Set Configuration**, **Set Feature, and Set Interface**.

Each time UDC receives a USB command, it writes the command into EP0's FIFO. Only when it receives unsupported command that the UDC will notify the MCU through interrupt.

Therefore, EM78M612 is very flexible under USB application because the developer can freely choose the method of decoding the USB command as dictated by different situation.

8.4.3 Device Address and Endpoints

EM78M612 supports one device address, two endpoints, EP0 for control endpoint, and EP1 for interrupt endpoint. Sending data to USB host in EM78M612 is very easy. Just write data into EP's FIFO, then set flag, and the UDC will handle the rest. It will then confirm that the USB host has received the correct data from EM78M612.

8.5 Reset

The EM78M612 provides three types of reset: (1) Power-on Reset, (2) WatchDog Reset, and (3) USB Reset.

8.5.1 Power-On Reset

Power-on Reset occurs when the device is attached to power and a reset signal is initiated. The signal will last until the MCU becomes stable. After a Power-on Reset, the MCU enters into following predetermined states (see below), and then, it is ready to execute the program.

a. The program counter is cleared.
b. The TCC timer and WatchDog timer are cleared.
c. Special registers and Special Control registers are all set to initial value.

The MCU also has a low voltage detector that detects low output power condition. Whenever the output voltage of the 3.3V regulator decreases to below 2.2V, a reset signal is set off.

8.5.2 WatchDog Reset

When the WatchDog timer overflows, it causes the WatchDog to reset. After it resets, the program is executed from the beginning and some registers will be reset. The UDC however, remains unaffected.

8.5.3 USB Reset

When UDC detects a USB Reset signal on USB Bus, it interrupts the MCU, then proceed to perform the specified process that follows.

8.6 Power Saving Mode

The EM78M612 provides two options of power saving modes for energy conservation, i.e., Power Down mode, and Dual Clock mode.

8.6.1 Power Down Mode

The EM78M612 enters into Power Down mode by clearing the RUN register (IOCE[4]). During this mode, the oscillator is turned off and the MCU goes to sleep. It will wake up when signal from USB host is resumed, or when the WatchDog resets, or the input port state changes.

If the MCU wakes up when I/O port status changes, I/O port direction should be set at input, then the port state is read. For example**:**

```
           :
           // Set the Port 6 to input port
   MOV     A , 0XFF
   IOW     PORT6
           // Read the state of Port 6
   MOV     PORT6, PORT6
           // Clear the RUN bit
   IOR     0XE
   AND     A , 0B11101111
   IOW     0XE
           :
           :
```

If the MCU is awaken by a USB Resume signal, the next instruction will be executed, and one flag, RC[3] will be set to 1.

8.6.2 Dual Clock Mode

The EM78M612 has one internal oscillator for power saving application. Clearing the Bit IOCE [7] will enable the low frequency oscillator. At the same time, the external oscillator will be turned off. Then the MCU will run under very low frequency to conserve power. Four types of frequency are available for selection in setting Bits IOCA [6, 7].

The USB Host Resume Interrupt can only be used in this mode. If this interrupt is enabled, the MCU will be interrupted when the USB Suspend signal is detected on USB Bus.

8.7 Interrupt

The EM78M612 has two interrupt vectors, one is in 0x0001, and the other is in 0x000A. When an interrupt occurs while the MCU is running, it will jump to the interrupt vector (0x0001 or 0x000A) and execute the instructions sequentially from interrupt vector. RF is the interrupt status register that records the interrupt status in the relative flags/bits.

The interrupt condition could be one of the following**:**

1. TCC Overflow — When the Timer Clock / Counter Register (R1) overflows, the status flag RF[0] will be set to 1. Its interrupt vector is 0X0001.

2. EP0 Interrupt — When the UDC successfully received a setup transaction from host to EndPoint0, the status flag RF[1] will be set to 1. Its interrupt vector is 0X000A.

3. USB Suspend — When UDC detects a USB Suspend signal on USB bus, the status flag RF[2] will be set to 1. Its interrupt vector is 0X000A.

4. USB Reset — When the UDC detects a USB Reset signal on USB bus, the status flag RF[3] will be set to 1. Its interrupt vector is 0X000A.

5. USB Host Resume — When UDC detects that the USB bus has left the Suspend condition, the status flag RF[4] will be set to 1. Its interrupt vector is 0X000A.

6. Port 5 State Change — When the input signals in Port 5 changes, the status flag RF[5] will be set to 1. Its interrupt vector is 0X0001.

7. High Pattern Detecting Interrupt Conditions — If the Pattern Detecting Application function is enabled, there will be three conditions with which interruption is generated, and the status flag RF[6] is set to 1, Its interrupt vector is 0X0001.

   a) P.60 turns to low, and the Pattern Counter value bigger than RA register value.

   b) P.60 stays at high, and Pattern Counter value equal 0XFF.

   c) P.60 turns to low and Pattern Counter value bigger than 0XFF.

8. Low Pattern Counter Interrupt Conditions   If the Pattern Detecting Application function is enabled, there will be three conditions with which interruption is generated and the status flag RF[7] is set to 1. Its interrupt vector is 0X0001.

    a) P.60 turns to high, and Pattern Counter value bigger than RB register value.

    b) P.60 stays low, and Pattern Counter value equal 0XFF.

    c) P.60 turns to high, and Pattern Counter value bigger than 0XFF.

IOCF is an interrupt mask register which can be set individually bit by bit. While their respective bit is written to 0, the hardware interrupt will inhibit, that is, the EM78M612 will not jump to the interrupt vector to execute instructions. But the interrupt status flags still records the conditions no matter whether the interrupt is masked or not. The interrupt status flags must be cleared by firmware before leaving the interrupt service routine and enabling interrupt.

The global interrupt is enabled by the ENI (RETI) instruction and is disabled by the DISI instruction.

8.8   Pattern Detecting Application (PDA)

8.8.1 Function Description

This function is designed for the serial signal transmission, e.g., the transmission between a wireless device and its receiver box. The EM78M612 has a built-in Pattern Detecting Application block that ensures the EM78M612 supports wireless devices, such as receiver box controller for a wireless mouse.

Pattern Detecting Application (PDA) can calculate the length of one pattern and interrupt the MCU while the serial signal is transiting from high to low (or vise-versa). Then the MCU reads the length value from a specified register.

8.8.2 Control Register

RA (High Pattern Counter Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
HP.7	HP.6	HP.5	HP.4	HP.3	HP.2	HP.1	HP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RA register is also used as a general-purpose register.

RB (Low Pattern Counter Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
LP.7	LP.6	LP.5	LP.4	LP.3	LP.2	LP.1	LP.0

This register is used in pattern detecting application. If this function is disabled (IOCE[2] = 0), the PDA function is disabled. RB register is also used as a general-purpose register.

IOC9 (Pattern Detecting Application Control Register)   Default Value：(0B_0111_0000)

7	6	5	4	3	2	1	0
0	Sample Time.2	Sample Time.1	Sample Time.0	0	DB.2	DB.1	DB.0

IOC9 [0~2] Deboucing　control registers. This is used for Pattern Detecting Application.
There are seven degrees available to debounce the input signal noise.

IOC9 [4~6] Sample time selection registers. This is used for Pattern Detecting Application.
The default value is 111.

Sample Time.2	Sample Time.1	Sample Time.0	Sample Rate (Divide the frequency of external oscillator by)
0	0	0	÷ 1
0	0	1	÷ 2
0	1	0	÷ 4
0	1	1	÷ 8
1	0	0	÷ 16
1	0	1	÷ 32
1	1	0	÷ 64
1	1	1	÷ 128

IOC9[3&7] Undefined register. The default value is Zero.

The PDA includes an enable control bit, an input pin (P60), a prescaler, a Pattern Detecting block, two special register (RA and RB), and two interrupts (high pattern counter interrupt and low pattern counter interrupt).

To use this function, the enable control bit, IOCE[2] has to be set first. Otherwise the P60 will just be treated as an input only pin and the RA/RB as general purpose register.
As long as the IOCE[2] control bit is set to 1 and the P60 is set as input pin, the Pattern

Detecting block will start to sample the P60 input signal and measure the high pulse or low pulse width. After detecting the transition of this signal and debouncing, the value of the counter will be loaded into the RA (if the signal is transiting from high to low) or RB (if the signal is transiting from low to high), and the counter is cleared to start counting from zero.

Two interrupts are supported individually by RA and RB. After the PDA function is enabled (by setting IOCE[2] to 1), a default value is written to the High Pattern counter register and Low Pattern counter register. Then define the corresponding interrupt enable bits (IOCF[6] and IOCF[7]). When the counter value of one "H" pattern is bigger than the RA default value, then the High Pattern Detecting interrupt will be generated. Similarly, if the counter value of one "L" pattern is bigger than the RB default value, the Low Pattern Detecting interrupt will occur. Then, the EM78M612 will be notified that one successful pattern is received from P60.

If these two interrupts are not used, they can be masked. The new counter value of a pattern will still be loaded to the RA and RB. The firmware must be made to poll and determines any changes to the value of these two registers.

The sample clock is programmable with 8 frequencies to choose from.

8.9 Pulse Width Modulation (PWM)

8.9.1 Function Description

In PWM mode, both of PWM1 (P64) and PWM2 (P65) produce up to a 8-bit resolution PWM output. PWM output has a duty cycle and keeps the output high.

The PWM Period is defined as *0xFF * Timer Counter Clock*. The Timer Counter clock source is controlled by Control Register IOC8S. For example; if the Clock source is 1MHz, then the Period will be 255μ seconds.
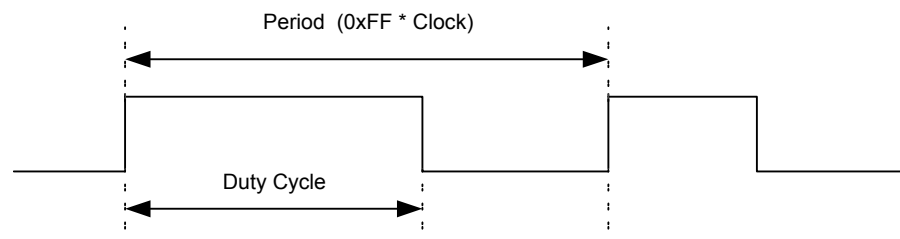
Period = 255 * (1/Timer Counter Clock)

Fig.8.9.2   The PWM Output Timing

The PWM duty cycle is defined by writing to the R8S/R9S Register for PWM1/PWM2.
Duty Cycle = R8S * (1/Timer Counter Clock) for PWM1
R9S * (1/Timer Counter Clock) for PWM2

8.9.2 Control Register

R8S (PWM1 Duty Cycle Register)

A specified value keeps the output of PWM1 to remain at high within a Period.

R9S (PWM2 Duty Cycle Register)

A specified value keeps the output of PWM2 to remain at high within a Period.

IOC8S (PWM Control Register) *Default Value: (0B_0000_0111)*

7	6	5	4	3	2	1	0
PEN2	PEN1	-	-	-	PS2	PS1	PS0

IOC8S [0~2] PWM Clock Prescaler.

Fosc = 6MHz (No matter Xtal is 6MHz or 12MHz)

PS2	PS1	PS0	Clock(Hz)	Period/255
0	0	0	Fosc/3	0.5us
0	0	1	Fosc/6	1us
0	1	0	Fosc/12	2us
0	1	1	Fosc/24	4us
1	0	0	Fosc/48	8us
1	0	1	Fosc/96	16us
1	1	0	Fosc/192	32us
1	1	1	Fosc/384	64us

IOC8S [6,7] PWM1/PWM2 Enable Bit

0:Disable

1:Enable

8.10 Analog-To-Digital Converter (ADC)

8.10.1 Function Description

The Analog to Digital converter consists of a 5-bit analog multiplexer, one Control Register (IOCAS), one AD Channel Select Register (RAS), and two data registers (RBS & RCS) for 10-bit resolution

The ADC module utilizes successive approximation to convert the unknown analog signal to a digital value. The result is fed to the ADDATA. Input channels are selected by the analog input multiplexer via the ADCS/RAS bits AD0~AD4.

- 10-bit resolution：0x00-00~0xC0-FF (0b11000000-11111111)
- Start (0x00-00)：0 Vref~(1/1024)*Vref
- Full (0xC0-FF)：(1023/1024)*Vref~Vref
- Conversion Rate：2.5K; 5K; 10K; & 20K

8.10.2 Control Register

RAS (AD Channel Select Register) *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
ADC	Token Bit	0	AD4	AD3	AD2	AD1	AD0

RAS [0~4]:AD Channel Selector

AD4	AD3	AD2	AD1	AD0	Channel	I/O Port
0	0	0	0	0	Disable AD	-
0	0	0	0	1	1	Reserved
0	0	0	1	0	2	P61
0	0	0	1	1	3	P62
0	0	1	0	0	4	P63
0	0	1	0	1	5	P64
0	0	1	1	0	6	P65
0	0	1	1	1	7	P66
0	1	0	0	0	8	P67
0	1	0	0	1	9	P70
0	1	0	1	0	10	P71
0	1	0	1	1	11	P72
0	1	1	0	0	12	P73
0	1	1	0	1	13	P74
0	1	1	1	0	14	P75
0	1	1	1	1	15	P76
1	0	0	0	0	16	P77

RAS [6] Token Bit. This bit is asserted when MCU receives or transmits USB transaction.

RAS [7] AD Converter ready flag.

> 0 → 1：Start AD Conversion (Set by firmware).

> 1 → 0：When AD finishes converting and has moved digital data into AD Data Register, this bit will be Cleared by hardware.

[NOTE] Hardware can enable this function only at AD Channel Selector of the functional I/O port. After Power-on reset, the initial value of this register is 0b0000 0000.

RBS (AD MSB Data Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2

AD Digital Data MSB 8 bits.

RCS (AD LSB Data Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
Bit 1	Bit 0	0	0	0	0	0	0

AD Digital Data LSB 2 bits.

IOCAS (AD Control Register)   *Default Value: (0B_0000_0000)*

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADPS1	ADPS0

IOCAS [0,1]**:** AD conversion rate.

          00**:** 256kHz
          01**:** 128kHz
          10**:** 64kHz
          11**:** 32kHz

9 Absolute Maximum Ratings

Symbol	Min	Max	Unit
Temperature under bias	0	70	ºC
Storage temperature	-65	150	ºC
Input voltage	-0.5	6.0	V
Output voltage	-0.5	6.0	V

10 DC Electrical Characteristic

(T = 0ºC ~70ºC, V_{DD}=4.4~5.2V, V_{SS}=0V)

Symble	Parameter	Condition	Min	Type	Max	Unit
3.3V Regulator						
V_{Rag}	Output voltage of 3.3v Regulator	V_{DD} = 4.2V ~ 5.2V	3.0	3.3	3.6	V
V_{ResetL}	Low Power Reset detecting low Voltage			-		V
V_{ResetH}	Low Power Reset detecting high Voltage			-		V
MCU Operation						
I_{IL}	Input Leakage Current for input pins	VIN= V_{DD},VSS	-	-	±1	μA
V_{IHX}	Clock Input High Voltage	OSCI	2.5	-	-	V
V_{ILX}	Clock Input Low Voltage	OSCI	-	-	1.0	V
I_{CC1}	V_{DD} operating supply current – Normal frequency operation mode	Crystal type Freq. = 6MHz Output pins floating	-	-	10	mA
I_{CC2}	V_{DD} operating supply current – Normal frequency operation mode	Crystal type Freq. = 12MHz Output pins floating	-	-	20	mA
I_{SB1}	Operating supply current 1 – Power down mode	All input and I/O pins at V_{DD} Output pins floating WDT disabled	-	-	50	μA
I_{SB2}	Operating supply current 2 – Low frequency mode	RC oscillation type Freq. = 20kHz~50kHz Output pins floating	-	-	200	μA
GPIO Pins						
V_{IH}	Input High Voltage	Port 5		-	-	V
V_{IL}	Input Low Voltage	Port 5	-	-		V
V_{OH}	Output High Voltage (Port5 & Port 6 & P72~P77), OSCO)	I_{Drive} = 5.0mA	2.4	-	-	V
V_{OL}	Output Low Voltage (Port5 & Port 6 & P72~P77, OSCO)	I_{Sink} = 5.0mA	-	-	0.4	V
I_{PH}	Input current with pull-high resister	The input pin with internal pull-high resistor of Port6 or Port7 is connected to V_{SS}.	-	25	-	μA
I_{PL}	Input current with pull-low resister	The input pin with internal pull-low resistor of Port6 is connected to V_{DD}.	-	330	-	μA

USB Interface						
V_{OH}	Static Output High	USB operation Mode	2.8	-	3.6	V
V_{OL}	Static Output Low		-	-	0.3	V
V_{DI}	Differential Input Sensitivity		0.2	-	-	V
V_{CM}	Differential Input Command Mode Range		0.8	-	2.5	V
V_{SE}	Single Ended Receiver Threshold	USB operation Mode	0.8	-	2.0	V
C_{IN}	Transceiver Capacitance		-	-	20	pF
V_{RG}	Output Voltage of Internal Regulator	USB operation Mode	3.0	-	3.6	V
I_{PH}	Input current with pull-high resister (D-)					mA
Programmable Large Current						
I_{Sink1}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 00	-10%	3	+10%	mA
I_{Sink2}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 01	-10%	6	+10%	mA
I_{Sink3}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 10	-10%	12	+10%	mA
I_{Sink4}	P70, P71 Output Sink Current	V_{OUT} = 0.4V, IOC8[0,1] or IOC8[4,5] = 11	-10%	30	+10%	mA
Internal Memory Cycle Time						
T_{ROM}	Endurance of Program ROM	T = 25ºC, V_{pp}=10V, V_{NN}=-10V	1K	-	-	Cycle
T_{EE}	Endurance of E2PROM	T = 25ºC, V_{DD} = 4.4V ~ 5.25V	4K			Cycle

ELAN   MICROELECTRONICS   CORPORATION