Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Title:	Electronic Circuits 1
Course Number:	ELE404
Semester/Year (e.g. F2017)	W2023

Instructor	Prof. Virgilio Valente

Assignment/Lab Number:	Design Project
Assignment/Lab Title:	Amplifier Design Project

Submission Date:	Apr 14th, 2023
Due Date:	Apr 14th, 2023

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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1. Introduction and Objective:

Our objective for this project was to design, simulate, analyze, implement and test a single-supply multistage, inverting transistor amplifier adhering to a set of predetermined specifications. A list of the predetermined specifications is as follows detailed in **Figure 1**:

Specifications

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$;
- No-load voltage gain (at 1 kHz): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10}\%)$;
- Maximum no-load output voltage swing (at 1 kHz): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at 1 kHz and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90}\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at 1 kHz and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at 1 kHz): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (−3dB response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$;
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

Figure 1. Specifications outlined for a design project.

One thing to consider is our designed amplifier must be AC-coupled for the load and the signal source. Coupling of either type is permissible between intermediate stages. In addition to this, our source resistance, $R_{S,}$ is 600 ohms, and our output voltage must be free of distortion.

2. Circuit Under Test:

The included figures display the circuit design used to complete this project via Multisim. Probes were included to get values to verify the specifications were met.

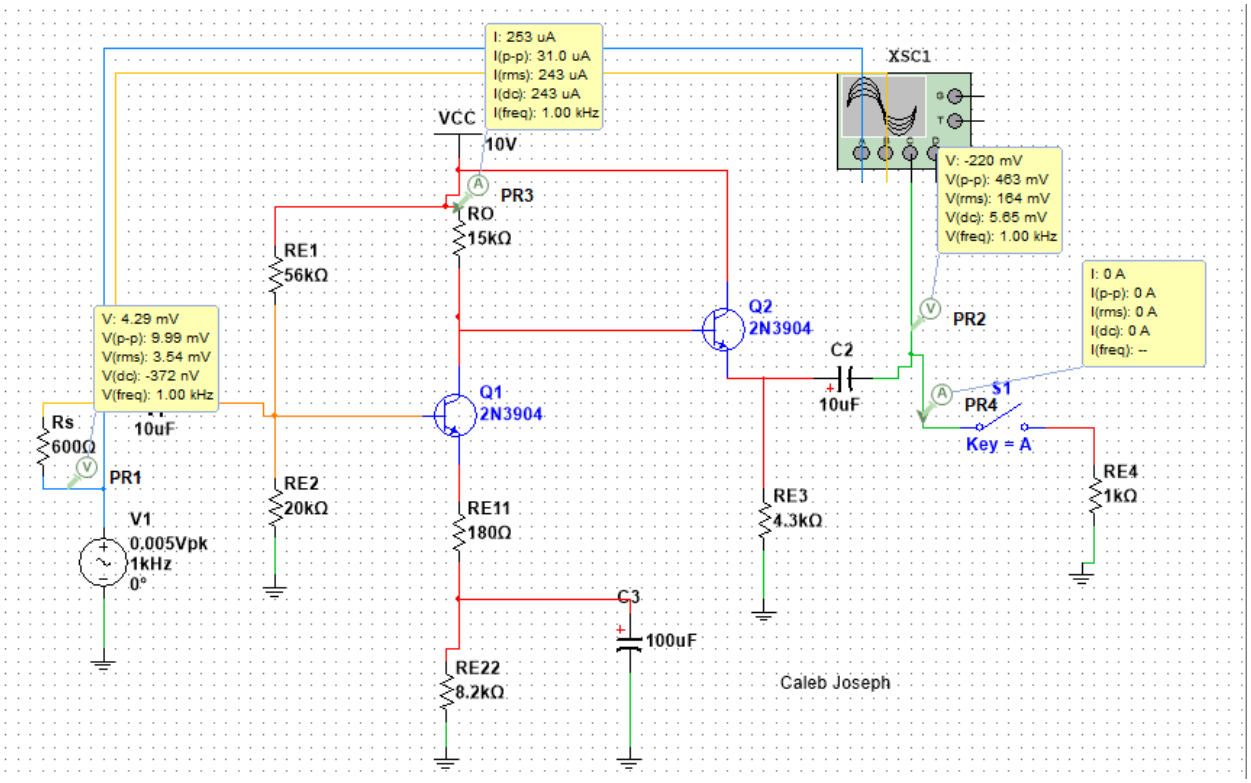


Figure 2. Multisim IDE screenshot of Amplifier Design circuit with no load

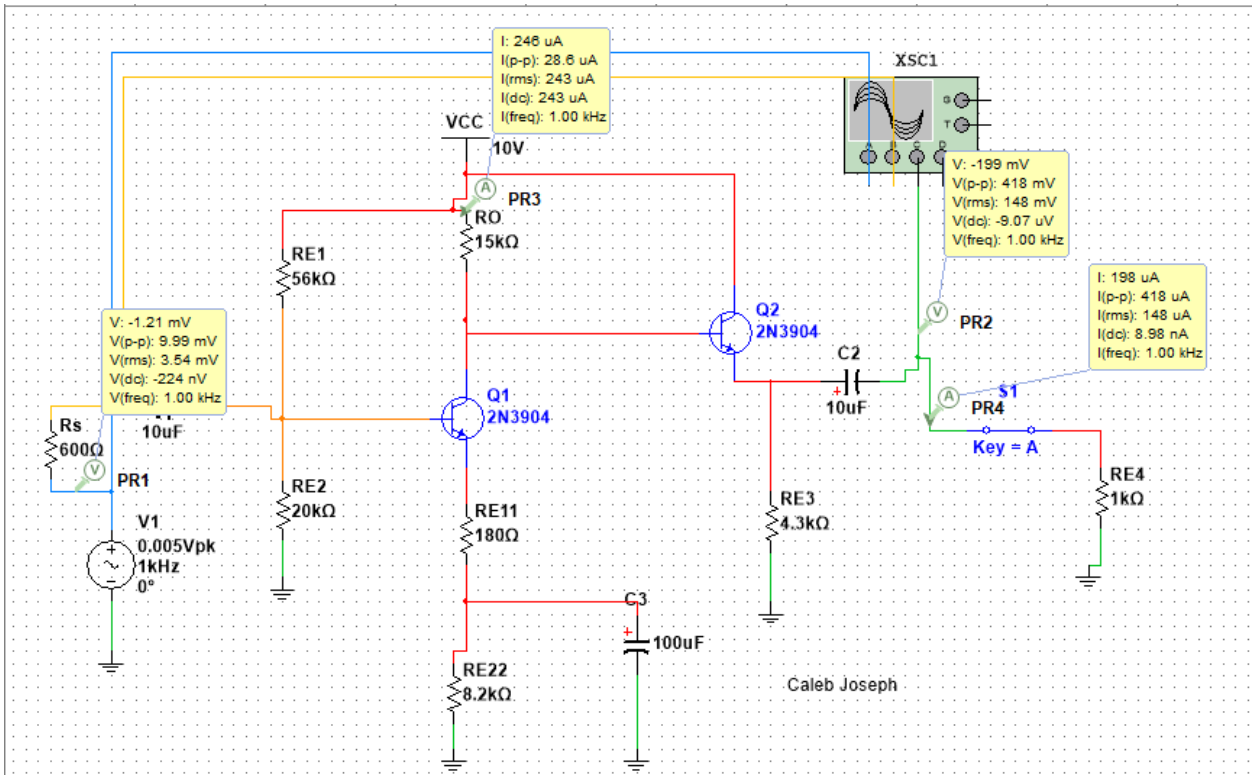


Figure 2.1. Multisim IDE screenshot of Amplifier Design circuit with load

The designed circuit I came up with comprises a CE-CE, as displayed in the Multisim screenshots. Based on the specifications I felt more comfortable working with a common emitter. One thing to note for bias current stability the voltage across the emitter degeneration should be greater than 3 V_{BE}. The common emitter acts as a main amplifier. The common collector manages the high input impedance while driving the gain. This allows the common emitter to behave as expected while minimally affecting the load.

3. Experimental Results:

Graphs were captured to display the transient response after designing the circuit and testing the input and output voltage. Four graphs were produced using a function generator with a 1kHz input with 5mV and 50mV input. The graphs in **Figure 3** experience no clipping with a minimal input voltage of 5mV. The graphs in **Figure 4** experience clipping with an input voltage of 50mV. With an increasing input voltage, there will be more distortion present. Through my tests, I could not produce a non-clipped graph with 8v peak-to-peak and loaded 4V peak-to-peak, respectively.

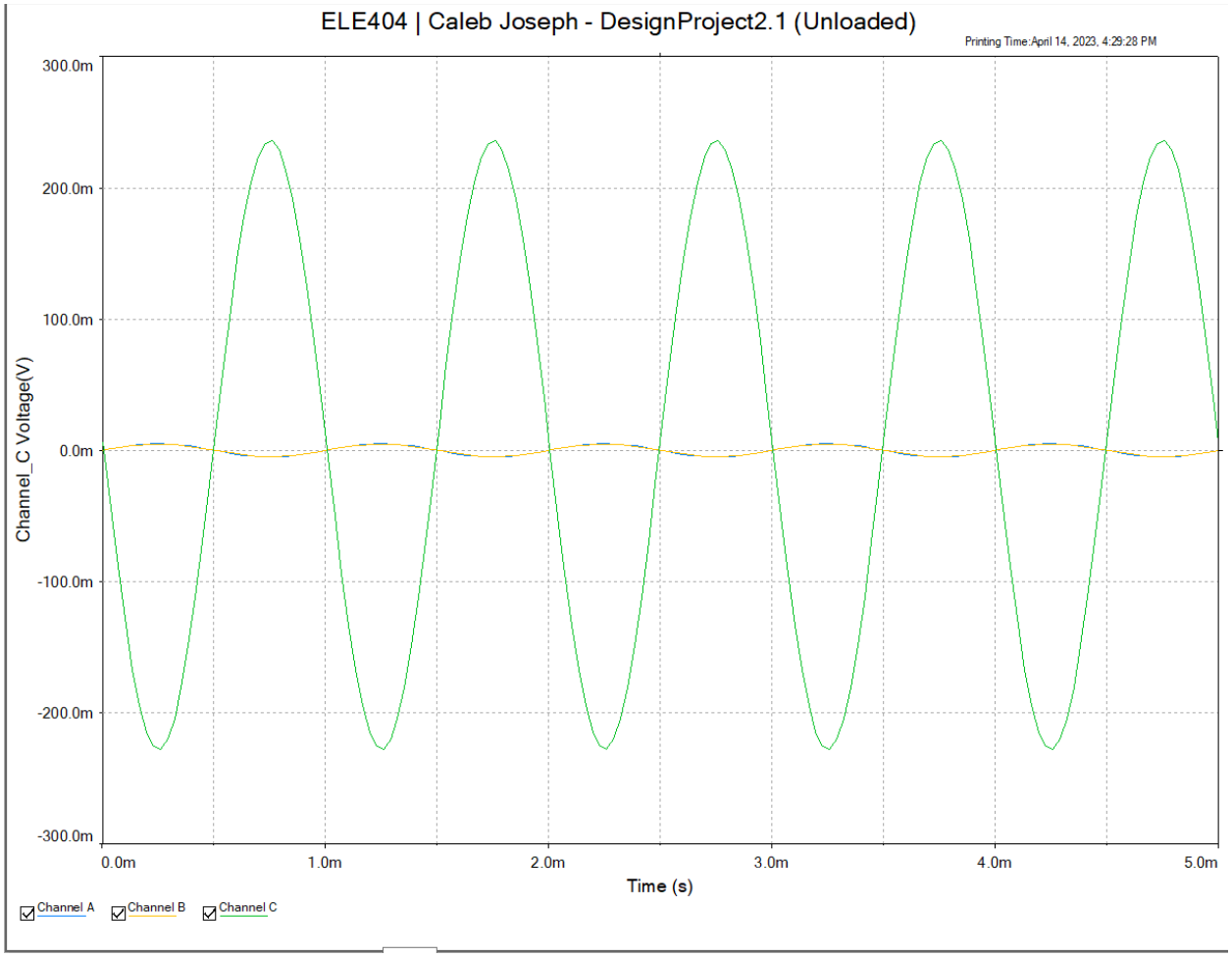


Figure 3.1 Transient graph of 5mV and 1khz Function generator (Unloaded).

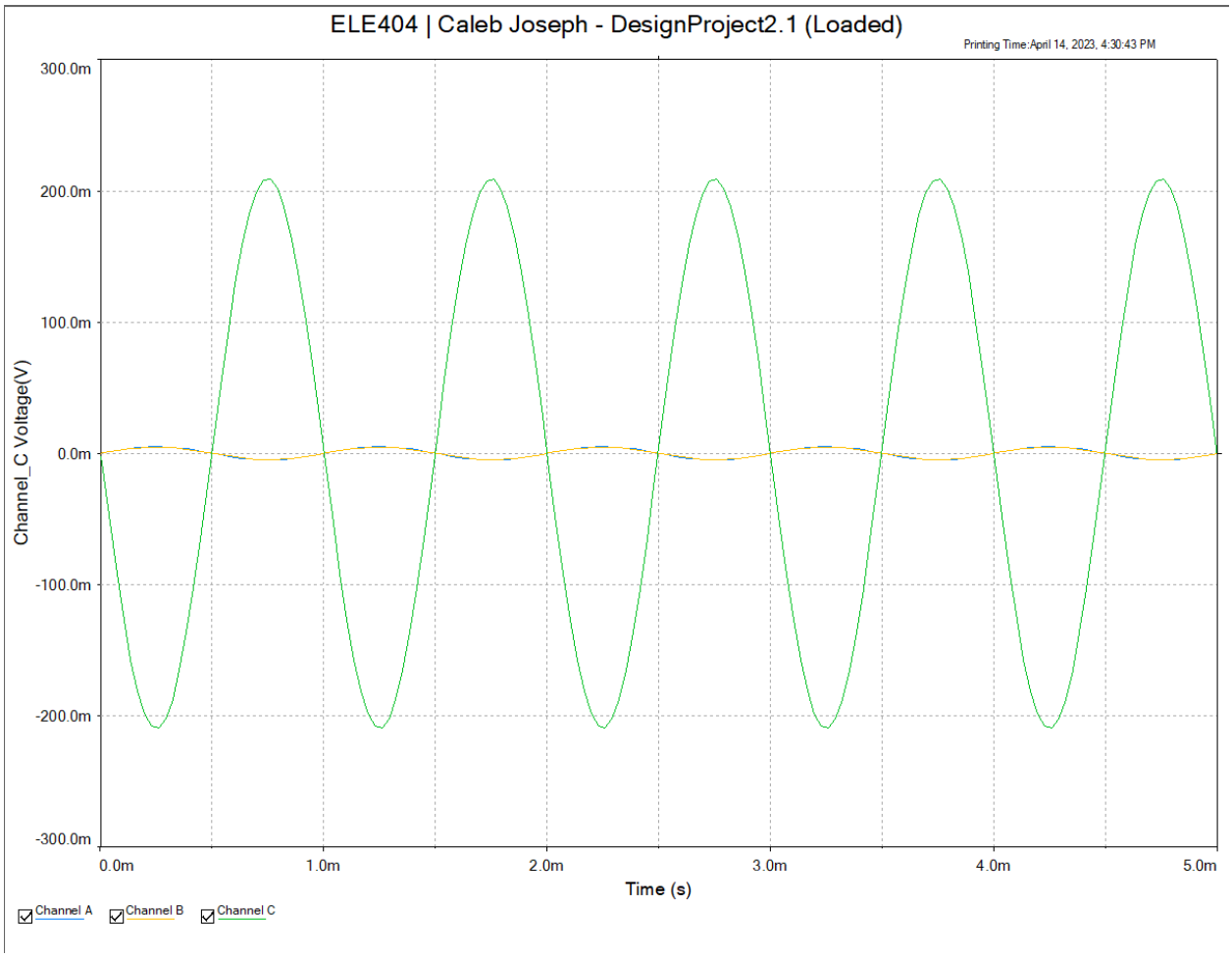


Figure 3.2 Transient graph of 5mV and 1khz Function generator (Loaded).

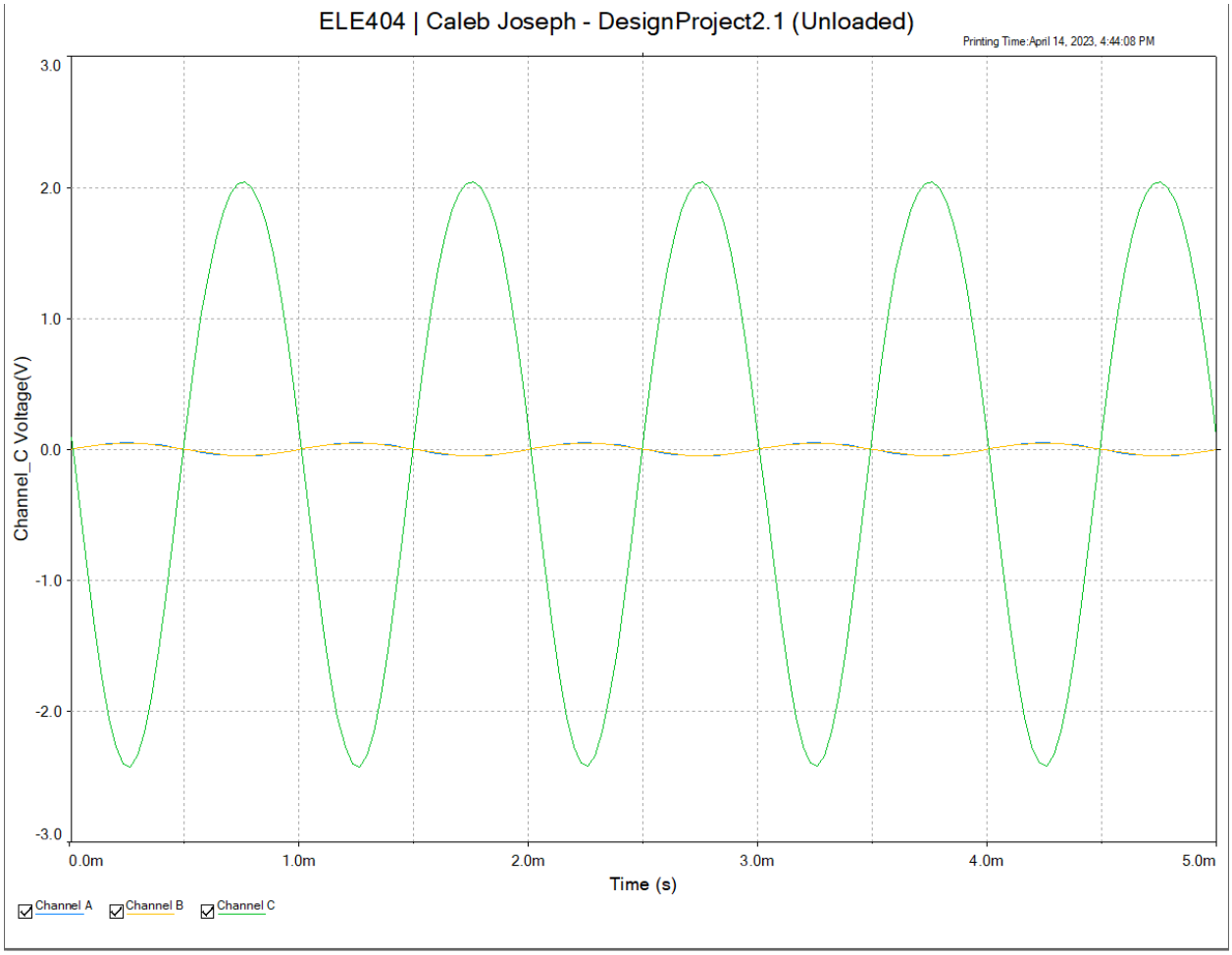


Figure 4.1 Transient graph of 50mV and 1khz Function generator (Unloaded).

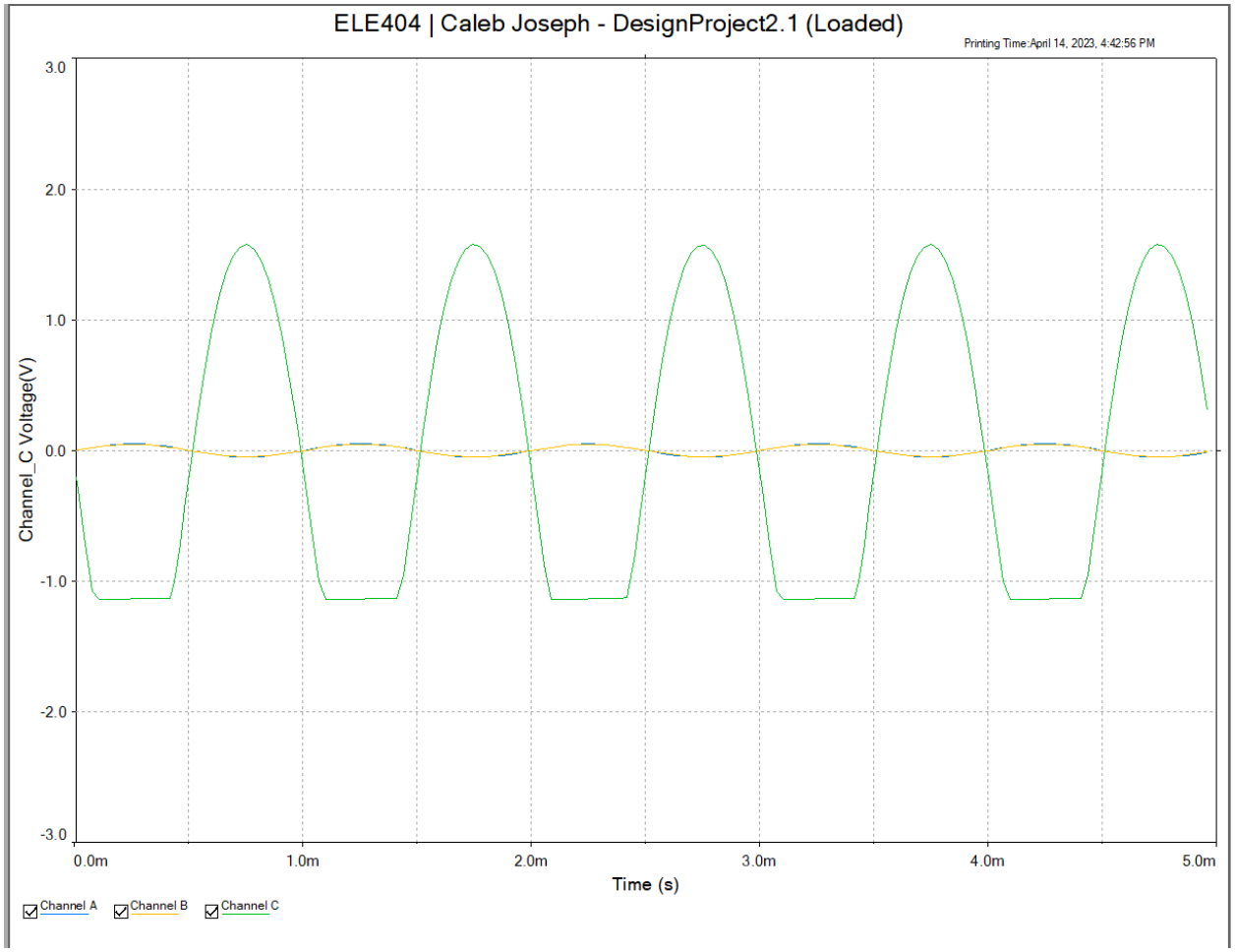


Figure 4.2 Transient graph of 50mV and 1khz Function generator (Loaded).

4. Conclusions and Results:

My reasoning for implementing a CE-CC circuit was because of the simplistic nature of implementation. We have previously worked with and thought of similar implementations through labwork and have been able to have discussions with our TAs to gain a better understanding. The design includes capacitors between each stage and the resistances connected at the base of the transistor. Adjustments were made during calculations to maintain our specified requirement of a gain of 50.

The resistances values selected for the circuit are the following: R_{E1} = 56kΩ, R_{E2} = 20kΩ, R_S = 600Ω, R_C = R_O = 15kΩ, $R_{E1,1}$ = 180Ω, $R_{E2,1}$ = 8.2kΩ, R_{E3} = 4.3kΩ, R_L = 1kΩ. The R_{E1} & R_{E2} values were calculated to meet the requirement of a minimum input resistance of 20kΩ. The 15kΩ value for our R_C affects our voltage gain in the first stage. I chose 15kΩ as it was a permissible value to keep the gain around 50 with the load. The common collector stage was added to combat a low output resistance. The capacitors were added to isolate the output and input bypassing R_E in our first stage. I wanted to block our DC components and short our AC. I

wanted to ensure that our I_{B2} was 20 times smaller than our I_{C1}. Another method would be implementing a DC-blocking capacitor and bias the second stage with another voltage divider.

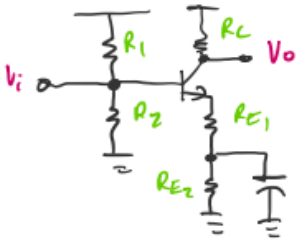
The values calculated during the prelab reflect those in our Multisim circuit. The discrepancy can attest to that around ±1%. Factors such as clipping and voltage swings were specifications I was unable to meet or fully understand. The frequency response was also another point in question.

In summary, my designed circuit implemented a two-stage CE-CC. The measured values resemble the ones used in the Multisim IDE. All subsequent calculations are included in the Appendix.

5. Appendix:

Design #2

Thursday, April 13, 2023 1:05 PM



$V_C = \frac{1}{2}(10 + 2.1 + 0.3) = 6.2V$

$V_E = 3 - 0.7 = 2.1V$

$R_0 = R_C = 15k\Omega = 14k\Omega$

$I_C = \frac{10 - 6.2}{15} = 0.25mA = 0.27$

$I_C = \alpha I_E \Rightarrow \beta = 100 \rightarrow \alpha = 0.99$

$I_E = 0.2475 = 0.2673$

$\rightarrow 2.1 = 0.25(R_{E1} + R_{E2})$

$R_{E1} + R_{E2} = 8.4$ ① $R_{E1} + R_{E2} = 7.77$

AC

$R_i = r_\pi + (\beta+1) R_{E_1}$

↳ $g_m = 40 I_C = 40(0.25)$

$g_m = 10\ mS$

$g_m = 10.8$

$\rightarrow A_{vo} = \frac{-g_m R_L}{1+g_m R_{E_1}} \Rightarrow 50 = \frac{(10)(15)}{1+(10)R_{E_1}}$

From ①; $R_{E_2} = 8.4 - 0.2 = 8.2k\Omega$

↳ $R_{E_1} = 0.2k\Omega$

$R_{E_1} = 0.2074k\Omega$

$R_{in} \geq 20k$; $\geq 20k$

$R_{in} = R_1 // R_2 // R_i \rightarrow R_i = \frac{\beta}{g_m} + (\beta+1)R_{E_1} = \frac{100}{10} + 101(0.2)$

$R_i = 30.2k\Omega = 30.2$

↳ $\frac{1}{20} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{30} \rightarrow R_1 // R_2 \geq \left(\frac{1}{20} - \frac{1}{30}\right)^{-1}$

Let $R_1 // R_2 = 60k$; $45k$

$\rightarrow I_L = \beta I_B \rightarrow I_B = 0.0025mA = 0.0027mA$

Since $R_1 // R_2 = 60 \rightarrow \frac{R_1 R_2}{R_1 + R_2} = 60$ ②

Ignore I_B: $2.8 \geq 10 \cdot \frac{R_2}{R_1 + R_2}$

$\frac{R_1 + R_2}{R_2} = 3.57$ ③

$R_1 = 3.57 R_2$

$R_1 = 3.57 \cdot 57.6050$

Solve ② & ③;

$R_1 = 205.6496\ k\Omega$

$R_2 = 57.6050\ k\Omega$

Check I: $I \geq \frac{10}{205.6496 + 57.6050} = 0.037398$

$I >> I_B$

CC Stage:

$$\frac{0.25}{20} = 0.0125 = I_{B2}$$

$$I_{E2} = (\beta+1) I_{B2}$$
$$= 101(0.0125)$$
$$I_{E2} = 1.2625 \text{ mA}$$

$$\rightarrow R_{E3} = \frac{3.5}{1.2625} = 4.3564$$

$$\rightarrow I_{C2} = \beta I_{B2} = 1.25 \text{mA} \quad \rightarrow g_{m2} = 50 \text{ mS}$$

$$\rightarrow r_{e2} = \frac{1}{g_{m2}} = 0.02 \text{k}\Omega$$

$$\rightarrow R_o = 4.3564 \text{k}\Omega \;//\; \underbrace{\left[0.02 + \frac{1\text{k}}{101}\right]}_{0.1685} = 0.6622 \text{k}\Omega$$

$$R_{i2} = r_{\pi 2} + (\beta+1) R_{E3}$$
$$= \frac{100}{50} + 101 \cdot 4.3564$$
$$= 442\text{k} \quad \text{if} \quad R_L = \infty$$

$$\rightarrow \frac{V_{c1}}{V_i} = \frac{-g_{m1}(R_L // R_{i2})}{1 + g_{m1} R_{E1}} = \frac{-10(15//442)}{1 + 10 \cdot 0.2} = -48.4 \text{ V/V}$$

$$\rightarrow \frac{V_o}{V_{c1}} = \frac{g_{m2} R_{E3}}{1 + g_{m2} R_{E2}} = 0.995 \text{ V/V}$$

$$\rightarrow A_{vo} = \frac{V_o}{V_{c1}} \cdot \frac{V_{c1}}{V_i} = (48.4 \cdot 0.995) = -48.2 \text{ V/V}$$

inverted gain: $\frac{V_{c1}}{V_i} = \frac{-50}{0.995} = -50.3 \text{ V/V}$

-50.3 @ CE

$$\rightarrow -50.3 = \frac{-10(15 \,//\, 442)}{1 + 10 R_{E2}} \Rightarrow \boxed{R_{Eq} = 0.1884\ k\Omega}$$

Then $R_{E2} = 8.4 - 0.1884 \rightarrow \boxed{R_{E2} = 8.2116}$

Change in R_i:

$$R_i = r_\pi + (\beta+1) R_{E1} = \frac{100}{10} + 101 \cdot 0.1884 \quad \boxed{R_i = 29.0284\ k\Omega}$$

Advice $R_{in} \approx 20k\Omega$

$$R_1 \,//\, R_2 \,//\, 29.0284 = 20 \rightarrow R_1 \,//\, R_2 = 15.25\ k\Omega$$

Since ; $V_B = 2.8V \rightarrow 2.8 = 10 \cdot \frac{R_2}{R_1 + R_2}$

$$\boxed{\begin{aligned} R_1 &= 55.3815\ \Omega \\ R_2 &= 21.0449k\Omega \end{aligned}}$$

$$I = \frac{10}{55.3815 + 21.0449}$$

$$I = 0.13mA << 0.25mA$$

Pin1