Caleb Joseph

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Accomplishment Statement

- Jr. Computer Engineering student with Design Verification, Scripting, SystemVerilog, and UVM experience at AMD.
- Continuous learner with passion for ASIC Hardware Design and Verification eager to work on hardware products.
- Implemented a Module-gated Clock-gating script into the power analysis flow, enhancing evaluation efficiency by approximately 20% and streamlining coverage analysis for video IP designs, supporting a team of 70+ engineers.

Education

Bachelor of Engineering, Computer Engineering (Co-op) Sep. 2021 – Apr. 2026 (Exp.)
Toronto Metropolitan University *Toronto, ON*

- **Relevant Courses**: Digital Systems, Computer Architecture, Embedded Systems, Microprocessors, DSA, OOP
- **Affiliations**: National Society of Black Engineers, ColorStack, Career Pathways Program, FEAS

Technical Skills

Languages & Scripting: Python, Verilog, C, C++, VHDL, SystemVerilog, TCL, Perl, Bash/CSH, Cron
Verification Tools & Technologies: UVM, VCS, Verdi, Intel Quartus II, Linux, UNIX, Perforce, Arduino, Git
Other: Verification, Synthesis, Lint, Regression testing, Scripting & Automation, CODEC, RTL, FPGA, SoC, Video IP, CDC

Experience

Design Verification Intern (Video Domain) May 2024 – Present
Advanced Micro Devices (AMD) *Markham, ON*

- Contributing to pre-silicon **video-related IP** verification **regression testing**, learning **SystemVerilog** and **UVM**, ensuring functional coverage and root-causing issues, improving verification completeness by approximately 12%.
- Collaborating with designers to drive **verification** strategies, support **code coverage** and resolve regression issues.
- Automated error tracking and categorization in release **regression** flows using a **Python**-based **script** to generate a custom report with **RegEx**, reducing build failures by about 25%.
- Enhanced automated design flows with **CSH**, **Python**, and **Perl** scripts, achieving a 10% improvement in efficiency.
- Performing **CDC** analysis and verification to ensure reliable data transfer across different clock domains, identifying and reporting potential issues on a subsystem level to enhance design robustness
- Executig **LINT** & **DC-ELAB** runs to verify **RTL** quality, cutting **synthesis** errors by 20% and enhancing readiness.

Information Technology Intern May 2023 – Aug. 2023
Environics Analytics *Toronto, ON*

- Spearheaded donation of **30+** laptops, repurposing **$10,000+** of equipment while gaining expertise in **BIOS**, **OS**, and **drivers**, ensuring data integrity through secure boot and **UEFI**, and showcasing hardware diagnostics skills.

Projects

RTL Design of Round Robin Arbiter | *EDA Playground, SystemVerilog, Verilog, RTL Design* GitHub

- Implemented a 4-request/grant Round Robin Arbiter in **Verilog** with a state machine based scheduling algorithm.
- Constructed a **SystemVerilog** testbench to simulate and validate the design, verifying correct arbitration behavior.

Multi-stage RISC Pipelined Processor | *Altera DE2-115, VHDL, Quartus II, Cyclone-IV EP4CE115F29C7* GitHub

- Constructed a 32-bit 3-stage pipeline **RISC CPU** using **VHDL** on an Altera DE2-115 **FPGA** board with **Intel Quartus II** for synthesis and simulation, achieving a target frequency of >50MHz.
- Designed and simulated a register set, **program counter**, **ALU**, data path, and control unit, ensuring optimized RISC processing and reducing data processing delays by 15%.

Ray Tracing Application | *C, C++, ImGui, Visual Studio, Walnut Framework* GitHub

- Developed a ray tracing application in C++; enhancing the Render class and leveraging multi-threading techniques, reducing render times by 30%, assessing gaming **GPU** acceleration for **CUDA** performance processing uplift.

Professional Development

Program Manager May 2024 – Present
Intern Steering Committee, Advanced Micro Devices (AMD) *Markham, ON*

- Led social events aligned with intern interests, fostering a vibrant community of **200+** interns at the Markham site.
- Assisted in onboarding **30+** interns by organizing key events that enhance career development and community.

Open to relocation. Canadian Citizen.