Caleb Joseph

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Education

Bachelor of Engineering, Computer Engineering (Co-op) Sep. 2021 – Apr. 2026 (Exp.)
Toronto Metropolitan University *Toronto, ON*

- **Relevant Courses**: Digital Systems & Software, Computer Architecture, Electronic Circuits, Data Structures & Algorithms, Embedded Systems & Microprocessors, Object-Oriented Programming (OOP), Solid State Physics
- **Affiliations**: National Society of Black Engineers, ColorStack, Career Pathways Program, FEAS, & IEEE CSTMC

Experience

Design Verification Intern (Video Domain) May 2024 – Present
Advanced Micro Devices (AMD) *Markham, ON*

- Contributing to pre-silicon verification of **video-related IP** using **SystemVerilog** and **UVM**, ensuring full functional coverage and root-causing critical issues, improving verification completeness by 15%.
- Collaborating with **6+** cross-functional teams (architects and design engineers) to implement **verification** strategies and resolve regression issues, reducing build failures by 20%.
- Automated error tracking and categorization in release **regression** flows using a **Python**-based custom report generator with **RegEx**, reducing build failures by 30%.
- Enhanced automated design flows using **CSH**, **TCL**, and **Perl** scripts, achieving a 10% improvement in efficiency.
- Validated **RTL** & **SoC** design functionality through simulations, reducing design errors by 20% before tape-out.
- Performed **FPGA** regressions to validate hardware designs, increasing test coverage by 35%.
- Executed **LINT** & **DC-ELAB** runs to ensure **RTL** quality, cutting **synthesis** errors by 20% and enhancing readiness.

Information Technology Intern May 2023 – Aug. 2023
Environics Analytics *Toronto, ON*

- Spearheaded donation of 30+ laptops, gaining expertise in computer software architecture, including **BIOS**, **OS**, and drivers, while ensuring data integrity via secure boot and **UEFI**, showcasing hardware diagnostics.
- Resolved **firmware** incompatibility for 150+ internal phones using IPv4, achieving annual cost savings of $5,000.

Projects

Multi-stage RISC Pipelined Processor | *Altera DE2-115, VHDL, Quartus II, Cyclone-IV EP4CE115F29C7 FPGA*

- Constructed a 32-bit 3-stage pipeline **RISC CPU** using **VHDL** on an **Altera DE2-115 FPGA** board with **Intel Quartus II** for synthesis and simulation, achieving a target frequency of $>$50MHz.
- Designed and simulated a register set, **program counter**, **ALU**, data path, and control unit, ensuring optimized RISC processing and reducing data processing delays by 15%.

Ray Tracing Application | *C, C++, ImGui, Visual Studio, Walnut Framework*

- Developed a ray tracing application in **C++**, improving performance by optimizing the **Renderer class** and implementing multi-threading techniques, reducing render times by 30%.
- Deployed an interactive ImGui UI for real-time adjustments with the Walnut framework in Visual Studio, assessing gaming & **GPU** acceleration for **CUDA** implementation to enhance performance.

Professional Development

Social Team Program Manager May 2024 – Present
Intern Steering Committee, Advanced Micro Devices (AMD) *Markham, ON*

- Led social events aligned with intern interests, fostering a vibrant community of **200+** interns at the Markham site.
- Assisted in onboarding **30+** interns by organizing key events that enhance career development and community.

Event Support Staff Feb. 2024 – Apr. 2024
FEAS Co-op Office, Toronto Metropolitan University *Toronto, ON*

- Managed registration by checking in **50+** attendees, coordinating name tags, and updating student information, facilitating efficient event flow and attendee tracking.

Technical Skills

Languages & Scripting: Python, C, C++, VHDL, Java, SystemVerilog, Verilog, TCL, Perl, Bash/CSH, Cron
Verification Tools & Technologies: UVM, VCS, Verdi, MATLAB, Intel Quartus II, Linux, UNIX, Perforce, Arduino, Git
Other: ASIC Design, Verification, Validation, RTL, FPGA, Synthesis, SoC, Firmware, Integration

Open to relocation. Canadian Citizen.