

Lab 07: Digital Photo Frame

(Nov. 14, 2019)

Submission deadlines:

Source Code:	18:30, Nov. 26, 2019
Report	23:59, Dec. 1, 2019

Objective

- To be familiar with modeling finite state machines with Verilog.
- To be familiar with the control of VGA Display and other I/Os on the FPGA demo-board.

Action Items

In this lab, you are asked to implement a digital photo frame with some transition effects on the VGA display.

Choose the image you want and use PicTrans.exe to generate your own .coe file (**make sure it is an appropriate image**).

1. (30%) Design a VGA controller that make your image scrolls left or right.

The behavior of the design is explained as follows :

- In the beginning or when pressing the **rst** button, the VGA display will show the image at the origin position.
- When **en** = 1, **dir** = 0, the image scrolls to the left in a column-by-column manner at the frequency of 100MHz divided by 2^{22}



- When **en** = 1, **dir** = 1, the image scrolls to the right in a column-by-column manner at the frequency of 100MHz divided by 2^{22}



- When **en** = 0, the image holds and stops scrolling.

The controller has the following input ports:

input clk,
input rst,
input en,
input dir,

and the following output ports:

output [3:0] vgaRed,
output [3:0] vgaGreen,
output [3:0] vgaBlue,
output hsync,
output vsync,

IO Connection:

clk	connected to W5
rst	connected to U18 (btnC)
dir	connected to V16
en	connected to V17
vgaRed	connected to pin N19, J19, H19, G19
vgaGreen	connected to pin J18, K18, L18, N18
vgaBlue	connected to pin D17, G17, H17, J17
hsync	connected to pin P19
vsync	connected to pin R19

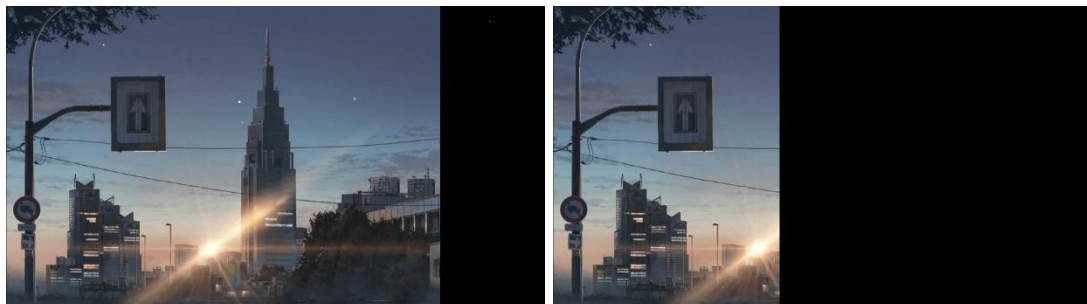
Demo Video:

https://youtu.be/xF6bc_ROIBA

2. (70%) Design a VGA controller with two modes to operate by the corresponding buttons.

The behavior of the design is explained as follows :

- In the beginning or when pressing the **rst** button, the VGA display will show the image at the origin position
- When the button **shift** is pressed, the image disappears from right to left and then the same picture appears from top to bottom.





- When the button **split** is pressed, the image is split into 4 pieces with 4 different directions to shift and disappear. The image will show again after the image completely disappears (after a cycle).
 - a. The top left piece shifts upward.
 - b. The top right piece shifts rightward.
 - c. The bottom right piece shifts leftward.
 - d. The bottom left piece shifts downward.



- When the VGA controller operates in either the shift or split mode, only the **rst** button is effective.

The controller has the following input ports:

input clk,
input rst,
input shift,
input split,

and the following output ports:

output [3:0] vgaRed,
output [3:0] vgaGreen,
output [3:0] vgaBlue,
output hsync,
output vsync,

IO Connection:

clk	connected to W5
rst	connected to U18 (btnC)
shift	connected to T17 (btnR)
split	connected to W19 (btnL)
vgaRed	connected to pin N19, J19, H19, G19
vgaGreen	connected to pin J18, K18, L18, N18
vgaBlue	connected to pin D17, G17, H17, J17
hsync	connected to pin P19
vsync	connected to pin R19

Demo Video:

https://youtu.be/n_S_Jtj8iEQ

Attention:

1. You should hand in the file named **lab07_1.v** and **lab07_2.v** as top module. If you create several modules for your design, upload them all.
2. You should also hand in your report as lab07_report_StudentID.pdf (i.e., lab07_report_105062224.pdf).
3. You should be able to answer questions of this lab from TA during the demo.
4. You need to generate bitstream before demo.