RevE Hardware Interface Control Document

ISIS-ICEPS2-ICD-0003

Version: 1.1

CI Number: N/A

Release Information

	Name	Function	Signature	Date
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Distribution List

Name	Organization	Description
N/A	ISISPACE	Innovative Solutions In Space B.V.

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Change Log

Version	Date	Affects	Description
0.1	2021-12-14	All	First Version of ICD revD
0.2	2021-12-17	All	Review of all pages
0.3	2021-12-20	All	Update of all pages
0.4	2022-02-04	1.3.2, 4.2, 4.3	Added description of J12 Changed revision number to revE
1.0	2022-03-15	-	Documents released
1.1	2022-05-23	Table 3-1	Updated VD3, VD4, VD5 voltage limits. Clarified general specifications.

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Acronyms

Name	Description
ABF	Apply Before Flight
CSKB	CubeSat Kit Bus
DB	Daughter Board
I^2C	Inter-Integrated Circuit
ICEPS	ISIS Compact Electrical Power System
ICD	Interface Control Document
ISIS	Innovative Solution in Space
MCU	Micro Controller Unit
MPPT	Maximum Power Point Tracker
PBP	Power Battery Pack

PBU	Power Battery Unit
PCB	Printed Circuit Board
PCU	Power Conditioning Unit
PDU	Power Distribution Unit
PIU	Power Integrated Unit
PSU	Power Supply
RBF	Remove Before Flight

1 Introduction

The ISIS Compact Electrical Power System version 2 (ICEPS2) is the second-generation minimized volume power system for nanosatellites, specifically targeting space constrained 1U to 3U cubesats, designed and manufactured by Innovative Solutions In Space.

This second-generation system leverages wide bandgap semiconductor technologies, implementing GaN technology to improve solar power conversion efficiency and performance. The EPS is equipped with hardware based Maximum Power Point Tracking (MPPT), voltage and over-current protection. The standard system provides 3.3V and 5V regulated bus voltages as well as a semi-regulated battery bus, distributed across nine load channels. An add-on daughterboard (DB) allows additional load channels, regulated voltages and solar panel inputs to suitably power the system and payload instruments

The system consists of two or three pieces: a PC-104 size mainboard PCB which is called the Integrated Unit (IU), a battery pack (BP) and optionally a daughterboard.

The compact EPS is available in three standard configurations:

- Type A consists of the PIU mainboard with a top-mounted 2-cell battery pack. This type provides around 7.2 V nominal battery bus voltage on the semi-regulated bus and is the smallest and lightest of the three.
- Type B consists of the PIU mainboard with a bottom mounted 4-cell battery pack. This type provides around 14.4 V nominal battery bus voltage for more power demanding applications, at an intermediate volume and weight.
- Type C is as Type B, but also includes a daughter board. This type provides additional switched channels and regulated voltage. This largest of the three options also yields the most in terms of flexibility and versatility at modest volume and weight.

The ISIS Compact EPS version 2 (ICEPS2) is the smaller cousin of the slightly larger ISIS Modular EPS version 2 (IMEPS2). The IMEPS2 is intended for larger or more power intensive satellites above 3U in size.

1.1 Purpose and Scope of Document

This document specifies all hardware interfaces of the system, both electrical and mechanical. Software interfaces are described in a separate software ICD [RD1]. The usage of the system is described in a separate user manual [RD2].

This document is valid until it is declared obsolete or replaced with a succeeding version. Changes with respect to the previous version will be clear from the revision. As this document may be updated without prior notice, it is advised to check the ISIS website http://www.isispace.nl or ask for the latest version at support@isispace.nl before using this document as reference.

1.2 Reference Documents

The table below contains documents that are not fully applicable and will provide supplementary information relevant for the present document.

Table 1-1 Reference Documents

Reference	Name	Version
RD1	ISIS.EPS2.ICD.SW.IVID.7 Software ICD IVID 7	1.2
RD2	ISIS-ICEPS2-MAN-0001-User_Manual	1.9
RD3	ISIS-ICEPS2-OS-0001-ICEPS2_Option_Sheet	2.1

1.3 Revision changes

1.3.1 PIU revC to PIU revD changes

- Functionality
  - Added temperature sensor on PIU (±0.1 °C (maximum) from –20 °C to 50 °C)
- Protection
  - Discharge path load switch added: discharge undervoltage & overcurrent limits
  - Discharge path current clamping, protecting battery from overcurrent in discharge
  - Charge path load switch added: charge undervoltage & overcurrent limits
  - Charge path current clamping, protecting battery from overcurrent in charge
  - Trickle charge path added, providing option for battery resuscitation
- Battery inhibit
  - Independent low side switch added
  - Dependency circuitry added to block high-side connect when low side is not connected
- Interface changes - Umbilical
  - Added option for pullups on the main I2C of the EPS. This is connected to CSKB I2C main (default) or ALT.
  - ABF1 renamed to umbilical 1.
  - Umbilical1 connector size changed from 15- to a 14-pin connector.
  - Umbilical1 pinout restructured.
  - ABF2 renamed to umbilical 2.
- Interface changes - Separation
  - Separation switch connector extended to accommodate for low side switch inhibits. (From 4 pin connector to 6 pin connector)

1.3.2 PIU revD to PIU revE changes

- Interface changes
  - J12 connector added (offers CH[3] and I^2C)

2 System Description

The ICEPS hardware is divided in three parts:

1. Power Battery pack (PBP). This is either a two-cell (2S1P) or a four-cell (4S1P) battery pack.
2. Power Integrated Unit mainboard (PIU)
3. Power Integrated Unit Daughter Board (PIU-DB)

The electronics on the PIU and PIU-DB can also be separated in three sections:

1. Power Conditioning Unit (PCU): Included all electronics interfacing with the solar panels. The electronics are divided over the PIU and PIU-DB.
2. Power Battery Unit (PBU): Includes all electronics interfacing with the battery pack and is located solely on the PIU.
3. Power Distribution Unit (PDU): Includes all electronics interfacing with the satellite and microcontroller. The electronics are divided over the PIU and PIU-DB.

2.1 System Block Diagram

A detailed block diagram of the system is provided in Figure 2-1.

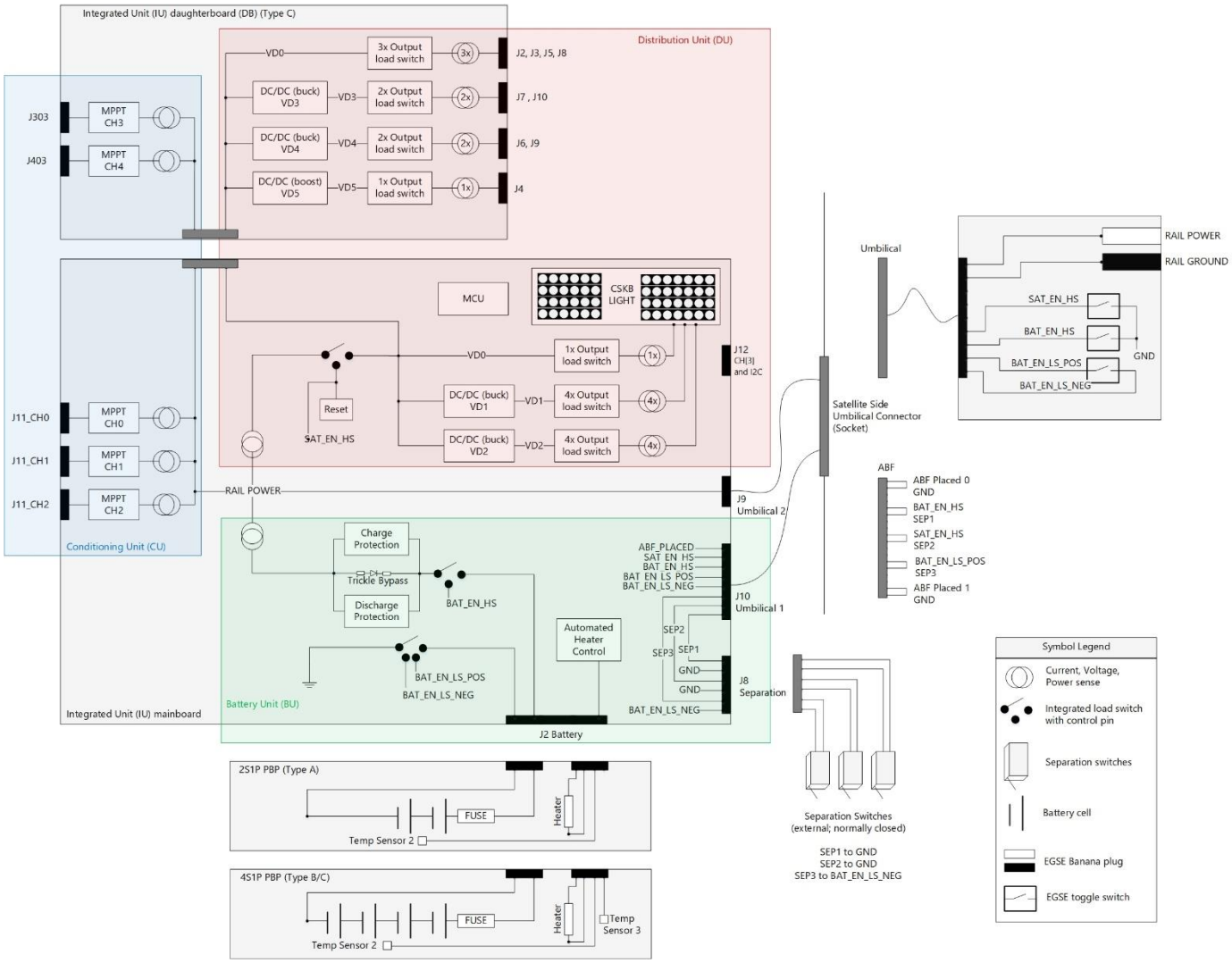


Figure 2-1: Functional Block diagram

2.2 Battery Unit

The PBU allows connecting a battery pack to the RAIL. The functionality of the battery unit consists of:

- a back-to-back (B2B) MOSFET high-side inhibit controlling whether the battery is attached to the RAIL.
- a single MOSFET low side inhibit blocks discharge return currents into the battery when inhibiting.
- independent high and low side inhibit enable controls. A special circuit mechanism introduces a dependency that only allows the high side to connect once the low side is connected. This ensures a proper ground connection is available before the high side connects. It also protects the non-B2B low side switch from charge currents.
- a Remove Before Flight (RBF) circuit allows overriding the inhibit control, fixing it in inhibited state.
- a discharge load switch provides discharge current limiting.
- a charge load switch provides charge current limiting, under and overvoltage lockout.
- a trickle charge bypass diode allows resuscitating batteries that have dropped to voltages below the charge undervoltage lockout threshold.
- a heater load switch, which is attached to the battery pack heater.
- voltage, current and power sensing
- a TVS protection diode

The PIU microcontroller collects housekeeping (HK) telemetry (TLM) and controls the battery heating. The battery unit electronics, other than the heater load switch, is fully autonomous and does not depend on a functioning microcontroller.

2.2.1 Inhibit scheme

On the PIU there are three inhibit switches, two high side switches (BAT_ENA_HS, SAT_ENA_HS) and one low side switch (BAT_ENA_LS). These switches are controlled by inhibit signals:

- The BAT_ENA_HS (battery enable high side) which controls the first independent high side switch. This first high side switch is activated by connecting BAT_ENA_HS to GND with the help of the physical separation switch.
- The second signal is the BAT_ENA_LS_POS (battery enable low side) which controls the battery low side switch. This switch requires a special activation because GND is blocked by the switch. To connect the low side switch, BAT_ENA_LS_POS should be connected to BAT_ENA_LS_NEG with a physical separation switch.
- The last signal is SAT_ENA_HS (satellite enable high side) which controls the second independent high side switch. This second high side switch is also activated by connecting SAT_ENA_HS to GND with a physical separation switch. The SAT_ENA_HS is part of the PDU electronics and is discussed in Section 2.4.1.

The signals are available on the umbilical connector and in a flight situation can be connected to the separation connector. In the lab environment the inhibits switches can be controlled directly via EGSE and umbilical connector 1. In flight environment, slave umbilical 1 to separation switch connector (with ABF plug) and connect plungers to separation connector, see Figure 2-2.

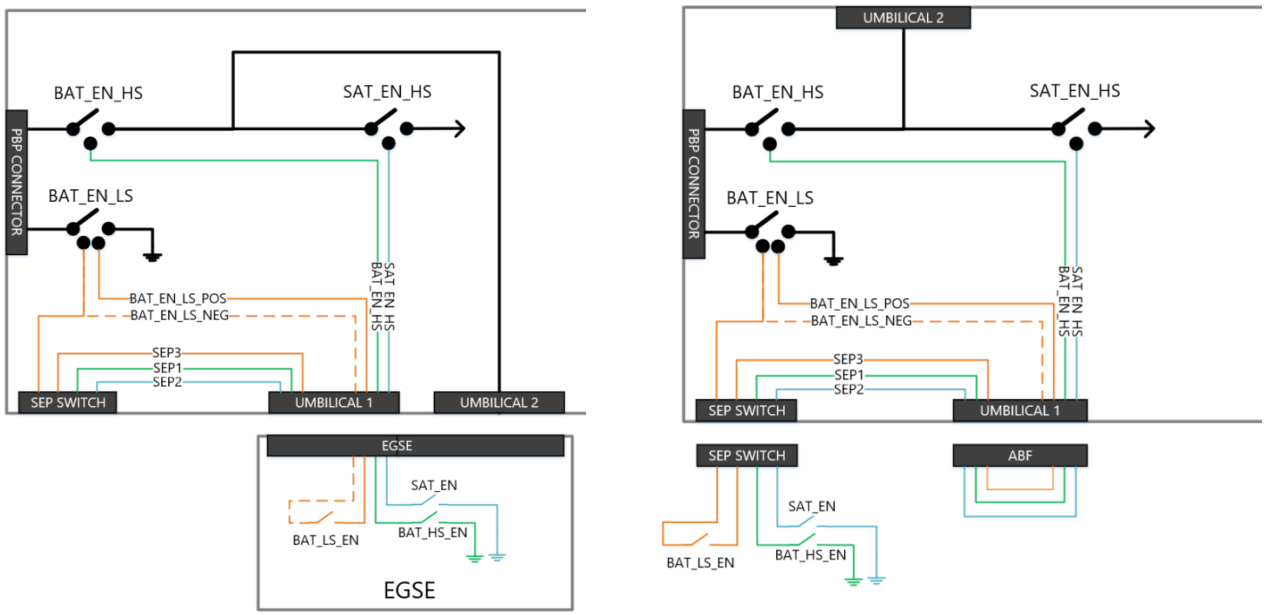


Figure 2-2 Inhibit diagram

The usual approach is to tie the enable signals to a plunger switch on the satellite body. The plunger is the normally closed (NC) type, with its neutral position being extended. Each plunger is electrically connected to the system's pair of separation signals that need to be connected. When the plunger is kept pressed down, the switch remains open circuit. This is the stowed configuration as the EPS remains inhibited in this situation. Once the plunger extends, the two signals are shorted. This activates the battery high and low switch and the PDU input load switch, allowing power to flow into the PDU electronics. This is the deployed configuration.

NOTE: The battery high side switch has a special circuit creating a dependency on having the low side switch connected. Hence the high side will not be able to connect when the low side is not yet connected, regardless of the high side control signal state.

2.2.1.1 Battery Enable High Side

The battery enable high side control signal, BAT_ENA_HS, controls connection of the battery high side onto the power rail by switching the B2B inhibit MOSFET. The battery enable is active low and is pulled up to either RAIL_PWR or the attached battery voltage level, whichever is higher. By connecting the BAT_ENA signal to ground the high side switch is enabled.

A signal diode is placed at the battery enable signal output, blocking any power flow back into the PBU through the battery enable pin. No back powering can occur through the BAT_ENA.

2.2.1.2 Battery Enable Low Side

The battery enable low side control signals, BAT_ENA_LS_POS and BAT_ENA_LS_NEG, control the low side MOSFET that inhibits power flow from ground to BAT- of the attached battery (i.e. discharge). The battery low side switch is enabled and conducting when BAT_ENA_LS_POS is connected to BAT_ENA_LS_NEG.

2.2.2 RBF Connector

The remove before flight (RBF) connector allows attaching a remove before flight device (e.g. a bus bar with label attachment) that is located on the outside of the satellite. Shorting the two signals BAT_ENA_LS_RBF and BAT_ENA_LS_POS together enables the RBF and locks the high and low side switches in inhibited state. Enabling the high or low side using their control signals will have no effect when the RBF is enabled.

NOTE: An enabled low side inhibited by an enabled RBF causes a power drain on the battery of around 20 µA max at 16V battery. This power drain is not present with a disabled low side. It is advised to disable the low side switch (e.g. by leaving the control signals floating) for long term storage, instead of using the RBF to override an enabled low side switch during storage.

2.2.3 Separation switches configuration

The ICEPS is designed to operate with three, four or more separation plunger switches. Three switches as a minimum, four switches for full redundant control. It is possible to combine SAT_EN_HS and BAT_EN_HS to a single plunger switch, as both are back power protected and need to pulled to GND to enable.

There are some cases where only two plunger switches can be used. For example, a structure might limit the amount of plunger switches. ICEPS can be modified to work with two plunger switches, but this is a non-standard configuration, additional cost applies, see also the Option Sheet [RD3]. If the board is modified to work with only two separation plungers, the board will not have three independent separation switches. Also, the RBF functionality will be lost.

The separation switches can be connected in several ways. Some optimized for redundancy, some for switch count or independent control. A list of possible options for wiring the plunger separation switches:

A. Six plunger switches, fully redundant, fully independent, see Table 2-1
B. Four plunger switches, fully redundant, SAT_EN and BAT_EN_LS not independent, see Table 2-2.
C. Three or four plunger switches, not redundant, fully independent, see Table 2-3.
D. Two plunger switches, fully redundant, not independent, see Table 2-4.
E. Two plunger switches, not redundant, fully independent, see Table 2-5.

Note that the configuration is both dependant on (1) the connections of the plunger switches to the separation switch connector and (2) the wiring of the ABF plug connected to Umbilical 1. See Figure 2-2.

Table 2-1 six plungers – Fully redundant, fully independent.

Interface with Umbilical 1				**Interface with Separation Switch Connector**		
On ABF	Connect	To		With plunger	Connect	To
1	SAT_EN_HS	Separation 1		1	Separation 1	GND
				2	Separation 1	GND
2	BAT_EN_HS	Separation 2		3	Separation 2	GND
				4	Separation 2	GND
3	BAT_EN_LS_high	Separation 3		5	Separation 3	BAT_EN_LS_low
				6	Separation 3	BAT_EN_LS_low

Table 2-2 four plungers – Fully redundant, SAT_EN and BAT_EN not independent.

Interface with Umbilical 1				**Interface with Separation Switch Connector**		
On ABF	Connect	To		With plunger	Connect	To
1	SAT_EN_HS & BAT_EN_HS	Separation 1		1	Separation 1	GND
2	SAT_EN_HS & BAT_EN_HS	Separation 2		2	Separation 2	GND
3	BAT_EN_LS_high	Separation 3		3	Separation 3	BAT_EN_LS_low
				4	Separation 3	BAT_EN_LS_low

Table 2-3 three or four plungers – Not redundant, fully independent

Interface with Umbilical 1				Interface with Separation Switch Connector		
On ABF	Connect	To		With plunger	Connect	To
1	SAT_EN_HS	Separation 1		1	Separation 1	GND
				(4)[1] optional	Separation 1	GND
2	BAT_EN_HS	Separation 2		2	Separation 2	GND
3	BAT_EN_LS_high	Separation 3		3	Separation 3	BAT_EN_LS_low

Table 2-4 two plungers – Fully Redundant, not independent, Customized PIU: no low-side battery inhibit

Interface with Umbilical 1				Interface with Separation Switch Connector		
On ABF	Connect	To		With plunger	Connect	To
1	SAT_EN_HS & BAT_EN_HS	Separation 1		1	Separation 1	GND
2	SAT_EN_HS & BAT_EN_HS	Separation 2		2	Separation 2	GND

Table 2-5 two plungers – Not redundant, fully independent, Customized PIU: no low-side battery inhibit

Interface with Umbilical 1				Interface with Separation Switch Connector		
On ABF	Connect	To		With plunger	Connect	To
1	SAT_EN_HS	Separation 1		1	Separation 1	GND
2	BAT_EN_HS	Separation 2		2	Separation 2	GND

2.2.4 Charge protection

The charge load switch is an auto-retry integrated load switch. It includes thermal protection, under and overvoltage lockout and a soft start function.

The undervoltage lockout is connected to the battery side and protects the EPS from a shorted or otherwise compromised battery. In case the battery voltage has fallen below the undervoltage lockout threshold, the battery will not be charged through the regular charge path. A trickle bypass current path is provided that will slowly charge the battery. Once the charge passes the undervoltage lockout high voltage threshold, the regular charge path will be enabled again.

The overvoltage lockout connected on the RAIL side protects the battery from voltages that exceed the maximum voltage. The charge path will be enabled again once the rail voltage drops below the overvoltage lockout low voltage.

The charge current limit is set for the maximum allowed charge current of the battery pack and/or PIU. In case the battery charge current exceeds the limit, the auto-retry switch will clamp the current momentarily until thermal protection turns off the switch. The switch then waits for its temperature to reduce and subsequently waits a short time before slowly switching on again. The soft start function slowly ramps the voltage to limit inrush current. If the overcurrent limit is tripped again, the mechanism will repeat. When more than sufficient

[1] Adding the fourth plunger can make SAT_EN_HS redundant, allowing sunlit only operation even if battery does not connect.

power is available on the rail causing repeated persistent overcurrent events, the system will effectively be pulse charging the battery.

> **NOTE:** the software undervoltage limits are higher than the hardware undervoltage limits. The hardware undervoltage lockout is a last resort lockout. See software ICD [RD1] for details on the software undervoltage lockout (refer to safety and emergency-low-power (EMLOPO) modes).

2.2.5 Discharge protection

The discharge load switch is an auto-retry integrated load switch. It includes thermal protection, undervoltage lockout and a soft start function.

The undervoltage lockout is connected to the battery side and protects the battery from deep discharge damage.

The discharge current limit is set for the maximum allowed discharge current of the battery pack and/or PIU. In case the battery discharge current exceeds the limit, the auto-retry switch will clamp the current momentarily until thermal protection turns off the switch. The switch then waits for its temperature to reduce and subsequently waits a short time before slowly switching on again. The soft start function slowly ramps the voltage to limit inrush current. If the overcurrent limit is tripped again, the mechanism will repeat.

> **NOTE:** the software undervoltage limits are higher than the hardware undervoltage limits. The hardware undervoltage lockout is a last resource lockout. See software ICD [RD1] for details on the software undervoltage lockout (refer to safety and emergency-low-power (EMLOPO) modes).

2.2.6 Trickle bypass

A trickle charge bypass path consists of a series resistance and diode. This creates a low current path that is used for charging batteries that have been deep discharged. Given the discharge path has undervoltage lockout functionality, this is likely a result of self-discharge and/or discharge due to IC leakage over long periods of non-use. The trickle path allows for a safe low charge current to try and resuscitate the battery. In case of a failed battery (e.g. reversed, shorted, very low capacity) the trickle charge path is a very light permanent load on the system.

2.2.7 Battery Heater & Thermostat control

The battery heater switch takes its power from the power RAIL. This allows power to flow through the battery heater resistors, located within each power battery pack (PBP).

The ICEPS2 MCU, using the heater switch, controls activation of the PBP heater automatically by comparing the temperature measured at the battery pack with internal setpoints in the software. See [RD1] for more information on the configuration of heater setpoints.

> **NOTE:** The MCU controls the heater activation. With satellite disabled (i.e. SAT_ENA floating) the battery heater will always be off. In addition, an EPS reset will interrupt any heating activity.

2.3 Conditioning Unit

The PCU provides three channels with a maximum power point tracker (MPPT) that take power from attached solar panels and regulate that to the voltage on the shared output RAIL. An additional two channels are available on the daughterboard. The MPPT on the channel ensures maximum power is extracted from the panels under varying illumination and temperature conditions. The conditioning unit regulates to a fixed voltage on its output that is equal to the maximum battery voltage level.

The functionality of a MPPT channel consists of:

- a boost regulator with true maximum power point tracking using the perturb and observe algorithm.

- voltage, current and power sensing on MPPT input and output
- an output ideal diode protecting against current backflow from the RAIL.

The MPPT channel electronics are fully autonomous and do not depend on a functioning MCU. This autonomy improves reliability through the redundancy provided by the parallel MPPT channels. During eclipse (no power on MPPT inputs) the conditioning units will be completely powered down, limiting power drain on the battery powered platform. In this case there will also be no MPPT telemetry available.

2.3.1 Solar Power Segment

The solar powered segment is directly powered from a 5V buck-boost regulator that is sourced directly from the attached solar panels. The 5V power is used to power the MPPT channel control electronics. Once the control electronics are powered up the main power conditioning commences, where the SPA power is boosted to the default output voltage.

2.3.2 No Battery Dependency

The PCU regulation stability is not dependent on the presence of a battery on its RAIL. The PCU can generate the default output voltage on the RAIL once a light load is applied. This allows use in "sunlit operation only" missions that do not fly with batteries.

Without any load on the RAIL, the regulated output voltage might not ramp up to the default output voltage level. Therefore running a PCU standalone without any load attached on the RAIL might not provide the expected voltage level on the RAIL. Adding a light load will cause the RAIL voltage to ramp up to the expected default voltage output, potentially after several seconds of delay.

2.4 Distribution Unit

The PDU distributes power taken from RAIL_PWR and splits that into several output bus channels. There are several output channels that provide buck regulated voltages. Apart from the regulated channels there is also one channel that passes RAIL voltage directly. Additional channels (including unregulated and boost voltage) are available on the daughterboard. All channels have load switches which are controlled by the PIU microcontroller.

2.4.1 Satellite Enable High Side

The satellite enable signal (SAT_ENA_HS) controls whether the PDU section is powered. The satellite enable is active low and is pulled up to RAIL_PWR. This signal can be connected to ground to enable the PDU and allow power to flow to the rest of the satellite. With satellite enable inhibited, no communication with PIU microcontroller is possible.

A signal diode is placed at the battery enable signal output, blocking any power flow back into the PIU through the satellite enable pin. No back powering can occur through the SAT_ENA_HS.

The satellite enable signal controls a set of integrated load switches on the input of the PDU electronics. These load switches provide:

- Latching current limiting (LCL) with time delayed auto-retry on overcurrent events.
- Overvoltage protection.
- Soft start voltage ramp upon enable.

The input switches are also controlled by an internal supervisor watchdog as part of the reset circuitry. A full power cycle of the PDU section and all attached satellite bus subsystems will result when either the active low SAT_ENA is set to a high level (i.e., disabled) or when the supervisor watchdog generates a reset pulse.

2.4.2 Voltage Domains

The ICEPS provides five voltage domains (VD) which are distributed on the output channels. These voltage domains are (see also Table 2-6):

• VD0 = Voltage Domain 0 = Unregulated RAIL_PWR.

• VD[1-4] = Voltage Domain [1-4] = DC/DC buck regulated voltage using RAIL_PWR as its input.

• VD5 = Voltage Domain 5 = DC/DC boost regulated voltage using RAIL_PWR as its input.

Table 2-6 Voltage domains defaults

Voltage domain	Default voltage	Remark
VD0	Unregulated Battery	Available on all types
VD1	5V	Available on all types
VD2	3.3V	Available on all types
VD3	5V	Only available for Type C
VD4	3.3V	Only available for Type C
VD5	28.2V	Only available for Type C

For more details on output voltage see Table 3-1 General Specifications.

NOTE: If custom voltages are required, they need to be specified when the production order is submitted, because these are implemented as a fixed setting in hardware. Additional cost applies.

NOTE2: VD2 voltage cannot be changed as it also provides the internal voltage for the ICEPS electronics.

2.4.3 Output Bus Channels

The ICEPS PDU distributes its voltage domains onto multiple output bus channels (OBC), using integrated load switches.

Each load switches provides:

- Latching current limiting (LCL) with overload protection, clamping to the current limit until thermal shutdown.
- Short circuit protection, with a fast trip current limiter that latches off the switch within microseconds.
- Current backflow protection, switch is turned off when currents start to reverse. This ensures no power sinks into the PDU section from the output, when the PDU section is powered.
- Passive current blocking ensuring no current sinks into the PDU section from the output, when the PDU section is unpowered.
- Soft start voltage ramp on enable.

All output channels have a load switch that is controlled by the MCU. Depending on the hardcoded and configurable PDU software configuration some of these channels are enabled on startup. See Section 2.4.3.3 for more information.

2.4.3.1 Identification Mechanism 1: VDx_OBC[y]

An output bus channel (OBC) can be identified according to its attachment to a voltage domain (VD). The used code is:

VDx_OBC[y]

with x = the VD number 0 through 5,

y = the OBC number 0 through 3 (available numbers depend on voltage domain).

A matrix representation of the available voltage domains versus the channels and the corresponding identifier is shown in Table 2-7. Note that the channels only available on type C are indicated in grey.

Table 2-7 Channel Matrix.

	VD0	VD1	VD2	VD3	VD4	VD5
Output Channel 0	VD0_OBC[0]	VD1_OBC[0]	VD2_OBC[0]	VD3_OBC[0]	VD4_OBC[0]	VD5_OBC[0]
Output Channel 1	VD0_OBC[1]	VD1_OBC[1]	VD2_OBC[1]	VD3_OBC[1]	VD4_OBC[1]	
Output Channel 2	VD0_OBC[2]	VD1_OBC[2]	VD2_OBC[2]			
Output Channel 3	VD0_OBC[3]	VD1_OBC[3]	VD2_OBC[3]			

2.4.3.2 Identification Mechanism 2: CH[x]

An output bus channel (OBC) can also be identified using a linear identification number irrespective of the voltage domain. For this the voltage domain channels are ordered sequentially, starting with all channels on the main PIU board (VD0_[0], VD1_[0-3], VD2_[0-3]) followed by the channels available on the daughterboard (VD0_[1-3], VD3[0-1], VD4[0-1], VD5[0])

The used linear code is:

CH[x]

with x = the channel number 0 through 16.

This type of linear mapping is primarily used in the software interface, as described in [RD1].

An overview of the mapping between the VDx_OBC[y] and CH[x] identification is provided in matrix form in Table 2-8. Note that the channels only available on type C are indicated in grey.

Table 2-8 Channel Matrix with CH[x] ID.

	VD0	VD1	VD2	VD3	VD4	VD5
Output Channel 0	CH[0]	CH[1]	CH[5]	CH[12]	CH[14]	CH[16]
Output Channel 1	CH[9]	CH[2]	CH[6]	CH[13]	CH[15]	
Output Channel 2	CH[10]	CH[3]	CH[7]			
Output Channel 3	CH[11]	CH[4]	CH[8]			

2.4.3.3 Automatic Output Channel Enable: Force-Enable/Command-Enable

The output bus load channels are configured as one of two possible types:

- Force-enable (FE) – these load switches are enabled automatically after power-on and cannot be switched off by command. Upon overcurrent latch-off, this load channel is automatically enabled again after a cooldown period.
- Command-enable (CE) – these load switches can be switched on or off by commands to the PIU. Automatic enable after power-on and automatic re-enable after overcurrent latch-off can be configured freely using the PIU software configuration. See [RD1] for more information.

The default enable configuration for the output bus channels is shown in Table 2-9, note that the channels only available on the daughterboard are indicated in grey.

Table 2-9 Channel matrix default enable config

	VD0	VD1	VD2	VD3	VD4	VD5
Output Channel 0	FE	FE	FE	CE	CE	CE
Output Channel 1	CE	CE	CE	CE	CE	
Output Channel 2	CE	CE	CE			
Output Channel 3	CE	CE	CE			

NOTE: The channel enable configuration can be customized upon request. A custom channel enable configuration needs to be specified when the production order is submitted, because these are hardcoded into the flight software. Additional cost may apply.

2.4.4 CSKB I²C Connections Options

The PIU data interface with the satellite is via I²C on the CSKB. Pull-ups for the CSKB I²C bus can be placed on the ICEPS, this is non-default. It needs to be specified in the option sheet if pull-ups on ICEPS are required. I²C SCL and DATA can be connected to CSKB default and to CSKB alternative position, see Table 4-2 H1 CSKB light pinout for details.

2.4.5 Voltage Supervisor/Watchdog

The PIU provides a voltage supervisor and watchdog integrated circuit that protects the PIU from invalid internal supply voltages and MCU runaway events. This PIU-internal hardware protection system is autonomously operating without requiring PIU external systems from interacting with it. In case the protection is triggered, all hardware after the satellite enable load switch located on the PDU section input is power cycled.

The battery and conditioning chain electronics are autonomous and independent and are not power cycled when the protection is triggered.

The PIU also supports a SW based I²C watchdog that safeguards against I²C bus lockups impairing EPS control by a bus master. More information on this can be found in [RD1].

2.4.6 Microcontroller

The MCU on the EPS interacts with the various components on the IU mainboard and optional daughterboard.

These components, as depicted on the block diagram Figure 2-1, are:

- Output load switches: controlling the enabling of load channels
- Power sensors: measuring voltage, current and power at the locations indicated
- Battery heater control: Controlling average heating power to the battery pack
- CSKB Digital Channels: Interfaces to the external master computer(s)

The MCU is mainly required for servicing external telemetry & tele-commanding (TM/TC), which is issued from the satellite's main control computer, the command & data handling system (CDHS).

Both the conditioning unit and battery units are designed to function mostly independently from the MCU to improve reliability. For these units the MCU gathers housekeeping (HK) telemetry. The MCU is only a dependency for providing battery pack heater control.

On the distribution unit the MCU controls all the output load switches, gathers telemetry on the power consumption of each output channel and keeps track of reset counters and overcurrent events.

The MCU provides several safeguards to recover the satellite in case of upsets. Apart from the current limit on each of the load switches, there is a hardware supervisor and watchdog to protect the proper operation of the MCU. There is also a global TM/TC I²C watchdog timer that will power cycle the satellite when communication

with the CDHS is lost.

A safe mode and an emergency low power mode are provided that go into effect automatically when the battery voltage drops below the user defined safety and hardware defined critical level respectively. This reduces the satellite power consumption by switching of selective output channels to restore the battery to an appropriate voltage level for nominal operation.

The MCU also provides a real time clock in its telemetry to the CDHS. that can be used to facilitate time keeping.

2.5 Voltage/Current/Power sensing

The ICEPS PIU provides measurements of the voltage, current and power at multiple locations on the board. These locations are:

- At the beginning of the battery unit (as seen from the RAIL_PWR)
- After the PDU satellite inhibit load switch (as seen from the RAIL_PWR) (VD0)
- On the output of each output bus channel
- On the input and output of each MPPT

The ICEPS PIU provides measured voltage for:

- VD1
- VD2

NOTE: the voltage/current/power sensing on the MPPT is done with the MPPT controller. Values are less accurate and tent to fluctuate more.

The voltage, current and power measurements are internally integrated from many samples taken at high frequency. The high frequency allows accurate power measurements even under conditions of fast changing pulses of power consumption. The voltage and current are taken from fewer samples than the power measurement, providing more realtime voltage and current values. Due to the different sample techniques the power is generally not equal to the voltage times current in a single HK TLM message. See [RD1] for more information.

NOTE: the voltage measurement of output bus channels is performed on the output side of the load switch. This also allows voltage sensing on the load power channel when the channel is switched off. It provides information on other power supplies that might be leaking power onto the channel or verification of a voltage when using redundant powering of channels. With a switched-on channel it allows verification of the proper operation of the channel switch. This is performed by comparing the VD voltage on the inside of the load switch with the voltage on the outside of the load switch, in combination with the sensed load current.

2.6 Daughterboard

As discussed in Section 2.3, Section 2.4.2 and Section 2.4.3, the daughterboard offers:

- Two additional solar MPPT chains
- Three more voltage domains (VD3, VD4, VD5)
- Eight more output bus channels (three on VD0, two on VD3, two on VD4 and one on VD5)

All housekeeping data of the daughterboard will be collected by the PIU (mainboard) microcontroller.

2.7 ICEPS Types

The PIU mainboard interfaces with a Battery Pack and can additionally be combined with the PIU-DB. Due to the mounting of the PBP-2S1P directly onto the PIU mainboard PCB, the PBP-2S1P cannot be used in

conjunction with the daughterboard.

Therefore, the following standard types are available:

- Type A: PIU + PBP-2S1P
- Type B: PIU + PBP-4S1P
- Type C: PIU + PBP-4S1P + PIU-DB

See Table 2-10, Table 2-11 and Table 2-12.

Table 2-10: ICEPS2 type A configuration

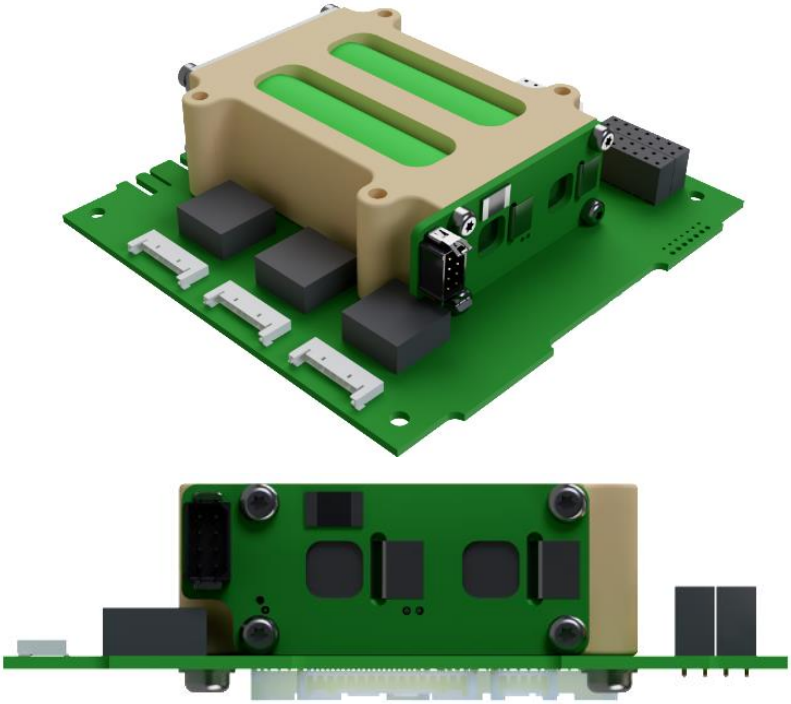
Type A	
Elements: • PIU mainboard • Power Battery Pack 2S1P The battery pack is mounted directly on top of the IU mainboard. The centre of mass of the assembly is close to the geometrical centre of the board.	

Table 2-11: ICEPS2 type B configuration

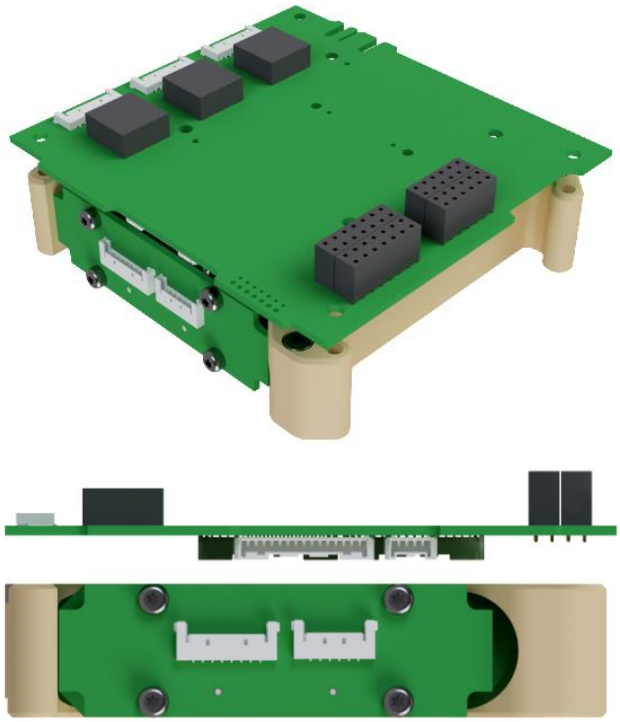
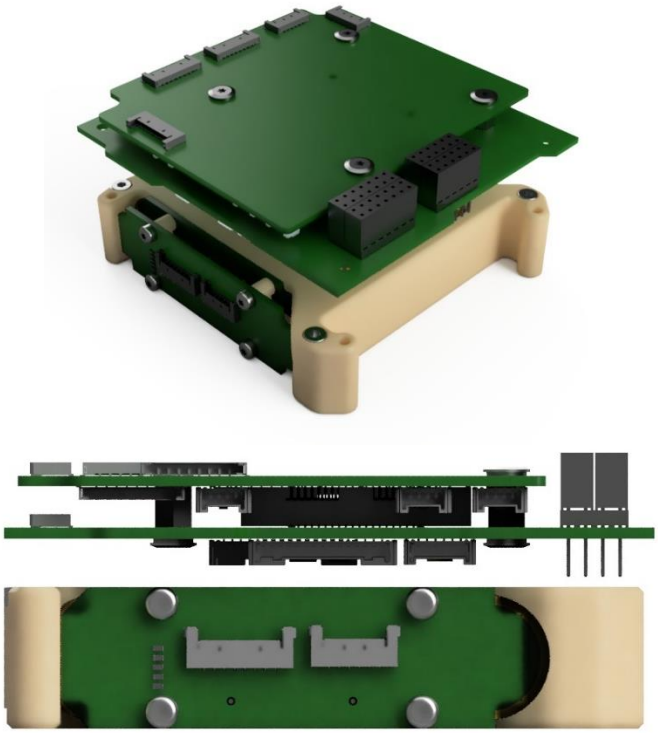
Type B	
Elements: • PIU mainboard • Power Battery Pack 4S1P The battery pack can be mounted anywhere in the stack.	

Table 2-12: ICEPS2 type C configuration

Type C	
Elements: • PIU mainboard • Power Battery Pack 4S1P • PIU Daughter Board The battery pack can be mounted anywhere in the stack. The daughterboard provides additional solar panel input channels and several regulated voltages and output channels on point-to-point connectors.	

3 Electrical performance

The sections below describe the electrical performance of the ICEPS2. Included are the specifications and performance of the solar panel to battery chain, performance of battery to output chain, line voltage drops and slew rate.

3.1 Specification

Specification assumes 20 °C ambient temperature unless otherwise specified.

Table 3-1 General Specifications

Parameter				Min	Typ	Max	Unit
Environmental Characteristics							
Without battery[2]	Operational temperature			-40		+85	°C
	Storage temperature			-50		+65	°C
	Storage lifetime (at relative humidity < 60 %)				12		months
With battery	Operational temperature[3] (heaters disabled)	charge		+10		+45	°C
		charge up to 800 mA		0		+45	°C
		discharge		-20		+60	°C
	Storage condition[4] (at relative humidity < 60 % and 30% state of charge)	up to 1 month		-20		+50	°C
		up to 3 months		-20		+40	°C
		up to 1 year		-20		+20	°C
Battery holding charge[5]		-20°C to +20°C			6-8	12	months
Electrical Characteristics							
Static (Idle) consumption					93		mW
(Power) Distribution Unit	Maximum input current PDU section			4.01	4.35	4.68	A
	VD0	Number of output channels	Type A and B	1			-
			Type C	1+3			
		Output voltage[6]		Battery Voltage			
		Output max. current per channel on PIU		2.75	3.01	3.30	A
		Output max. current per channel on PIU-DB (Type C)		3.0	3.3	3.6	A
	VD1	Number of output channels		4			-
		Output voltage unloaded (for loaded see Figure 3-5)		4.91	4.99	5.07	V
		Output max. current per channel		2.75	3.01	3.30	A

[2] Estimate from design evaluation.

[3] Operational temperature can be extended by use of the EPS battery heaters. Additional testing is recommended to verify the battery can be kept within specified operating conditions within the target satellite configuration and environment. See software ICD [RD1] for information on enabling the heaters.

[4] Battery aging reduces total capacity. Recoverable battery capacity is ≥ 80% under specified storage conditions. Reduce battery state of charge to ~30% before long term storage to reduce aging effects. Storage is preferably done in a protected container that can withstand leakage of electrolyte and thermal runaway conditions.

[5] Estimated by analysis, intermediate check would be recommended when exceeding 8 months.

[6] Battery voltage range.

Parameter				Min	Typ	Max	Unit
		Output max. current total for voltage domain[7]		4			A
	VD2	Number of output channels			4		-
		Output voltage unloaded (for loaded see Figure 3-5)		3.26	3.33	3.41	V
		Output max. current per channel		2.75	3.01	3.30	A
		Output max. current total for voltage domain[7]		4			A
	VD3 (Type C only)	Number of output channels			2		-
		Output voltage default		4.91	4.99	5.07	V
		Custom output voltage range[8]		2.8		12.0[9]	V
		Output max. current per channel		3.0	3.3	3.6	A
		Output max. current total for voltage domain[7]		4			A
	VD4 (Type C only)	Number of output channels			2		-
		Output voltage default		3.26	3.33	3.41	V
		Custom output voltage range[8]		2.8		12.0[9]	V
		Output max. current per channel		3.0	3.3	3.6	A
		Output max. current total for voltage domain[7]		4			A
	VD5 (Type C only)	Number of output channels			1		-
		Output voltage default		27.4	28.2	29.0	V
		Custom output voltage range[8, 10]		V_{bat}[11]	28.2	32.1	V
		Output max. current		1.4	1.5	1.6	A
Condition Unit (Solar interface)	Number of MPPTs inputs		Type A and B	3	3		-
			Type C	3 + 2	3+2		
	Maximum input voltage MPPT					15.0	V
	Functional voltage range for MPPT[12, 13]		Type A	3.5		7.5	V
			Type B and C	3.5		13.0	
	Input current per channel[14,15]					2	A
Battery Unit	Cell[16]	Voltage		2.5	3.6	4.0	V
		Nominal Capacity			3.2		Ah
	Pack[16]	Configuration	Type A	2 in series			-
			Type B and C	4 in series			

[7] Peak currents up to 6 A possible for a short duration on either VD1 or VD2 and VD3 or VD4.

[8] Custom output voltage possible, additional cost may apply.

[9] Requires a higher battery voltage

[10] If a voltage > Vbat and < 2 x Vbat is required outside 28V – 32.1V range, contact ISIS.

[11] Maximum battery voltage

[12] If one channel input voltage is above 3.5V on other channels 2.0V is sufficient.

[13] If input voltage is above functional MPPT range but below absolute maximum input voltage, no power point tracking with boost regulation is performed. SPA power will be allowed to pass to RAIL without regulation.

[14] If a higher current limit is required, please contact ISIS.

[15] Not enforced in hardware. Hardware limit set to 2.5A.

[16] Specification of default 18650 cells. Alternative 18650 cells can be provided upon request. Contact ISIS.

Parameter				Min	Typ	Max	Unit
	Charge over voltage limit. See Section 2.2.4	Vth rising	Type A		8.27		V
		Vth falling			7.68		V
	Charge under voltage limit[17] See Section 2.2.4	Vth rising			4.20		V
		Vth falling			3.91		V
	Discharge under voltage limits See Section 2.2.5	Vth rising			5.82		V
		Vth falling			5.41		V
	Charge over voltage limits See Section 2.2.4	Vth rising	Type B and C		16.27		V
		Vth falling			15.13		
	Charge under voltage limit[17] See Section 2.2.4	Vth rising			8.42		V
		Vth falling			7.82		
	Discharge under voltage limits See Section 2.2.5	Vth rising			11.88		V
		Vth falling			11.04		
	Operating Voltage (software limits)[18]		Type A	6.0			V
			Type B and C	12.0			
	Battery charge current			1.60	1.78	1.96	A
	Battery discharge current			4.0	4.45	4.9	A
	Trickle charge path	Blocking Diode V_f (at 10mA)				0.75	V
		Series Resistance R			2		kΩ
	Maximum battery heater current allowed by load switch			0.80	1.00	1.20	A
EGSE	Maximum input voltage		Type A			8	V
			Type B and C			16	V
Physical characteristics							
Mass			Type A	179	184	189	gram
			Type B	305	310	315	
			Type C	355	360	365	
Volume (excluding CSKB)	IU mainboard + 2 cell BP		Type A	96 x 92 x 26.5			mm^3
	IU mainboard		Type B	96 x 92 x 11.3			
	IU mainboard + daughterboard		Type C	96 x 92 x 16			
	4 cell BP		Type B and C	94 x 89 x 21.0			
Digital characteristics							
I^2C Specifications							
Bus logic low-level input voltage				0		1	V DC
Bus logic high-level voltage				2.3		3.3	V DC
Supported I^2C modes		Standard-mode				100	kbit/sec
		Fast-mode				400	
Supported address types				7 bits			-

[17] Trickle bypass path included for reviving cells that are below charge under voltage limit. Current: ~8mA.

[18] Software limits turn off the satellite when the lower voltage level is reached, to limit the depth of discharge to acceptable levels. Deep discharge causes accelerated degradation of the battery, reducing lifetime and increasing risk of sudden failure. If different levels are required, contact ISIS.

Parameter	Min	Typ	Max	Unit
I^2C node type		Slave only		-
I^2C general call supported		No		-

3.2 Solar Input to Battery Connector Chain Efficiency

The efficiency of MPPTs for the four-battery cell configuration is shown in Figure 3-1. The efficiency of the MPPTs in the two-battery cell configuration is shown in Figure 3-2. Efficiency is measured for the entire chain from the solar panel connector to the battery connector. All efficiencies include static losses. Refer to Figure 2-1 on page 10 for more information on the location of the connectors used for the measurement.

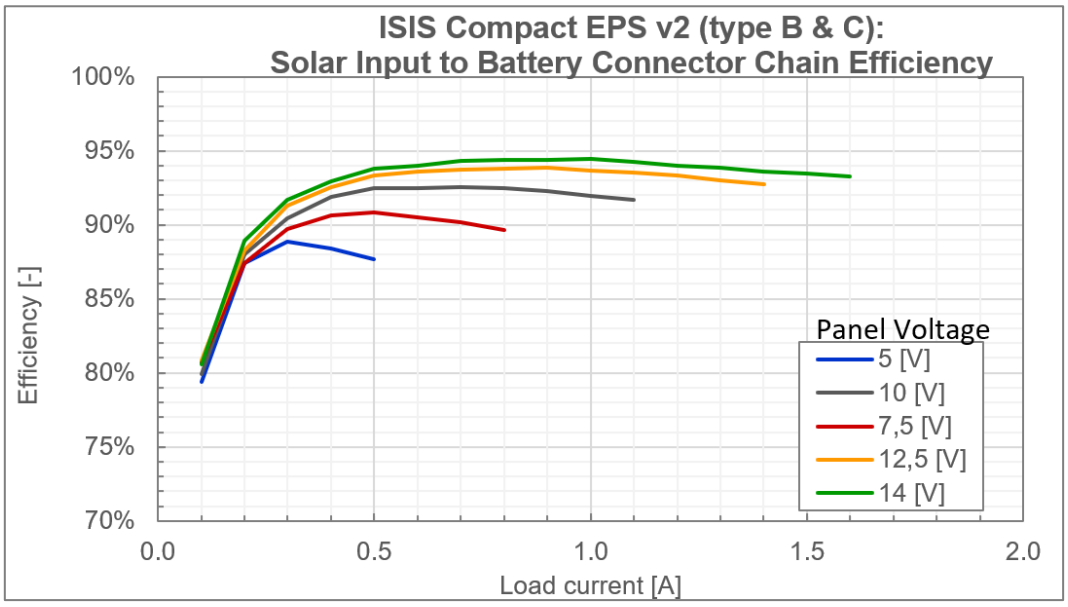


Figure 3-1: ICEPS2 Solar cell input to battery connector converter efficiency at different input voltages

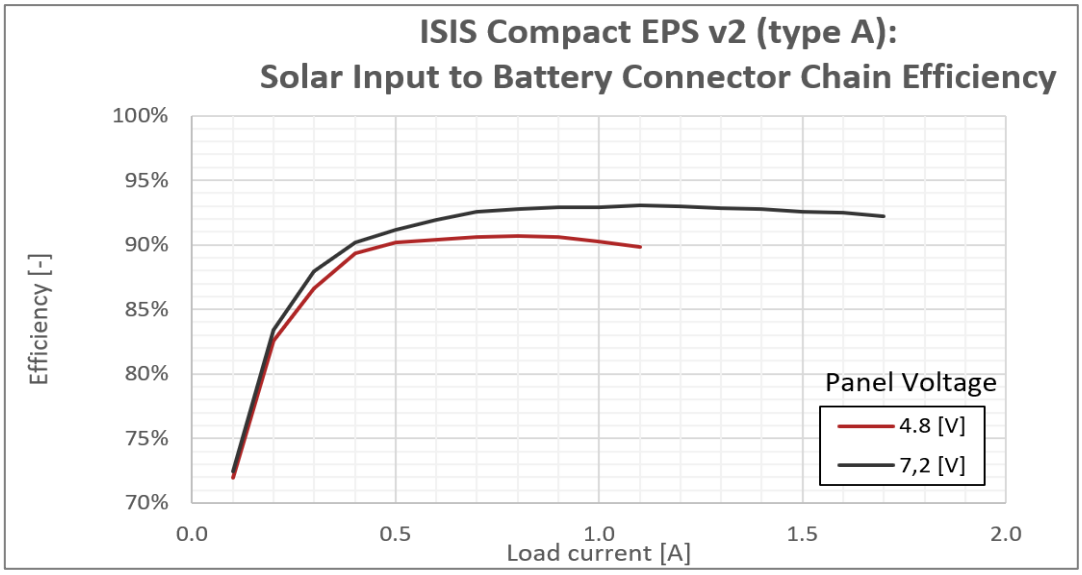


Figure 3-2: ICEPS2 Solar cell input to battery connector converter efficiency at different input voltages

3.3 Battery to CSKB Connector Chain Efficiency

Efficiencies of output power bus at different voltage domains are shown for the two and four cell battery

configurations in Figure 3-3. Efficiency of the boost converter on type C is shown in a separate graph in Figure 3-4. Efficiency is measured from battery input to the output on the CSKB. All measurements include static losses. Refer to Figure 2-1 on page 10 for more information on the location of the connectors used for the measurement.

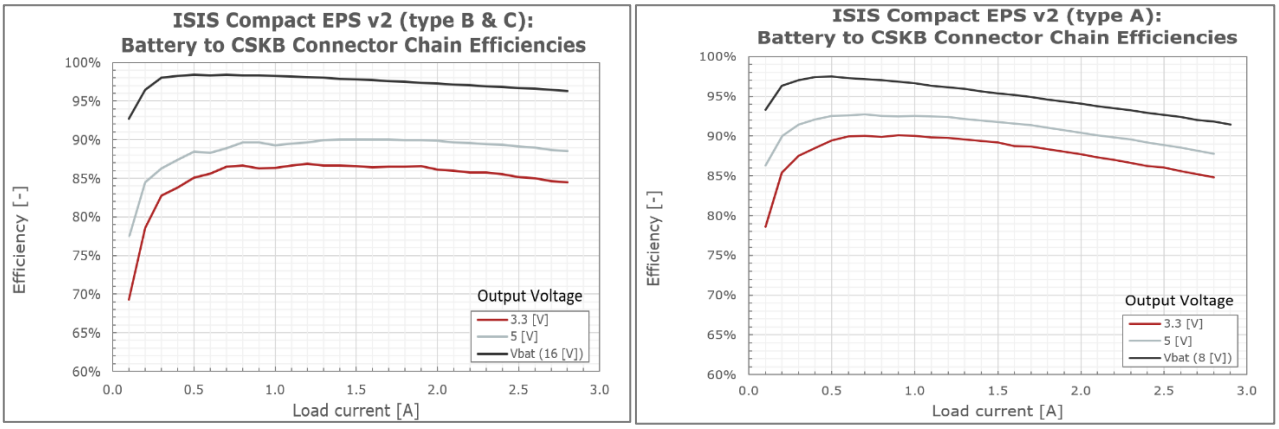


Figure 3-3: Output bus efficiencies

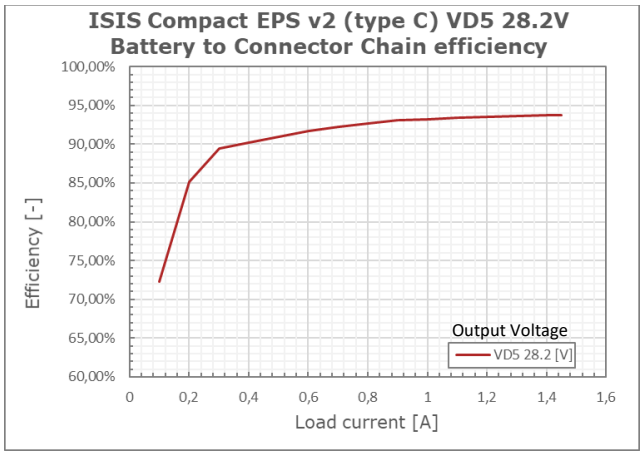


Figure 3-4 Output bus efficiencies for VD5 with four cell battery configuration

3.4 Line loss

The output voltage will drop under higher loads due to resistance on the lines in the ICEPS2. The voltage drop versus output current for 3.3V and 5V is shown in Figure 3-1. For the type C boost converter (28.2V) the line losses are shown in Figure 3-6. Line losses are measured at the output of the regulator and at the CSKB.

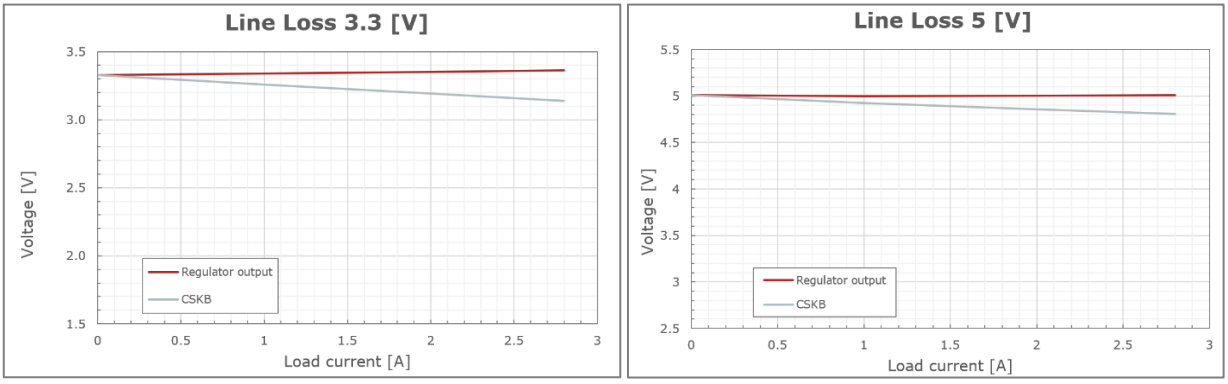


Figure 3-5: Line losses at 3.3V and 5V output

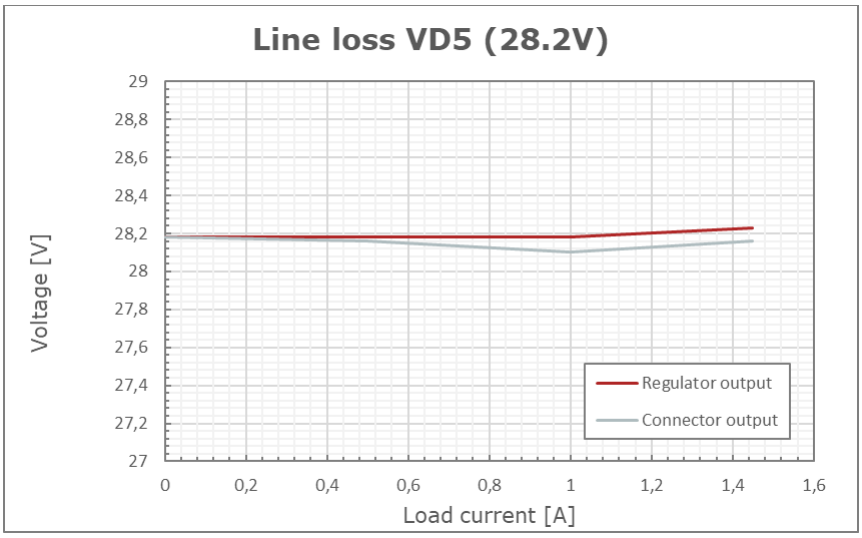


Figure 3-6 Line losses at 28.2V output

3.5 Slew Rate Control

Each of the output load switches have slew rate control. The slew rate is a hardware setting. The slew rate during start up is show in Figure 3-7.

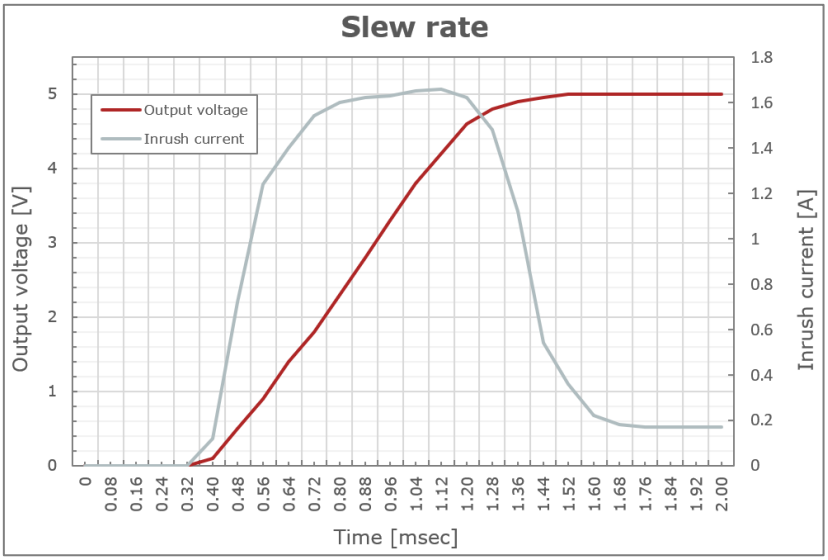


Figure 3-7: ICEPS2 slew rate

4 Electrical interface

4.1 PIU connector location

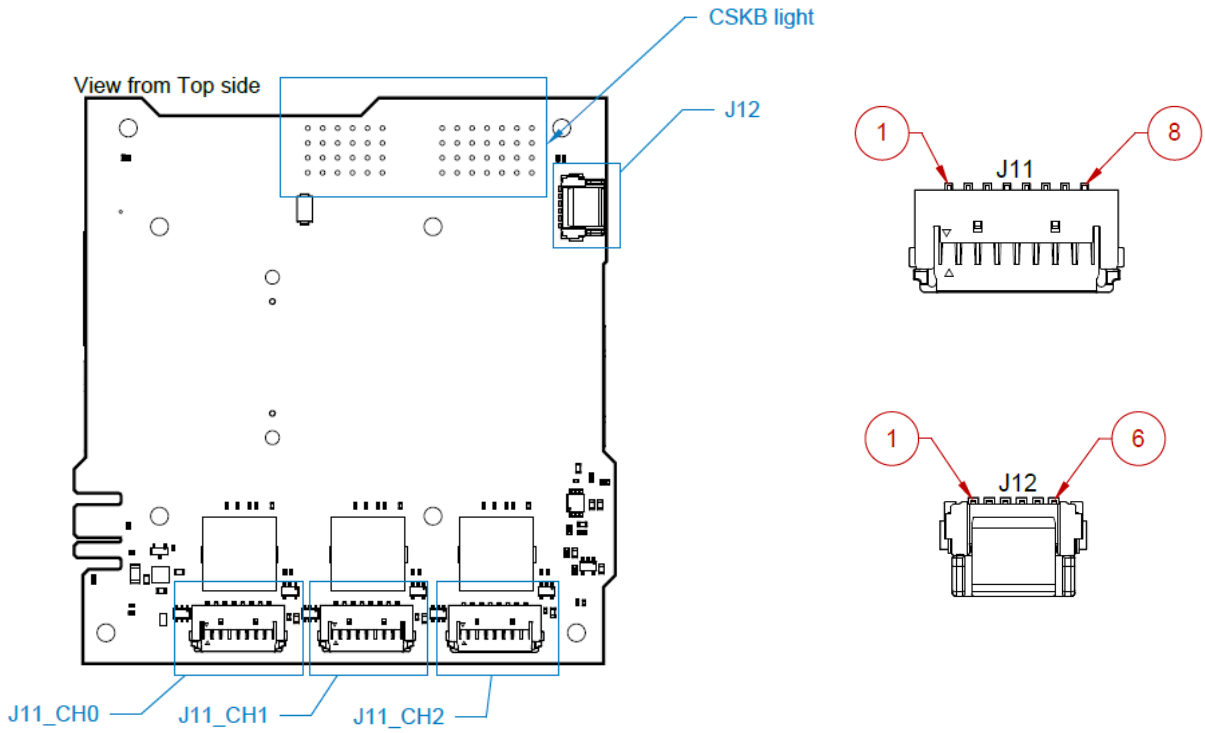


Figure 4-1: IU top face connectors

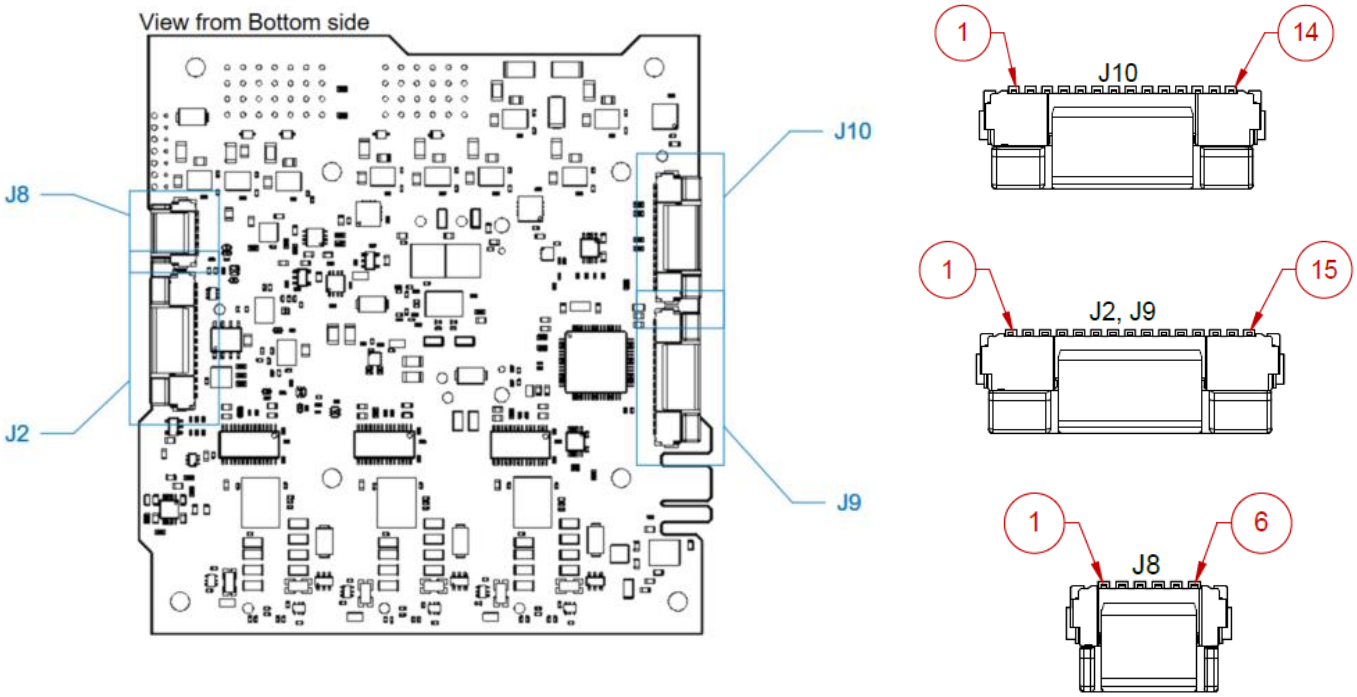


Figure 4-2: IU bottom face connectors

4.2 PIU Connector Pinout

4.2.1 H1 H2 CSKB light

A full CSKB has two times 52 pins, the CSKB on the ICEPS is the light version of the CKSB. The pins 21-32 and 39-52 are broken out on both H1 and H2. For the CSKB connector type refer to the ICEPS option sheet [RD3]. H1 and H2 are 2.54 mm trough hole connectors.

H2				UART-Tx	-	5V_p	3V3_p	GND	GND				GND	GND	GND	V_{BATT_p}	GPIO	GPIO ABF[0]*	GPIO
	2	-	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52
				UART-Rx	-	5V_p	3V3_p	GND	AGND				GND	GND	GND	V_{BATT_p}	GPIO	GPIO	GPIO ABF[1]*
	1	-	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51
H1				GND	GND	-	GND	-	GND				GND	GND	GPIO	GPIO	3V3_s1	3V3_s2	3V3_s3
	2	-	20	22	24	26	28	30	32	34	36	38	40	42	44	46	48	50	52
				I2C-SCL ALT	I2C-SDA ALT	-	GND	-	GND				GND	I2CSDA	I2CSCL	GPIO ABF[2]*	5V_s1	5V_s2	5V_s3
	1	-	19	21	23	25	27	29	31	33	35	37	39	41	43	45	47	49	51

**Preferred (POWER) ABF output signal pin assignment can be selected on the ICEPS2.*

Table 4-1 H2 CSKB light pinout

Pin	Name	Description	Remarks
H2_21	UART_RX_H2_21	Rx input for data coming in from the CSKB (e.g. transmitted by CDHS).	3.3 V
H2_22	UART_TX_H2_22	Tx output into the CSKB (e.g. received by CDHS).	3.3 V
H2_25, H2_26	OUTP_BUS_CH[1]	5V switched 0, channel is automatically enabled by default	
H2_27, H2_28	OUTP_BUS_CH[5]	3V3 switched 0, channel is automatically enabled by default	
H2_29, H2_30, H2_32,	GND	GND return path	
H2_39, H2_40, H2_41, H2_42, H2_43, H2_44	GND	GND return path, not CSKB standard	
H2_46, H2_45	OUTP_BUS_CH[0]	Rail voltage[19], channel is automatically enabled by default	
H2_50	GPIO24_H2_50_ABF_PLACED [0][20]	ABF placed indicator signal; output	Active low, pulled-up to 3.3 V
H2_51	GPIO25_H2_51_ABF_PLACED [1][20]	ABF placed indicator signal; output	Active low, pulled-up to 3.3 V
H2_52	GPIO26_H2_52	Auxiliary interface signal; Input	not connected by default

[19] Rail voltage is the voltage of the EPS internal power rail. The rail voltage, with a battery attached, is close to the battery voltage. Without a battery attached the rail will be the regulated CU output voltage.

[20] ABF placed pin signals, available in HK TLM, can be connected to the CSKB upon request. Contact ISIS.

Table 4-2 H1 CSKB light pinout

Pin	Name	Description	Remarks
H1_21	CSKB_I2C_SCL_ALT_H1_21	Alternative I^2C SCL	
H1_23	CSKB_I2C_SDA_ALT_H1_23	Alternative I^2C SDA	
H1_27, H1_28, H1_31, H1_32, H1_39, H1_40, H1_42	GND	GND return path, not CSKB standard.	
H1_41	CSKB_I2C_SDA_H1_41	I^2C SCL	
H1_43	CSKB_I2C_SCL_H1_43	I^2C SDA	
H1_45	GPIO22_H1_45_ABF_PLACED[2][20]	ABF placed indicator signal; output	Active low, pulled-up to 3.3 V
H1_47	OUTP_BUS_CH[2]	5V switched 1	
H1_49	OUTP_BUS_CH[3]	5V switched 2	
H1_51	OUTP_BUS_CH[4]	5V switched 3	
H1_48	OUTP_BUS_CH[6]	3V3 switched 1	
H1_50	OUTP_BUS_CH[7]	3V3 switched 2	
H1_52	OUTP_BUS_CH[8]	3V3 switched 3	

4.2.2 J9 and J10 Umbilical Connectors

J9 umbilical connector type: 505567-1581, J9 mates with 505565-1501. J10 umbilical connector type 505567-1481 and mates with 505565-1401. Both umbilical connectors are rated for 20 mating cycles.

Table 4-3 J10 Umbilical 1 Connector

Pin	Name	Description	Remarks
1	GND	Low power ground return.	
2	!abf_placed_0	First active low ABF detection signal.	Pulled up through 100kOhm to 3.3V on PIU. Connect to GND in an ABF.
3	!Separation_1	Active low separation signal 1. Connected to SEP connector.	Connect to !BAT_ENA_HS in an ABF to slave its activation to SEP_1.
4	!Bat_ENA_HS	Active low battery high side switch control signal, pulled up to battery or RAIL voltage.	Active low. Connect to GND to activate.
5	!Separation_2	Active low separation signal 2. Connected to SEP connector.	Connect to !SAT _ENA_HS in an ABF to slave its activation to SEP_2.
6	!Sat_ENA_HS	Active low satellite enable control signal.	Active low. Connect to GND to activate.
7	!Separation_3	Active low separation signal 3. Connected to SEP connector.	Connect to BAT_ENA_LS_POS in an ABF to slave its activation to SEP_3.
8	BAT_ENA_LS_POS	Positive of battery low side switch control, pulled up to battery or RAIL voltage whichever is higher.	Connect to BAT_ENA_LS_NEG to enable low side switch.
9	BAT_ENA_LS_RBF	RBF control override signal, weakly	Connect to BAT_ENA_LS_POS to override

		pulled up to rail or battery voltage, whichever is higher.	the enables and keep the battery disconnected.
10	BAT_ENA_LS_NEG	Negative of battery low side switch control, pulled to battery GND.	Connect to BAT_ENA_LS_POS to enable low side switch. Leave unconnected in ABF!
11	GND	Low power ground return.	
12	GND	Low power ground return.	
13	!abf_placed_1	Second active low ABF detection signal.	Pulled up through 100kOhm to 3.3V on PIU. Connect to GND in an ABF.
14	GND	Low power ground return.	

Table 4-4 J9 Umbilical 2 Connector

Pin	Name	Description	Remarks
1, 2, 3, 4	RAIL_PWR	Rail power	Max. EPS rail voltage
5, 6, 7, 8, 13	GND	Ground return	
9	UART_RX_H2_21	Direct feedthrough of CSKB H2 21. This is a Rx (e.g. transmit by CDHS) on the CSKB, meaning that on this pin data will be output, see Figure 4-3.	Max. 3.3 V
10	UART_TX_H2_22	Direct feedthrough of CSKB H2 22. This is an Tx (e.g. receive by CDHS) on the CSKB, meaning that on this pin data will be input, see Figure 4-3.	Max. 3.3 V
11	I2C_EXT_SCL	CSKB I^2C	Max. 3.3 V
12	I2C_EXT_SDA	CSKB I^2C	Max. 3.3 V
14	UART_TX_3V3_OUT1	EPS UART @115200 kbps, no parity and 1 stop bit.	Max. 3.3 V
15	UART_RX_3V3_IN1	EPS UART @115200 kbps, no parity and 1 stop bit.	Max. 3.3 V

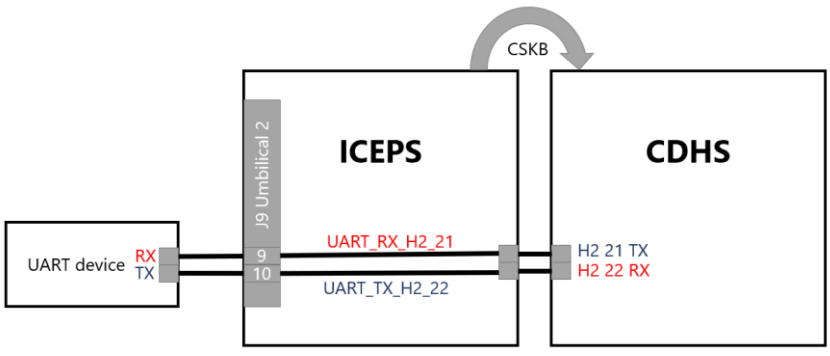


Figure 4-3 CDHS UART connection diagram

4.2.3 J8 Separation Connector

The sep connector simply routes the SEP signals onto the umbilical 1 connector. The ABF connector is used to slave the battery low, battery high and satellite enables to the SEP signals. In this config (i.e. ABF seated) the SEP signals can control EPS activation. See Section 2.2.1 for details.

With physical roller or plunger switches connect:

- !SEP1 to GND to connect the satellite high side switch
- !SEP2 to GND to connect the battery high side switch
- !SEP3 to !Separation_bat_LS_NEG to connect the battery low side switch

The separation signal connector is rated for 20 mating cycles. J8 connector is a micro-lock connector from Molex (part number: 505567-0681) and mates with: Molex 505565-0601.

Table 4-5 J8 Separation pinout

Pin	Name	Description	Remarks
1	!SEP1	Active low separation signal 1. Connect to separation switch(es).	Routes onto UMB connector.
2	GND	Ground return counterpart of !SEP1.	Low power system GND
3	!SEP2	Active low separation signal 2. Connect to separation switch(es).	Routes onto UMB connector.
4	GND	Ground return counterpart of !SEP2.	Low power system GND
5	!SEP3	Active low separation signal 3. Connect to separation switch(es).	Routes onto UMB connector.
6	!Separation_bat_LS_NEG	Counterpart of !SEP3.	Pulled down to battery negative.

4.2.4 J2 Battery connector

J2 connector type is 505567-1581 and mates with 505565-1501. The connector is rated for 20 mating cycles.

Table 4-6 J2 Battery Connector

Pin	Name	Description	Remarks
1	HEATERS_ON	Power supply to heaters	Rail Voltage. Max 1A.
2	VBAT_NEG		
3	TH_R_BATT[1]	Analog	Twist with GND pin 5
4	TH_R_BATT[0]	Analog	Twist with GND pin 6
5, 6	VBAT_NEG		
7, 8, 9, 10	VBAT_POS	Battery positive	Twist each with VBAT_NEG
11, 12, 13, 14	VBAT_NEG	Battery negative	
15	N.C.	Not connected	

4.2.5 J11 CH0, CH1, CH2 Solar Connectors

J11 connector type is a Molex Picolock. Part number 504050-0891 and mates with 504051-0801. The connector is rated for 20 mating cycles.

Table 4-7 J11 CH0, CH1, CH2 Solar Connectors

Pin	Name	Description	Remarks
1, 2	SP+	Solar panel input voltage	B side connector
3, 4	GND	Solar panel ground return path	Twist with corresponding SP+
5, 6	SP+	Solar panel input voltage	B side connector

7, 8	GND	Solar panel ground return path	Twist with corresponding SP+

4.2.6 J12 CH[3] and I2C connector

J12 connector type is a Molex Microlock. Part number 505567-0681 and mates with 505565-0601. The connector is rated for 20 mating cycles.

Table 4-8 J12 CH[3] and I2C

Pin	Name	Description	Remarks
1	CH[3]	VD2_OBC[1]	Same as on the CSKB
2, 6	GND	Ground return	
3	I2C_EXT_SDA	I^2C SDA	Same signal as on CSKB
4	I2C_EXT_SCL	I^2C SCL	Same signal as on CSKB
5	N.C.	Not connected	

NOTE: J12 cannot be used in combination with the PIU-DB. On type C this connector will **not** be mounted on the PIU. If point to point I^2C is required, use any of the PIU-DB connectors that offer I^2C.

4.3 PIU-DB Connector location

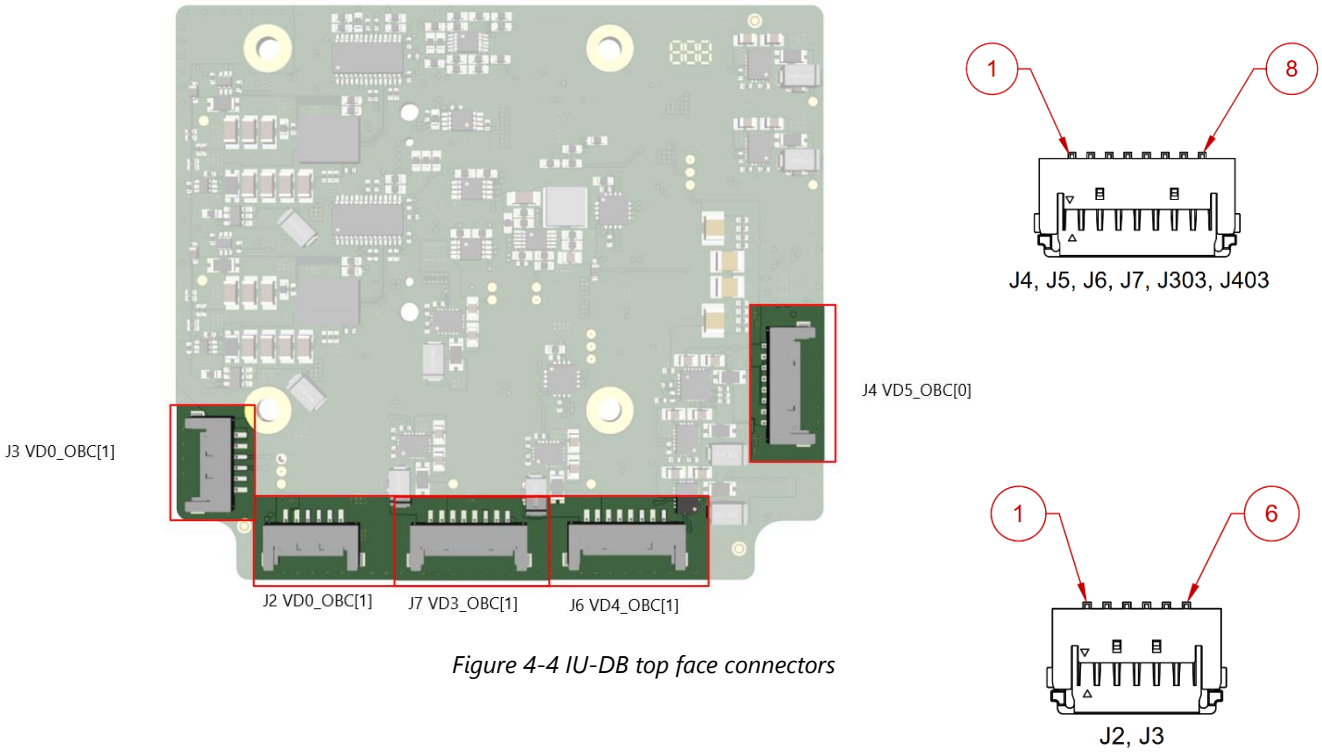


Figure 4-4 IU-DB top face connectors

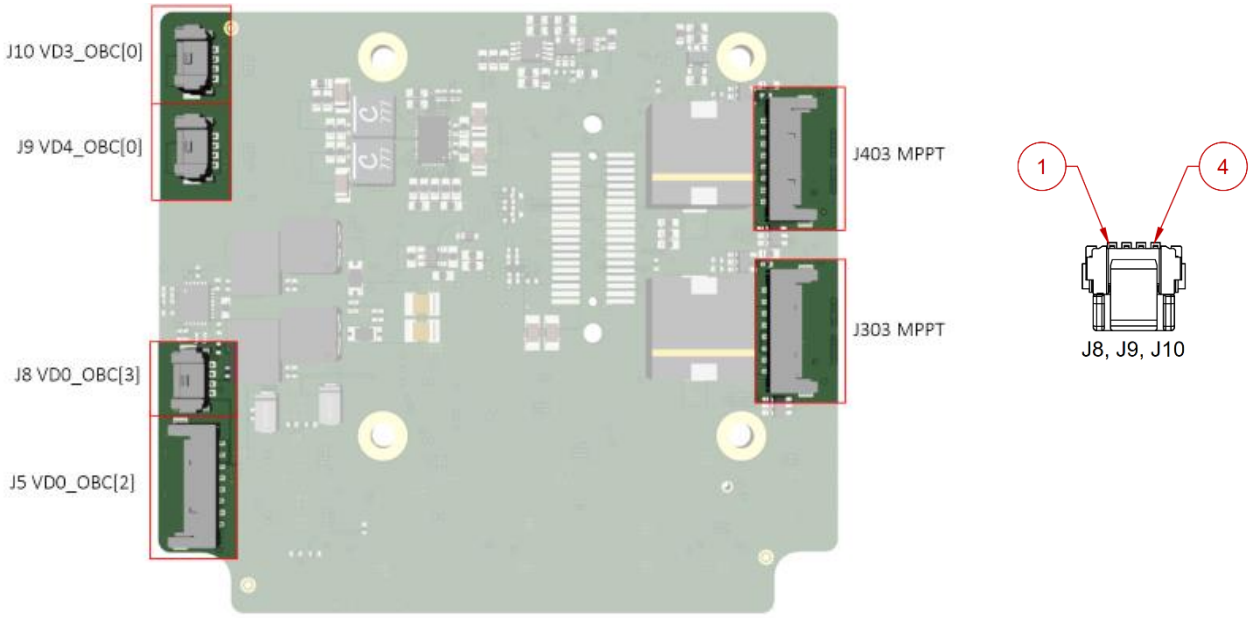


Figure 4-5: IU-DB bottom face connectors

4.4 PIU-DB Pinout

4.4.1 J2 & J3 VD0_OBC[1]

Both J2 and J3 have the same pinout and are therefore interchangeable. J2 and J3 connector is a pico-lock connector from Molex (part number: 504050-0691) and mates with: Molex 504051-0601. The connectors are rated for 20 mating cycles.

Table 4-9: J2 & J3 connector pinout

Pin	Name	Description	Remarks
1	VD0_OBC[1]	Voltage domain 0 (VBAT unregulated) switchable line 1	J2 and J3 pin 1 are connected to the same output switch.
2, 6	GND	VD return path	-
3	I2C SDA	I2C Data line	J2 and J3 I2C are connected to the same buffer output.
4	I2C SCL	I2C Clock line	
5	N/A	Non connected	

4.4.2 J5 VD0_OBC[2]

J5 connector is a pico-lock connector from Molex (part number: 504050-0891) and mates with: Molex 504051-0801. The connectors are rated for 20 mating cycles.

Table 4-10: J5 connector pinout

Pin	Name	Description	Remarks
1,2	VD0_OBC[2]	Voltage domain 0 (VBAT unregulated) switchable line 2	
3, 4, 5, 7	GND	Ground return patch for switchable output and I2C	
6	I2C SCL	I2C Clock line	
8	I2C SDA	I2C Data line	

4.4.3 J8 VD0_OBC[3]

J8 connector is a micro-lock connector from Molex (part number: 505567-0481) and mates with: Molex 505565-0401. The connectors are rated for 20 mating cycles.

Table 4-11: J8 connector pinout

Pin	Name	Description	Remarks
1, 2	GND		
3, 4	VD0_OBC[3]	Voltage domain 0 (VBAT unregulated) switchable line 3	

4.4.4 J10 VD3_OBC[0]

J10 connector is a micro-lock connector from Molex (part number: 505567-0481) and mates with: Molex 505565-0401. The connectors are rated for 20 mating cycles.

Table 4-12: J10 connector pinout

Pin	Name	Description	Remarks
1, 2	GND		
3, 4	VD3_OBC[0]	Voltage domain 3 switchable line 0	

4.4.5 J7 VD3_OBC[1]

J7 connector is a pico-lock connector from Molex (part number: 504050-0891) and mates with: Molex 504051-0801. The connectors are rated for 20 mating cycles.

Table 4-13: J7 connector pinout

Pin	Name	Description	Remarks
1,2	VD3_OBC[1]	Voltage domain 3 switchable line 1	
3, 4, 5, 7	GND	Ground return patch for switchable output and I2C	
6	I2C SCL	I2C Clock line	
8	I2C SDA	I2C Data line	-

4.4.6 J9 VD4_OBC[0]

J9 connector is a micro-lock connector from Molex (part number: 505567-0481) and mates with: Molex 505565-0401. The connectors are rated for 20 mating cycles.

Table 4-14: J9 connector pinout

Pin	Name	Description	Remarks
1, 2	GND		
3, 4	VD4_OBC[0]	Voltage domain 4 switchable line 0	

4.4.7 J6 VD4_OBC[1]

J6 connector is a pico-lock connector from Molex (part number: 504050-0891) and mates with: Molex 504051-0801. The connectors are rated for 20 mating cycles.

Table 4-15: J6 connector pinout

Pin	Name	Description	Remarks
1,2	VD4_OBC[1]	Voltage domain 4 switchable line 1	
3, 4, 5, 7	GND	Ground return patch for switchable output and I2C	
6	I2C SCL	I2C Clock line	
8	I2C SDA	I2C Data line	

4.4.8 J4 VD5_OBC[0]

J4 connector is a pico-lock connector from Molex (part number: 504050-0891) and mates with: Molex 504051-0801. The connectors are rated for 20 mating cycles.

Table 4-16: J4 connector pinout

Pin	Name	Description	Remarks
1, 2	VD5_OBC[0]		
3, 4, 5, 7	GND		
6	I2C SCL	I2C Clock line	
8	I2C SDA	I2C Data line	

4.4.9 J303 & J403 Solar panel connectors

J303 and J403 connector type is 504050-0891 and mates with 504051-0801. The connector is rated for 20 mating cycles.

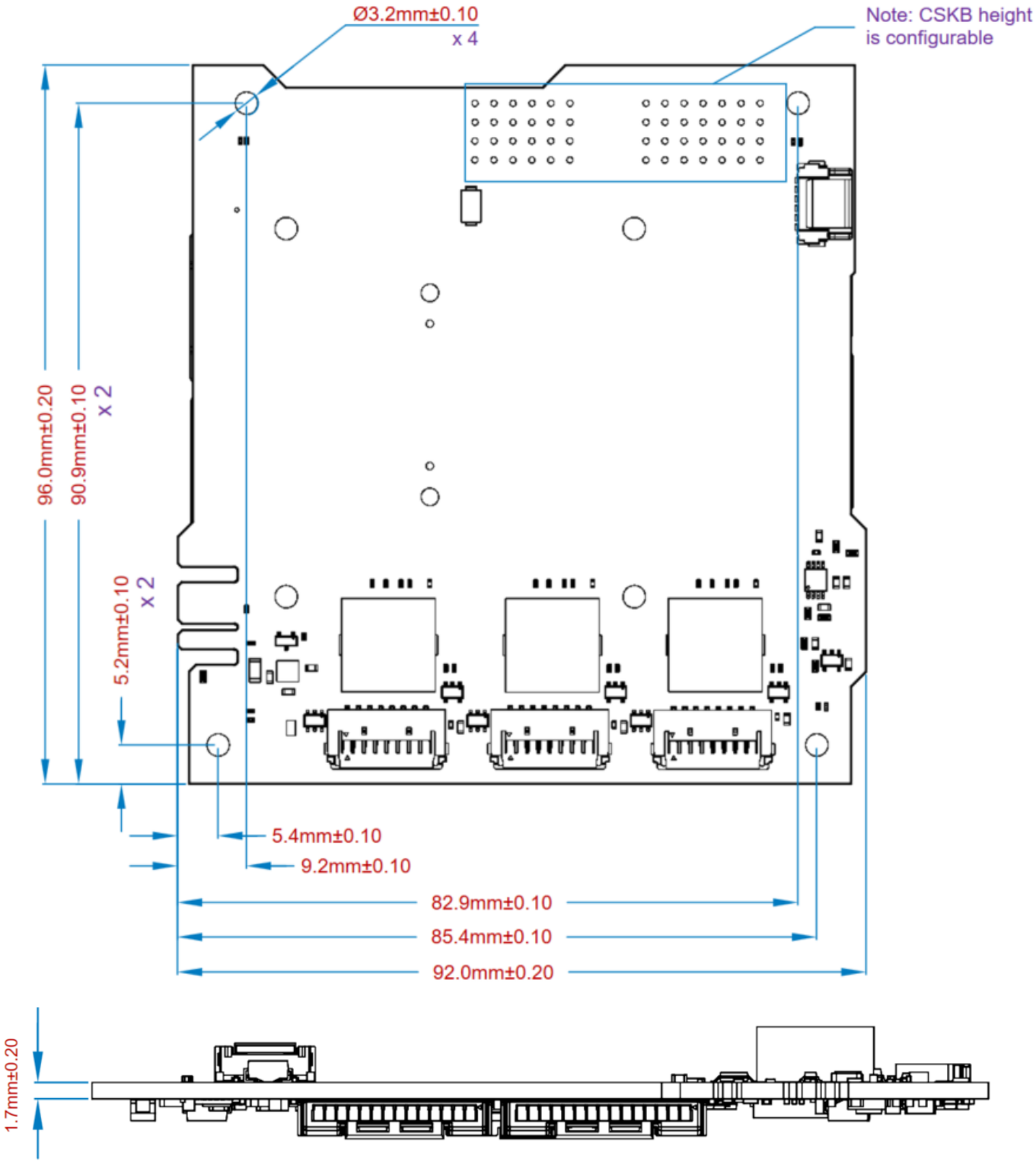
Table 4-17 J303, J403 Solar Connectors

Pin	Name	Description	Remarks
1, 2	SP+	Solar panel input voltage	B side connector
3, 4	GND	Solar panel ground return path	Twist with corresponding SP+
5, 6	SP+	Solar panel input voltage	B side connector
7, 8	GND	Solar panel ground return path	Twist with corresponding SP+

5 Mechanical Interface

The outer board dimensions and mounting hole pattern is the same for all three types (Type A, Type B, Type C). The board hight is different per type.

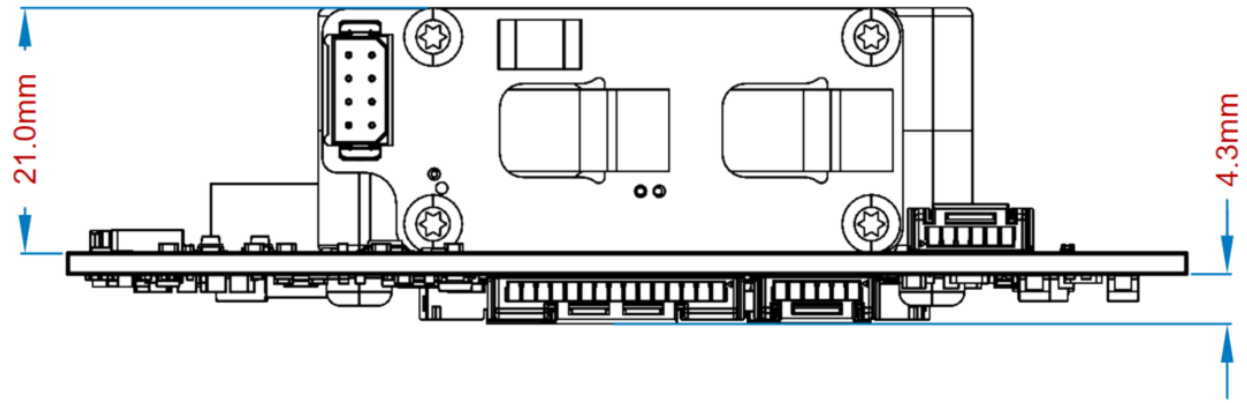
5.1 Generic board dimensions



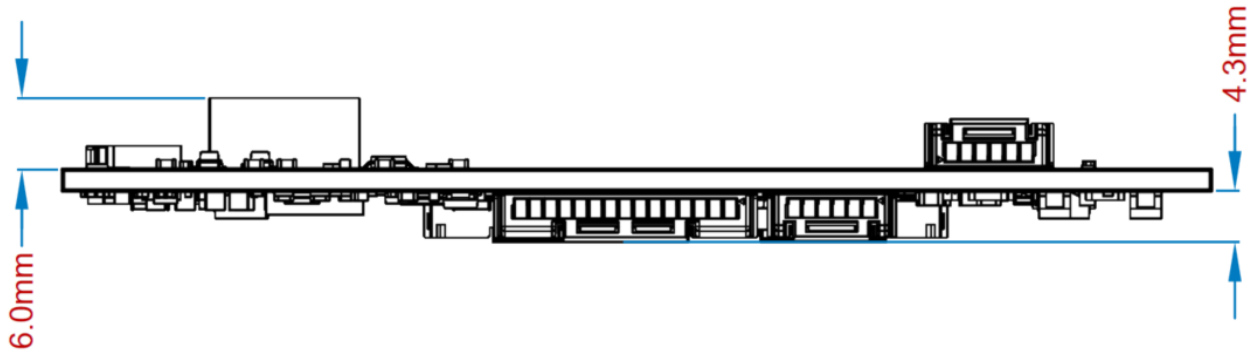
5.2 Type specific dimensions

The board type specific dimensions have nominal values only.

5.2.1 Type A



5.2.2 Type B



5.2.3 Type C