

APP-AI MCU 2024 簡介



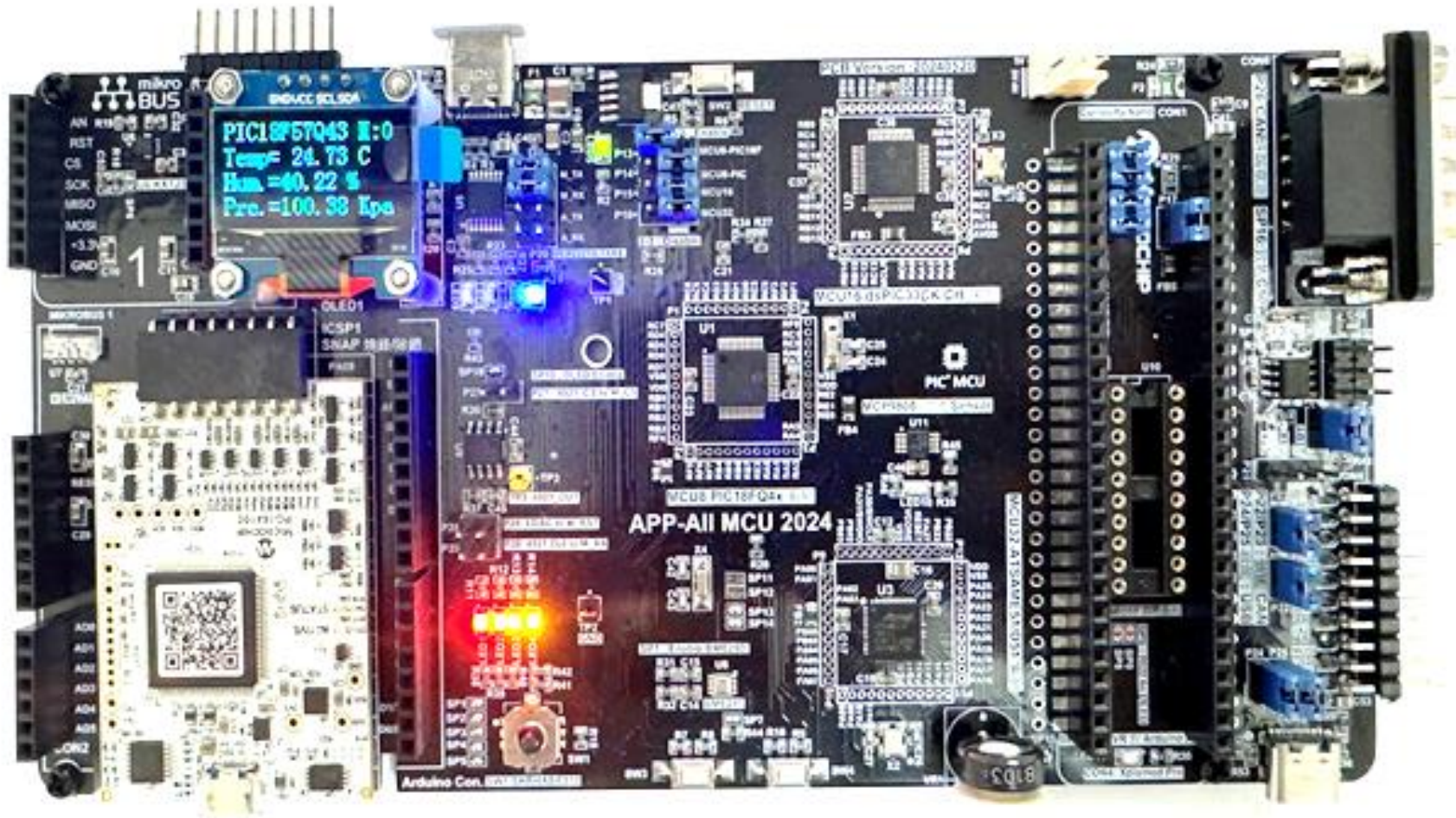
A Leading Provider of Smart, Connected and Secure Embedded Solutions



SMART | CONNECTED | SECURE

Version : 2023-July, total 37+ pages, average 40 minutes to review

APP-AII MCU 2024 : 另一個 Microchip MCU 泛用平台



APP-AI MCU 2024 上預置的 MCU 型號

- **8-bit MCU : PIC18F57Q43**
- **8-bit MCU : 在 U10 的位置上保留 20-pin 的 IC 腳座，可以自由使用相容的 PIC16F1/PIC18F MCU**
- **16-bit MCU : dsPIC33CK256MP505**
 - 具備 CAN FD 功能的 16-bit MCU
- **32-bit MCU : ATSAME51G19A**
 - 具備 USB、CAN FD 等功能的 32-bit ARM Cortex M4 MCU

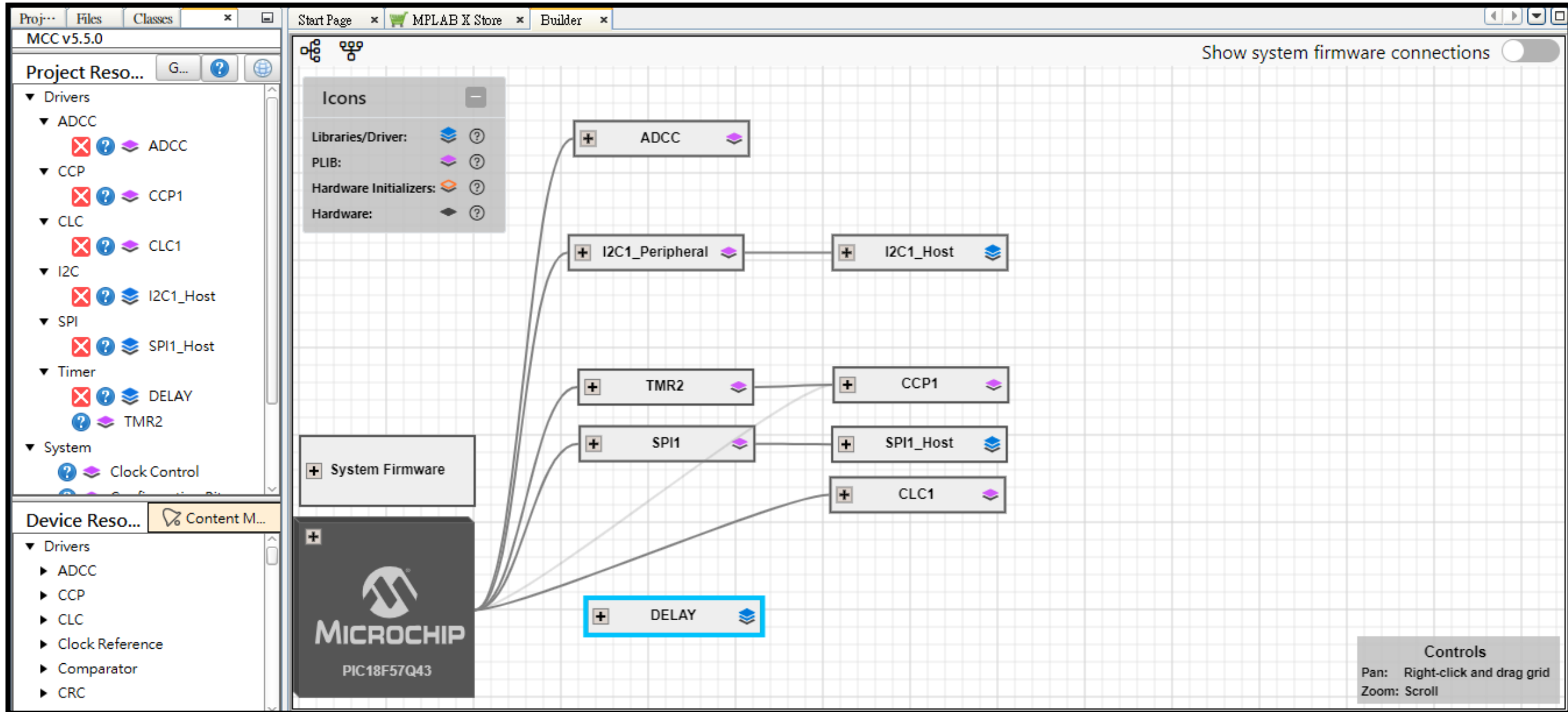
APP-AII MCU 2024 內建的周邊

- 一個I2C 介面的三軸加速度計 KXTJ3-1057
- 一個I2C 介面的Lighting Sensor – Vishay 的VEML7700-TT
- 一個I2C 介面的Humidity sensor - BOSCH BME280
- 一個I2C 介面的溫度Sensor –Microchip MCP9808
- 一個I2C 介面的OLED Display -單色128 * 64
- 一個SPI 介面的DAC –Microchip MCP4921
- 兩個WS2812B One-Wire Color LED
- 一個MCP2221A 作實驗板上的UART 以及I2C 介面轉換至USB 的介面IC
- 一個ALPS 的SKRHABE010 五向開關
- CAN Transceiver : ATA6561
- CAN Connector (DB-9 & 排針)
- USB Connector : Type-C for USB Device function

APP-All MCU 2024

PIC18F57Q43 出廠測試程式的Configuration

PIC18F57Q43 所使用到的Drivers & Resources



PIC18F57Q43 接腳的 Configuration

SPI & CCP1 的功能因為使用在 CLC，所以不須做實際規劃

Output	Notifications [MCC]	Pin Grid View ×																																																
Package:	TQFP48 ▾	Pin No:	21	22	23	24	25	26	33	32	8	9	10	11	16	17	18	19	34	35	40	41	46	47	48	1	42	43	44	45	2	3	4	5	27	28	29	20	36	37	38	39	12	13	14	15				
			PORTA								PORTB								PORTC								PORTD								PORTE				PORTF											
Module	Function	Direction	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3	4	5	6	7				
CCP1 ▾	CCP	in/out																	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒													🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒			
CLC1 ▾	CLC1	output	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																														🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒		
	CLCIN0	input	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																						🔒		
SPI1 ▾	SCK1	in/out									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																									
	SDI1	input									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																									
	SDO1	output									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																								
OSC ▾	CLKOUT	output							🔒																																									
RESET ▾	MCLR	input																																																🔒
I2C1 ▾	SCL1	in/out									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																									
	SDA1	in/out									🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																									
ADCC ▾	ADGRDA	output	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																														🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	
	ADGRDB	output	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒																														🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	
	ANx	input	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	
Pins ▾	GPIO	input	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒
	GPIO	output	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒	🔒

PIC18F57Q43 接腳名稱的列表參考

MCC 產生的 API 開頭名稱會採用 Custom Name 中的名稱

The screenshot displays the MPLAB X IDE interface for the PIC18F57Q43 device. The main workspace shows a block diagram of the device with various modules connected to the System Firmware. The left sidebar shows the Project Resources tree, and the right sidebar shows the Pins table.

Project Resources:

- CLC
 - CLC1
- I2C
 - I2C1_Host
- SPI
 - SPI1_Host
- Timer
 - DELAY
 - TMR2
- System
 - Clock Control
 - Configuration Bits
 - Interrupt Manager
 - Main
 - Pins

Pins Table:

Location	Pin Name	Module	Function	Direction	Custom Name	Analog	Start High	Weak Pullup	Open Drain	Slew Rate	Input Buffer	Ac
15	RF7	CLC1	CLC1	output	IO_RF7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
9	RB1	I2C1	SCL1	in/out	IO_RB1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	ST	Sta
10	RB2	I2C1	SDA1	in/out	IO_RB2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	ST	Sta
8	RB0	ADCC	ANx	input	IO_RB0	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
22	RA1	Pins	GPIO	input	SWA	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
23	RA2	Pins	GPIO	input	SWB	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
26	RA5	Pins	GPIO	input	SWD	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
11	RB3	Pins	GPIO	input	SWC	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
17	RB5	Pins	GPIO	input	SWCNT	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
42	RD0	Pins	GPIO	input	SW3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
43	RD1	Pins	GPIO	input	SW4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
44	RD2	Pins	GPIO	output	LED1	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
45	RD3	Pins	GPIO	output	LED2	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
12	RF4	Pins	GPIO	output	LED3	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	
13	RF5	Pins	GPIO	output	LED4	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	ST	

確認PIC18F57Q43 設定於最高的工作頻率 (64M)

The screenshot displays the MPLAB X IDE interface for configuring a PIC18F57Q43 microcontroller. The central workspace shows a block diagram of the system, including the PIC18F57Q43 device and various peripherals like ADCC, I2C1_Peripheral, TMR2, SPI1, and DELAY. The right-hand pane shows the 'Clock Control' settings, which are configured for a system clock of 64,000,000 Hz (64 MHz) using the HFINTOSC source. The 'Advanced Settings' section indicates that 'Active Clock Tuning Update' is enabled.

System Settings:

- System Clock (Hz): 64000000
- Clock Source: HFINTOSC
- HF Internal Clock: 64_MHz
- Clock Divider: 1

Advanced Settings:

- Secondary Oscillator Power Mode Select: Low power
- Clock Switch Hold Control: may proceed
- Secondary Oscillator: ☐
- PLL Enable: ☐
- Active Clock Tuning: ☐
- Active Clock Tuning Update: ☒

PIC18F57Q43 中 CLC module 的設定 - 參考 AN1606

<https://ww1.microchip.com/downloads/en/AppNotes/00001606A.pdf>

The screenshot displays the MPLAB X IDE interface for configuring the CLC1 module in a PIC18F57Q43 project. The left pane shows the Project Resources tree with CLC1 selected. The main workspace shows a block diagram with various modules connected to the CLC1 module. The right pane shows the CLC1 configuration settings, including Custom Name (CLC1), CLC dependency selector (CLC1), and CLC Settings (Enable CLC, Logic Cell Mode bits). The bottom right shows a logic diagram for the CLC1 module.

Project Resources:

- Drivers
 - ADCC
 - ADCC
 - CCP
 - CCP1
 - CLC
 - CLC1
 - I2C
 - I2C1_Host
 - SPI
 - SPI1_Host
 - Timer
 - DELAY
 - TMR2
- System
 - Clock Control
 - Configuration Bits

Device Resources:

- Drivers
 - ADCC
 - CCP
 - CLC
 - Clock Reference
 - Comparator
 - CRC
 - CWG

CLC1 Configuration:

- Custom Name: CLC1
- CLC dependency selector: CLC1
- CLC Settings
 - Enable CLC: ☒
 - Logic Cell Mode bits: AND-OR
- Interrupt Settings
- Export CLC image

Logic Diagram:

The logic diagram shows the CLC1 module connected to various inputs and outputs. The inputs are CCP1_OUT, SPI1 SCK OUT, SPI1 SDO OUT, and CLCIN0 (CLCIN0PPS). The outputs are connected to a logic circuit consisting of four 3-input AND gates (labeled 1, 2, 3, 4) and a final 4-input OR gate. The output of the OR gate is connected to a buffer.

加入OLED128x64.c 來完成OLED 的控制

