

24006 PNP67 Lab2_1 使用 APP-MCU-MASTERS24 ATSAME54P20A



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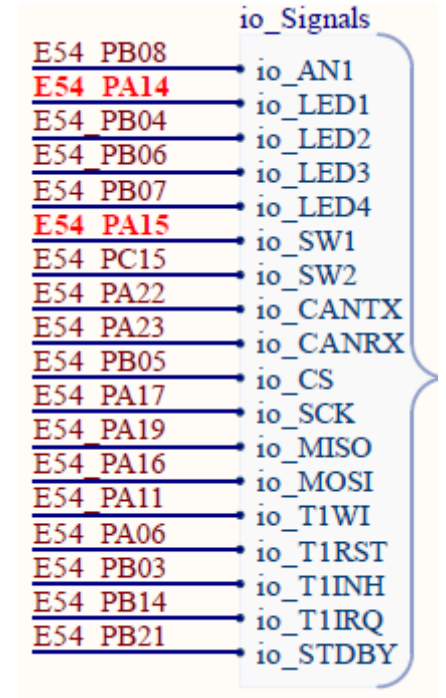
Version : 2023-July, total 37+ pages, average 40 minutes to review

Lab2_1

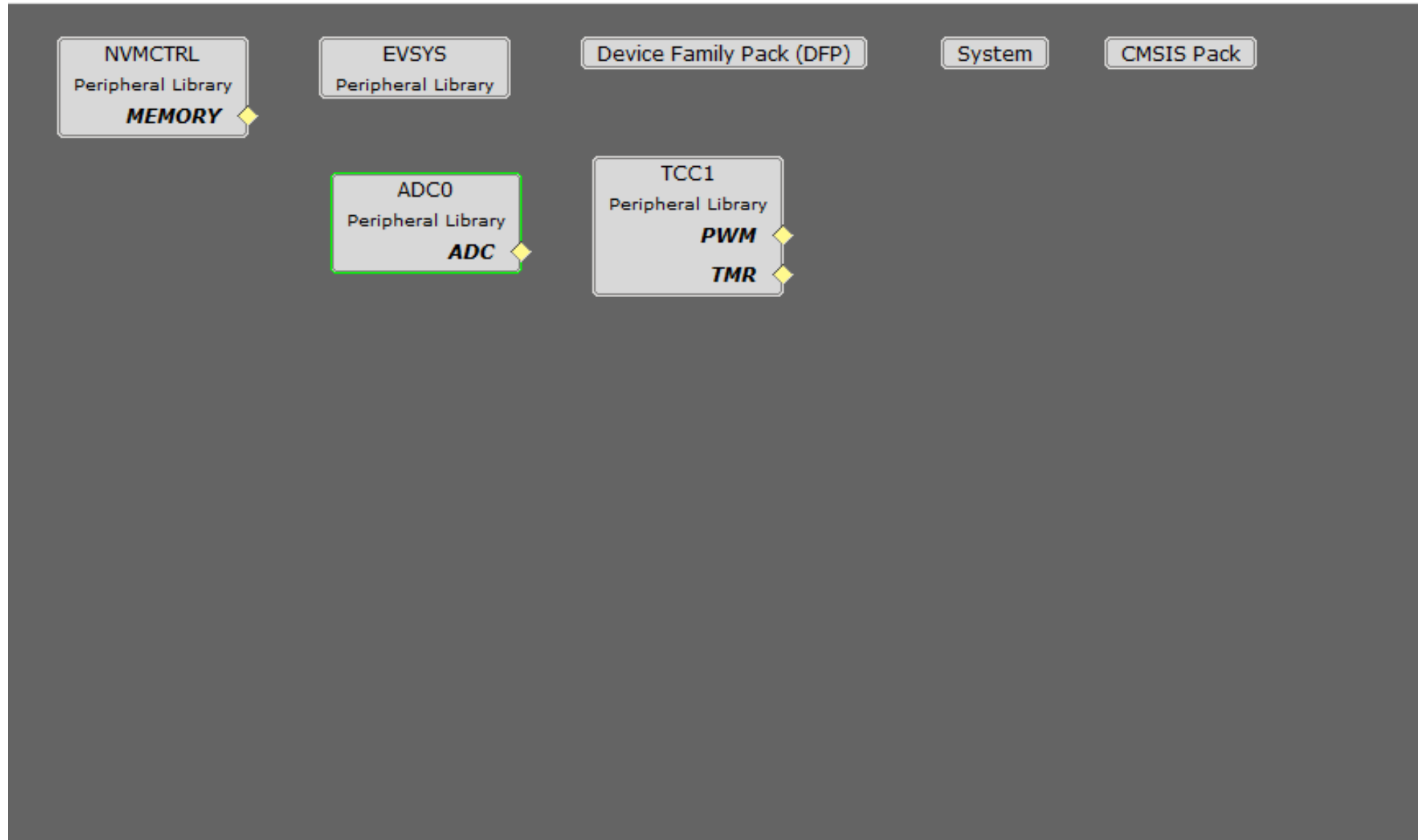
• Lab2_1 主要功能

- 使用 APP-MCU-MASTERS24 的 VR1 來控制 LED1 的亮度
 - VR1 : ADC0 的 AIN2
 - LED1 : PA14 ， 可以是 TCC1 的 WO2
- 透過 DMA Channel 0 ， 使 ADC0 的轉換結果直接控制 TCC1 的 Duty
 - ADC0 設定為 8-bit resolution 就好
 - TCC 1 設定為 Period 為 255 的 PWM
- 使用中斷的方式來處理DMA 完成後再次 Enable 的動作

```
DMAC_ChannelCallbackRegister( DMAC_CHANNEL_0,  
                               &myDmacInterruptHandler, (uintptr_t)NULL);
```



Lab2_1 的 Project Graph 配置



Lab2_1 ADC0 的設定

ADC0 的 Prescaler 設為 divided by 128，故意讓 ADC 的轉換時間大過 TCC1 Period

The screenshot displays the Microchip Studio IDE interface. On the left, the 'Peripheral Library' pane shows various components: NVMCTRL (Peripheral Library, MEMORY), EVSYS (Peripheral Library), Device Family Pack (DFP), System, CMSIS Pack, ADC0 (Peripheral Library, ADC), and TCC1 (Peripheral Library, PWM, TMR). The ADC0 component is highlighted with a green box. On the right, the 'ADC0' configuration window is open, showing the following settings:

- Select Prescaler: Peripheral clock divided by 128
- Select Sample Length (cycles): 4
- **** Conversion Time is 32.0 uS ****
- Select Reference: VDDANA
- Select Conversion Trigger: Free Run
- Enable DMA Sequencing: ☐
- Channel Configuration
 - Select Positive Input: ADC AIN2 Pin
 - Select Negative Input: Internal Ground
- Result Configuration
 - Select Result Resolution: 8-bit result
 - Left Aligned Result: ☐
 - Enable Result Ready Interrupt: ☐
 - Enable Result Ready Event Out: ☐
- Window Mode Configuration
- Sleep Mode Configuration

Lab2_1 TCC1 的設定

TCC1 的設定要點為：Period Value = 255，以便讓 ADC0 的 8bit 轉換結果來控制 Duty

The screenshot displays the MPLAB Code Configurator (MCC) interface for configuring the TCC1 peripheral. The main workspace shows a block diagram with components like NVMCTRL, EVSYS, Device Family Pack (DFP), System, CMSIS Pack, ADC0, and TCC1. The TCC1 block is highlighted with a green border and labeled with 'PWM' and 'TMR'. The right-hand pane shows the configuration tree for TCC1, with the following settings:

- Enable Slave: ☐
- Run during Standby: ☐
- Select Prescaler: No division (dropdown)
- Prescaler and Counter Synchronization: Reload or reset counter on next prescaler clock (dropdown)
- Operating Mode: PWM (dropdown)
 - Select PWM Type: NPWM (dropdown)
 - PWM Direction - Count Down: ☐
 - Period Value: 255 (spin box)
 - **** PWM Frequency is 187500 Hz ****
 - Enable Period Interrupt: ☐
 - Enable Period Event Out: ☐
 - Select Output Matrix: Default Channel Outputs (dropdown)
- Channel Configurations
 - Channel 0: ☐
 - Channel 1: ☐
 - Channel 2:
 - Duty Value: 128 (spin box)
 - Output Polarity: Output is ~DIR and set to DIR when counter match (dropdown)
 - Enable Dead Time: ☐
 - Swap Outputs: ☐
 - Enable Compare Match Interrupt: ☐
 - Enable Compare Match Event OUT: ☐
 - Enable Compare Match Event IN: ☐
 - Channel 3: ☐
- Outputs
 - Invert Output 0: ☐
 - Invert Output 1: ☐
 - Invert Output 2: ☒

The bottom status bar shows the output window with the following messages:

```
13:20:31.510 INFO: ..\src\packs\CMSIS\CMSIS\Core\Include\core_cm4.h Success.
13:20:31.510 INFO: ..\src\packs\CMSIS\CMSIS\Core\Include\mpu_armv7.h Success.
```

Lab2_1 的 Pin Setting

PB08 (AN1) 以及 PA14 (LED1) 為本實驗使用的腳位

Order: Pins Table View <input checked="" type="checkbox"/> Easy View									
Pin Number	Pin ID	Custom Name	Function	Mode	Direction	Latch	Pull Up	Pull Down	Drive Strength
16	PD01		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
17	PB06		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
18	PB07		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
19	PB08		ADC0_AIN2/X1/Y1	Analog	High Impedance	n/a	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
20	PB09		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
21	PA04		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
22	PA05		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
23	PA06		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL

Pin Number	Pin ID	Custom Name	Function	Mode	Direction	Latch	Pull Up	Pull Down	Drive Strength
58	PC14		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
59	PC15		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
60	PA12		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
61	PA13		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
62	PA14	E54_LED	TCC1_WO2	Digital	High Impedance	n/a	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
63	PA15		Available	Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL
64	GND			Digital	High Impedance	Low	<input type="checkbox"/>	<input type="checkbox"/>	NORMAL

io_Signals	
E54 PB08	io_AN1
E54 PA14	io_LED1
E54 PB04	io_LED2
E54 PB06	io_LED3
E54 PB07	io_LED4
E54 PA15	io_SW1
E54 PC15	io_SW2
E54 PA22	io_CANTX
E54 PA23	io_CANRX
E54 PB05	io_CS
E54 PA17	io_SCK
E54 PA19	io_MISO
E54 PA16	io_MOSI
E54 PA11	io_T1WI
E54 PA06	io_T1RST
E54 PB03	io_T1INH
E54 PB14	io_T1IRQ
E54 PB21	io_STDBY

Lab2_1 中DMAC 的設定

設定 ADC0 為 DMA Channel 0 的 Trigger source 並致能中斷

Active Channels List

Channel Number	Trigger
DMAC Channel 0	ADC0_RESRDY

Add Channel

Remove Selected Channel

☐ Use Linked List Mode

DMA Channel 0 Settings

Enable Interrupt



Trigger Action

One Beat Transfer per DMA Request

Source Address Mode

Fixed Address Mode

Destination Address Mode

Fixed Address Mode

Beat Size

8-bit bus transfer

Burst Length

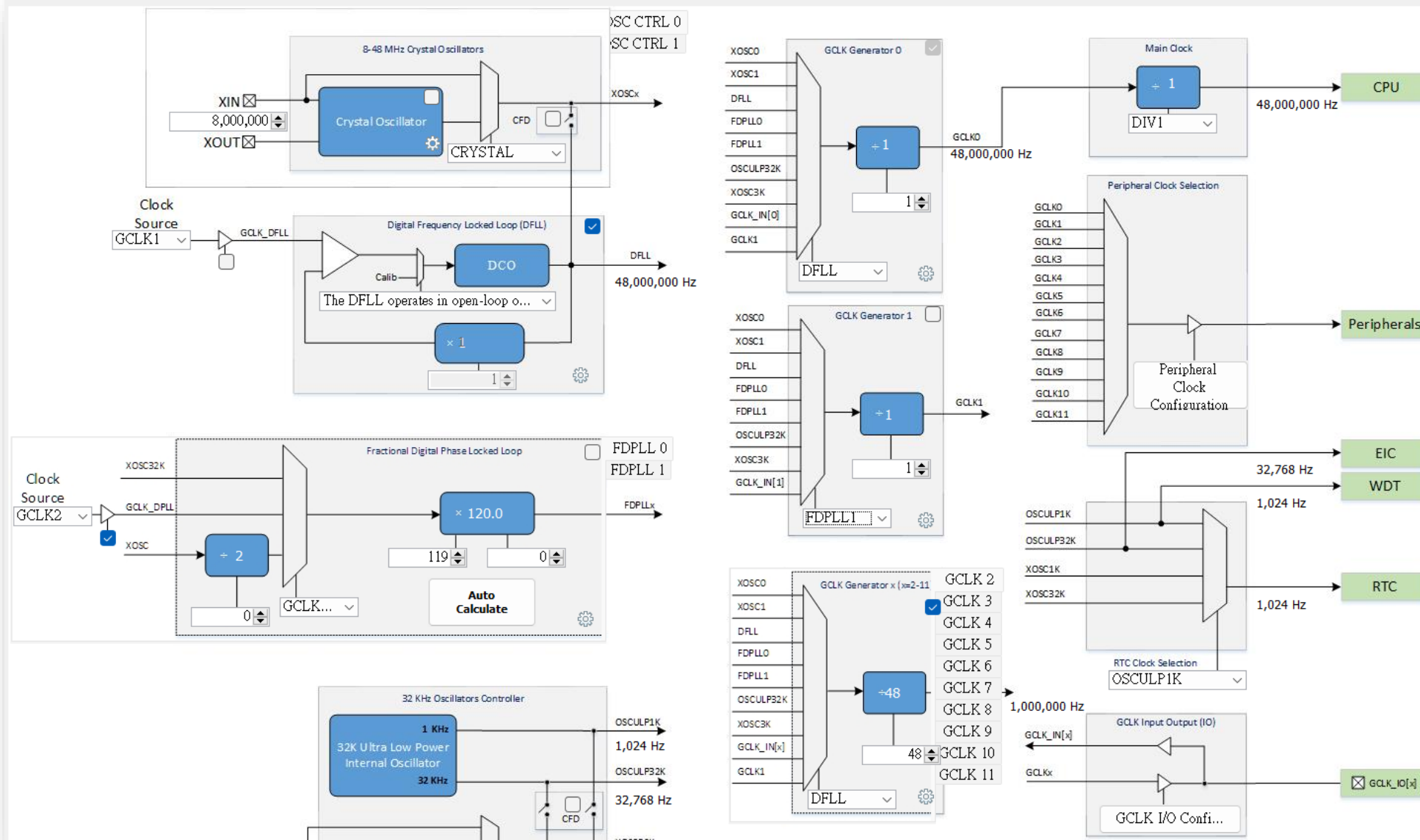
SINGLE

FIFO Threshold

1BEAT

Lab2_1 中Clock 的設定

請注意我們將 Main Clock 由 120Mhz 改為 48 Mhz 並關閉 GCLK1



Lab2_1 中Clock 的設定 - Peripherals

對於使用到的周邊，要記得設定好 clock 的來源才能正常工作

Peripheral Clock Configuration

Peripheral	Enable	Source	Peripheral Clock Frequency
AC	<input type="checkbox"/>	GCLK1	--
ADC0	<input checked="" type="checkbox"/>	GCLK0	48,000,000 Hz
ADC1	<input type="checkbox"/>	GCLK1	--
CAN0	<input type="checkbox"/>	GCLK1	--
CAN1	<input type="checkbox"/>	GCLK1	--
CCL	<input type="checkbox"/>	GCLK1	--
DAC	<input type="checkbox"/>	GCLK1	--
EIC	<input type="checkbox"/>	GCLK1	--
EVSYS_0	<input type="checkbox"/>	GCLK1	--
EVSYS_1	<input type="checkbox"/>	GCLK1	--
EVSYS_10	<input type="checkbox"/>	GCLK1	--
EVSYS_11	<input type="checkbox"/>	GCLK1	--

Close



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