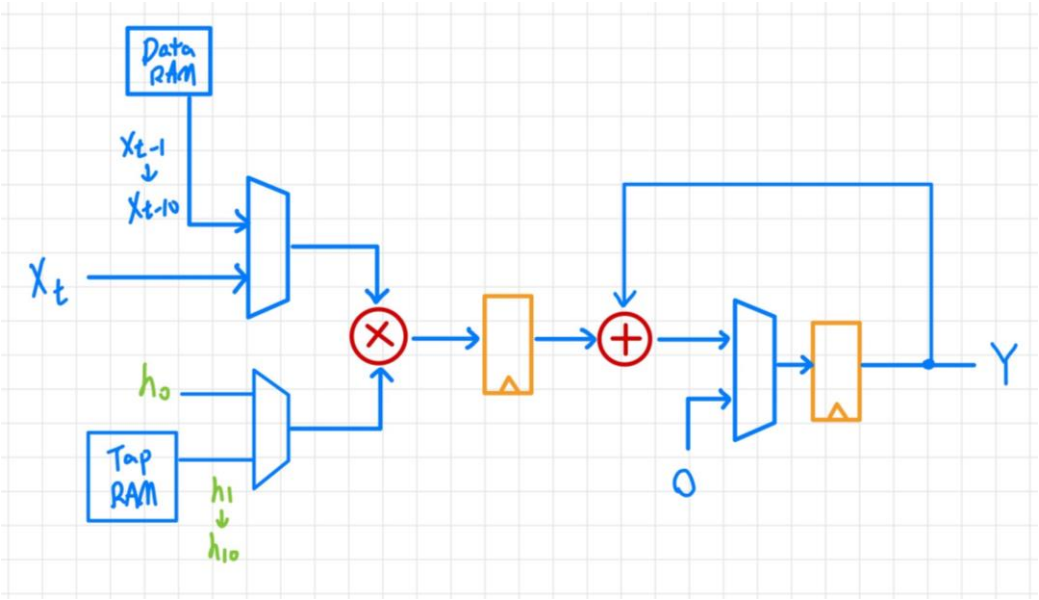
LAB3 – FIR

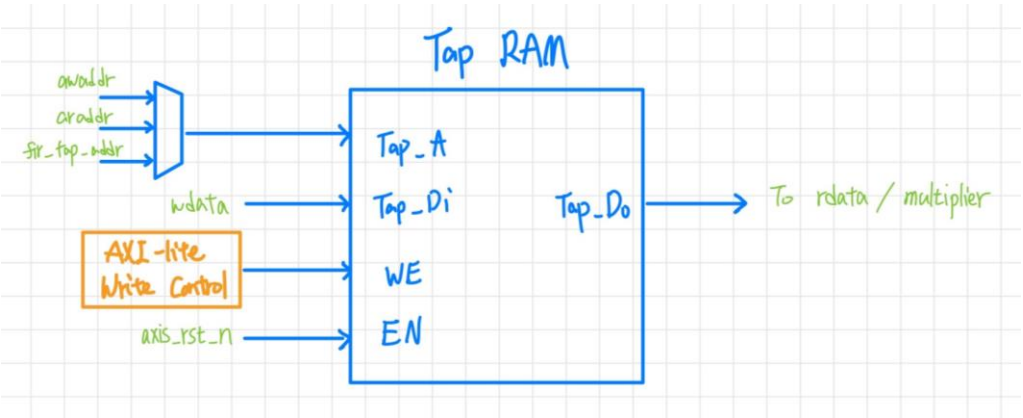
111064559 徐詠祺

- Block Diagram:

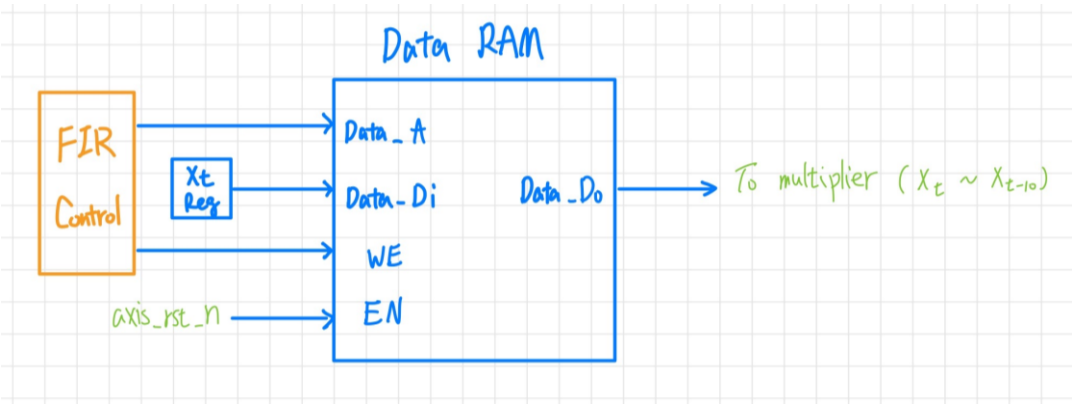
1. **FIR:**



2. **Tap RAM:**



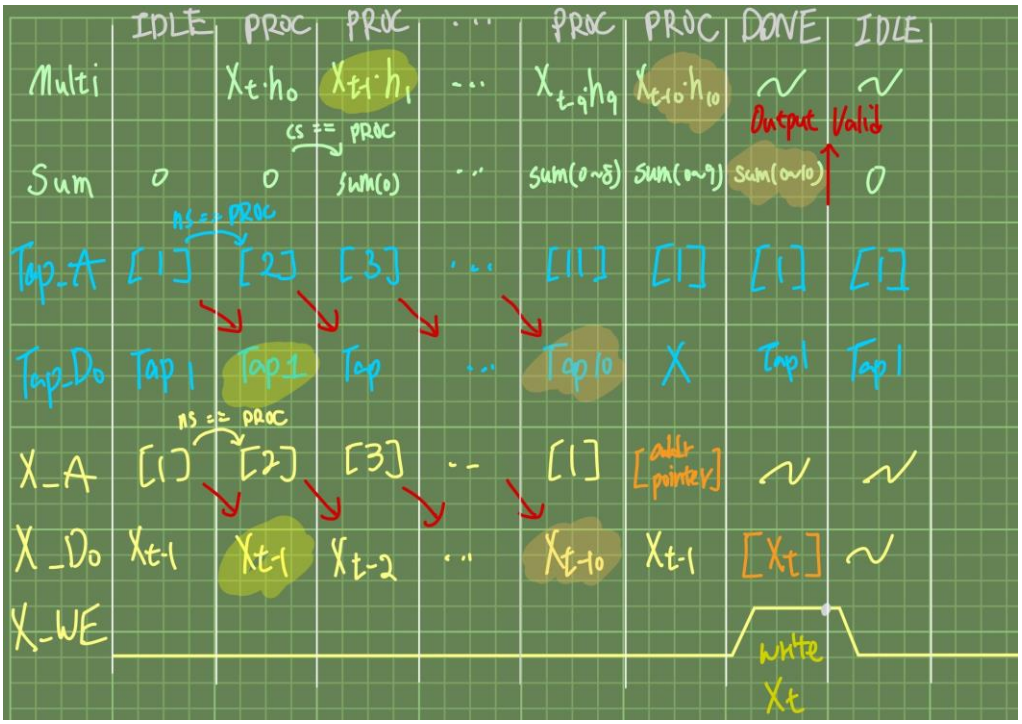
3. **Data RAM:**



- **Describe operation:**
  - **Cycle count for AP_START triggered to AP_DONE triggered:**

    7751

  - **FIR Timing Diagram:**



1. **Tap RAM write:**

   AXI-lite write channel 透過三個 state 的 FSM 來控制，分別是

S_IDLE, S_ADDR, S_DATA，S_ADDR 時會拉起 awready 並等待和 awvalid 握手才進去 S_DATA，S_DATA 會拉起 wready 並等待 awvalid 握手，在 address 握手時我會把 address 暫時存進一個 register 中用來判斷該 address 是否寫入的目的地為 Tap RAM，並在 data 握手時根據目的地決定是否拉起 Tap RAM WE 寫入該筆 data。

2. **Tap RAM access for computation:**

由於我在設計 FIR 時希望在時序上為達到能在 12 個 cycle (2 stage pipeline FIR)處理後送出 output data，並且同時考慮 RAM 寫入 address 後下一個 posedge 才能拿到對應的 data，為了滿足 12 個 cycle 目的， FIR 從 IDLE 進到 PROC 的 posedge，乘法 register 便須存進$X_t \times h_0$，並在下一個 posedge(1st PROC)存進$X_{t-1} \times h_1$，再下一個 posedge(2st PROC)存進$X_{t-2} \times h_2$，以此類推，因此需要在 FIR 狀態為 idle 時就對 Tap_A 輸入 h1 的 addr，但同個 edge 乘法器又要吃 h0 來做$X_t \times h_0$，因此會需要一個 h0 的 register 來滿足在 IDLE 到 PROC 的 posedge 能完成$X_t \times h_0$，同時下個 posedge 又能完成$X_{t-1} \times h_1$的情況，所以 Tap_A 會由 0x24 開始，且每個 cycle+4 直到完成計算。

3. **Data RAM write:**

同上述時序問題，且 FIR IDLE 到 PROC 的原因便是 X input 握手完

成，因此我在 IDLE 進 PROC 的 posedge 時就要對 DATA_A 輸出X_{t-1}的 addr，因此需要先把X_t先用 register 存起來等到倒數最後一個 PROC 時(乘法器已經完成 11 個 tap 和 X 的乘法)再拉起 DATA_WE 寫入下一筆 DATA RAM addr。

4. Data RAM access for computation:

   由於每次的 FIR 計算會需要X_t到X_{t-10}，因此我設計了一個 address pointer 來指向下一筆 X input 要寫入的位置，並且每次 FIR 計算的 addr 便從 address pointer – 4 開始，並且在每個 cycle – 4 直到計算完成，便可以從 DATA RAM 中取出X_{t-1}到X_{t-10}，此外需要考慮到 DATA RAM 的邊界，也就是判斷是不是到了 0x00, 0X24 並相應進行處理。

5. AP_DONE generate:

   AP_DONE 是根據 FIR 該次 input 是否有收到 tlast 來判斷是否為最後一筆 data，因此設置一個 tlast register 來記，並且在 FIR 狀態為 DONE 時根據該 register 決定 AP_DONE 是否為 1。

- **Resource usage:**
  - LUTs: 269
  - Registers: 201

- DSPs (DSP48E1): 3

1. Slice Logic

Site Type	Used	Fixed	Prohibited	Available	Util%
Slice LUTs*	269	0	0	53200	0.51
LUT as Logic	269	0	0	53200	0.51
LUT as Memory	0	0	0	17400	0.00
Slice Registers	201	0	0	106400	0.19
Register as Flip Flop	201	0	0	106400	0.19
Register as Latch	0	0	0	106400	0.00
F7 Muxes	0	0	0	26600	0.00
F8 Muxes	0	0	0	13300	0.00

3. DSP

Site Type	Used	Fixed	Prohibited	Available	Util%
DSPs	3	0	0	220	1.36
DSP48E1 only	3				

4. IO and GT Specific

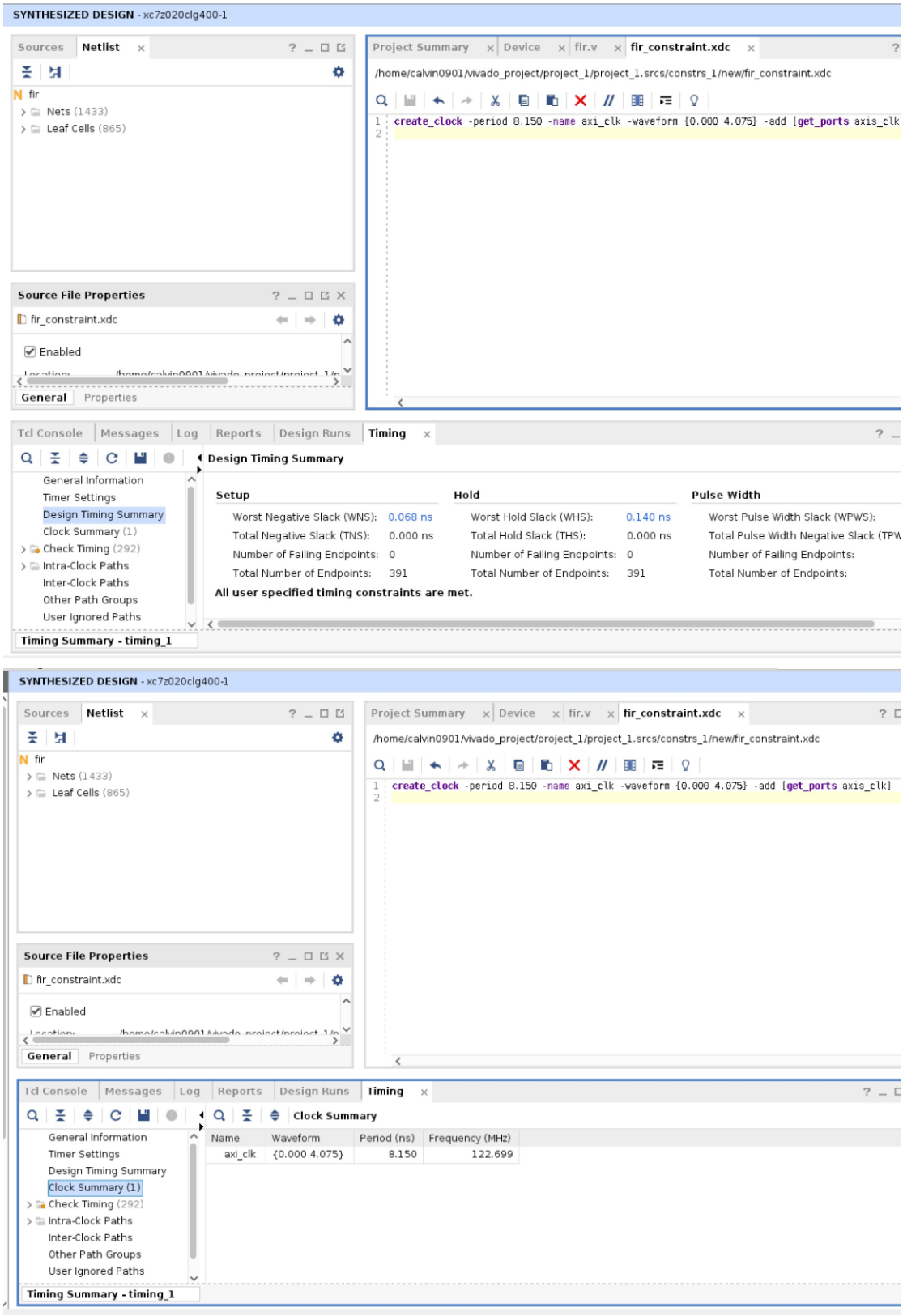
Site Type	Used	Fixed	Prohibited	Available	Util%
Bonded IOB	329	0	0	125	263.20
Bonded IPADs	0	0	0	2	0.00
Bonded IOPADs	0	0	0	130	0.00
PHY_CONTROL	0	0	0	4	0.00
PHASER_REF	0	0	0	4	0.00
OUT_FIFO	0	0	0	16	0.00
IN_FIFO	0	0	0	16	0.00
IDELAYCTRL	0	0	0	4	0.00
IBUFDS	0	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	0	200	0.00
ILOGIC	0	0	0	125	0.00
OLOGIC	0	0	0	125	0.00

```
5. Clocking
-----------

+------------+------+-------+------------+-----------+-------+
|  Site Type | Used | Fixed | Prohibited | Available | Util% |
+------------+------+-------+------------+-----------+-------+
| BUFGCTRL   |    1 |     0 |          0 |        32 |  3.13 |
| BUFIO      |    0 |     0 |          0 |        16 |  0.00 |
| MMCME2_ADV |    0 |     0 |          0 |         4 |  0.00 |
| PLLE2_ADV  |    0 |     0 |          0 |         4 |  0.00 |
| BUFMRCE    |    0 |     0 |          0 |         8 |  0.00 |
| BUFHCE     |    0 |     0 |          0 |        72 |  0.00 |
| BUFR       |    0 |     0 |          0 |        16 |  0.00 |
+------------+------+-------+------------+-----------+-------+
```

- **Timing Report:**

1. Max frequency: 122.699 MHz

```
------------------------------------------------------------------------
| Clock Summary
| -------------
------------------------------------------------------------------------

Clock    Waveform(ns)         Period(ns)      Frequency(MHz)
-----    ------------         ----------      --------------
axi_clk  {0.000 4.075}        8.150           122.699
```



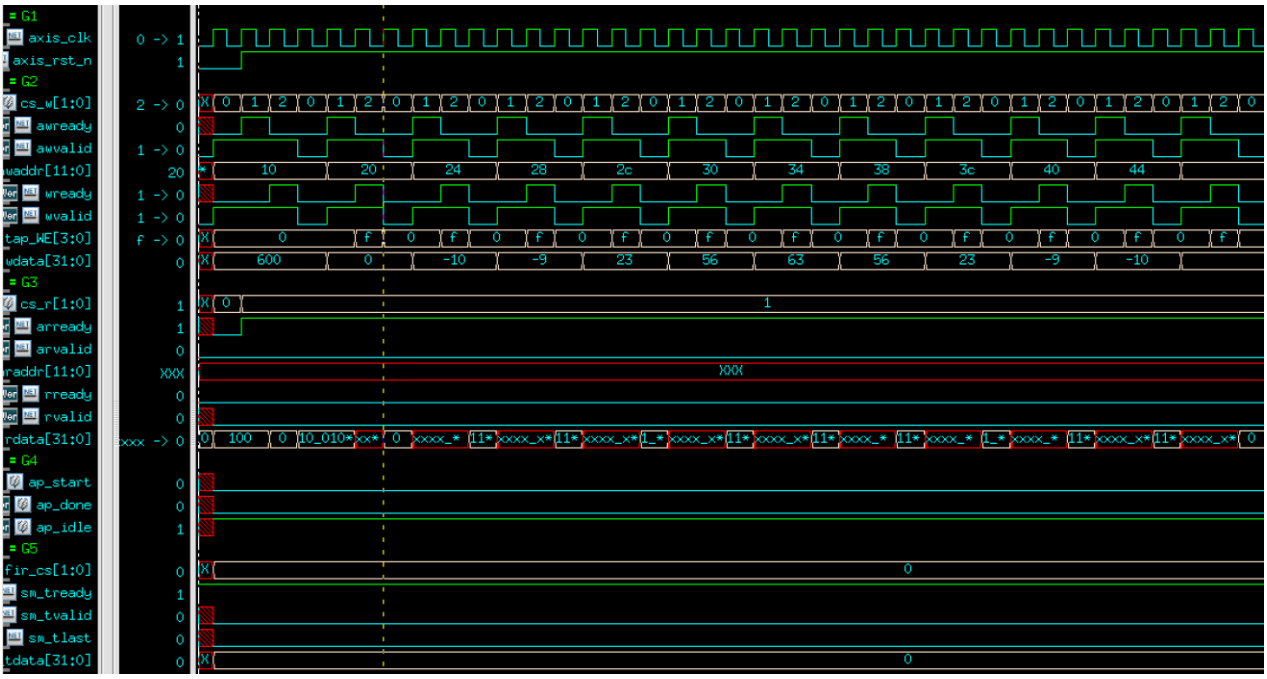
2. Critical path: slack = 0.068 ns

```
Max Delay Paths
--------------------------------------------------------------------------------
Slack (MET) :             0.068ns  (required time - arrival time)
  Source:                 fir_cs_reg[1]/C
                            (rising edge-triggered cell FDRE clocked by axi_clk  {rise@0.000ns fall@4.075ns period=8.150ns})
  Destination:            fir_multi_reg/PCIN[0]
                            (rising edge-triggered cell DSP48E1 clocked by axi_clk  {rise@0.000ns fall@4.075ns period=8.150ns
  Path Group:             axi_clk
  Path Type:              Setup (Max at Slow Process Corner)
  Requirement:            8.150ns  (axi_clk rise@8.150ns - axi_clk rise@0.000ns)
  Data Path Delay:        6.502ns  (logic 4.809ns (73.965%)  route 1.693ns (26.035%))
  Logic Levels:           2  (DSP48E1=1 LUT4=1)
  Clock Path Skew:        -0.145ns (DCD - SCD + CPR)
    Destination Clock Delay (DCD):    2.128ns = ( 10.278 - 8.150 )
    Source Clock Delay      (SCD):    2.456ns
    Clock Pessimism Removal (CPR):    0.184ns
  Clock Uncertainty:      0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter     (TSJ):    0.071ns
    Total Input Jitter      (TIJ):    0.000ns
    Discrete Jitter          (DJ):    0.000ns
    Phase Error              (PE):    0.000ns
```

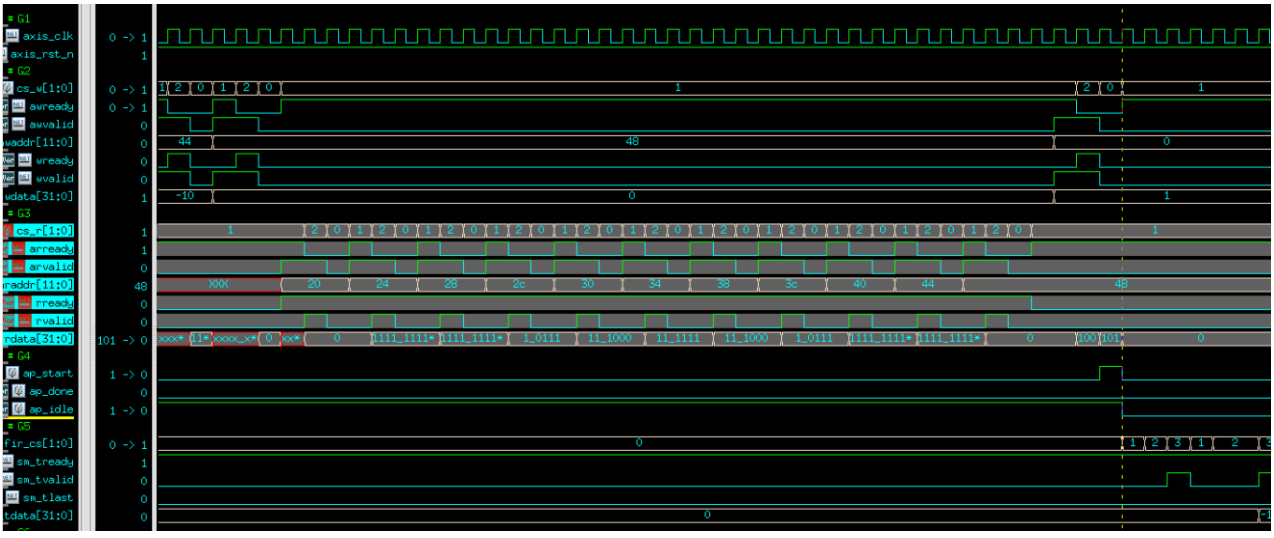
```
  Location             Delay type                Incr(ns)  Path(ns)    Netlist Resource(s)
-------------------------------------------------------------------    -------------------
                     (clock axi_clk rise edge)    0.000     0.000 r
                                                  0.000     0.000 r  axis_clk (IN)
                     net (fo=0)                   0.000     0.000    axis_clk
                                                                   r  axis_clk_IBUF_inst/I
                     IBUF (Prop_ibuf_I_O)         0.972     0.972 r  axis_clk_IBUF_inst/O
                     net (fo=1, unplaced)         0.800     1.771    axis_clk_IBUF
                                                                   r  axis_clk_IBUF_BUFG_inst/I
                     BUFG (Prop_bufg_I_O)         0.101     1.872 r  axis_clk_IBUF_BUFG_inst/O
                     net (fo=203, unplaced)       0.584     2.456    axis_clk_IBUF_BUFG
                     FDRE                                        r  fir_cs_reg[1]/C
-------------------------------------------------------------------    -------------------
                     FDRE (Prop_fdre_C_Q)         0.478     2.934 r  fir_cs_reg[1]/Q
                     net (fo=90, unplaced)        0.838     3.772    fir_cs[1]
                                                                   r  fir_multi0__0_i_1/I1
                     LUT4 (Prop_lut4_I1_O)        0.295     4.067 r  fir_multi0__0_i_1/O
                     net (fo=1, unplaced)         0.800     4.867    fir_multi0__0_i_1_n_0
                                                                   r  fir_multi0__0/A[16]
                     DSP48E1 (Prop_dsp48e1_A[16]_PCOUT[0])
                                                  4.036     8.903 r  fir_multi0__0/PCOUT[0]
                     net (fo=1, unplaced)         0.055     8.958    fir_multi0__0_n_153
                     DSP48E1                                     r  fir_multi_reg/PCIN[0]
-------------------------------------------------------------------    -------------------
```

```
                     (clock axi_clk rise edge)    8.150     8.150 r
                                                  0.000     8.150 r  axis_clk (IN)
                     net (fo=0)                   0.000     8.150    axis_clk
                                                                   r  axis_clk_IBUF_inst/I
                     IBUF (Prop_ibuf_I_O)         0.838     8.988 r  axis_clk_IBUF_inst/O
                     net (fo=1, unplaced)         0.760     9.748    axis_clk_IBUF
                                                                   r  axis_clk_IBUF_BUFG_inst/I
                     BUFG (Prop_bufg_I_O)         0.091     9.839 r  axis_clk_IBUF_BUFG_inst/O
                     net (fo=203, unplaced)       0.439    10.278    axis_clk_IBUF_BUFG
                     DSP48E1                                     r  fir_multi_reg/CLK
                     clock pessimism              0.184    10.461
                     clock uncertainty           -0.035    10.426
                     DSP48E1 (Setup_dsp48e1_CLK_PCIN[0])
                                                 -1.400     9.026    fir_multi_reg
 -------------------------------------------------------------------
                     required time                          9.026
                     arrival time                          -8.958
 -------------------------------------------------------------------
                     slack                                  0.068
```

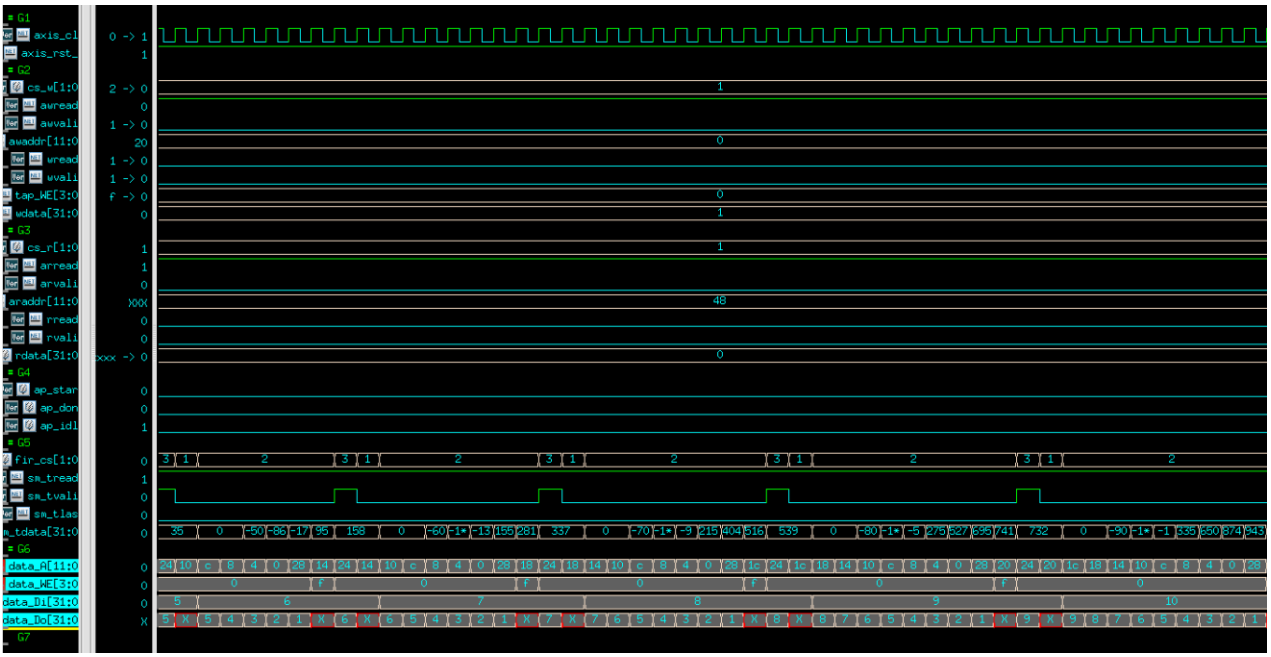
- Simulation Waveform (clock period = 10 ns):
  - Tap RAM write:



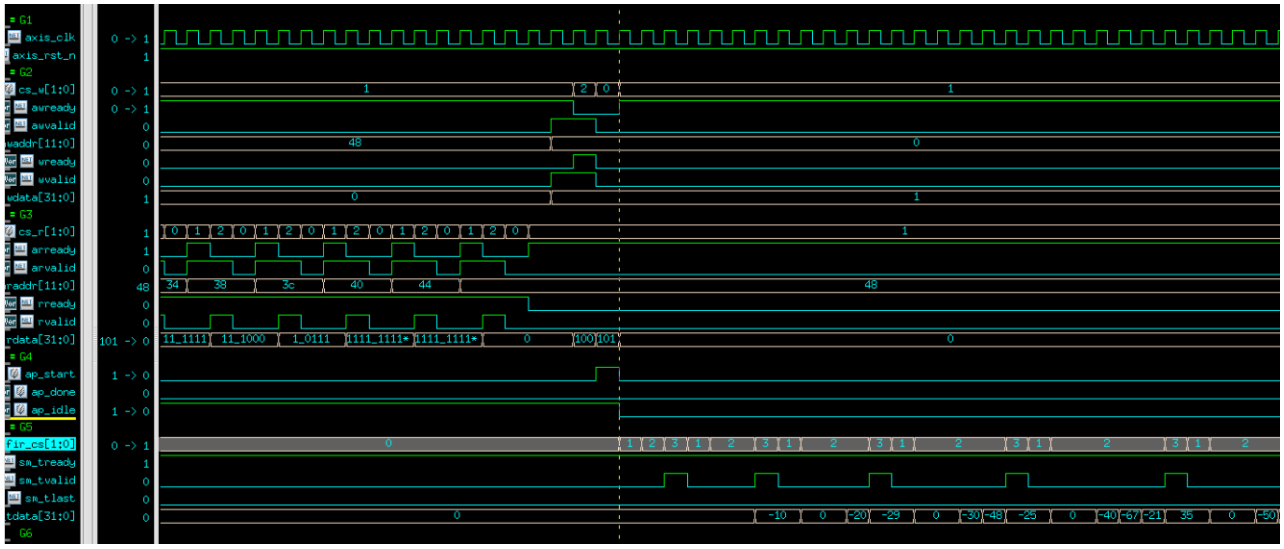
  - Tap RAM read:



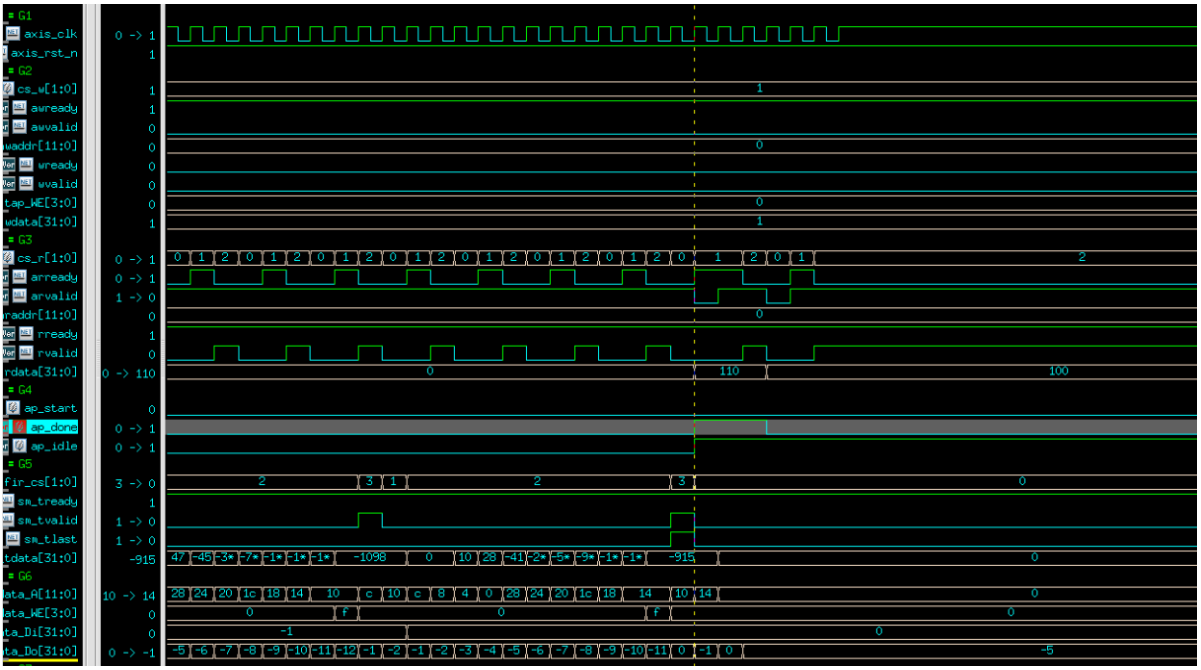
  - Data RAM read/write:



- FIR engine start:



- FIR engine done:


G1
axis_clk
axis_rst_n
G2
cs_w[1:0]
awready
awvalid
waddr[11:0]
wready
wvalid
tap_WE[3:0]
wdata[31:0]
G3
cs_r[1:0]
arready
arvalid
raddr[11:0]
rready
rvalid
rdata[31:0]
G4
ap_start
ap_done
ap_idle
G5
fir_cs[1:0]
sm_tready
sm_tvalid
sm_tlast
tdata[31:0]
G6
data_A[11:0]
data_WE[3:0]
data_Di[31:0]
data_Do[31:0]