SOC design Lab4-1

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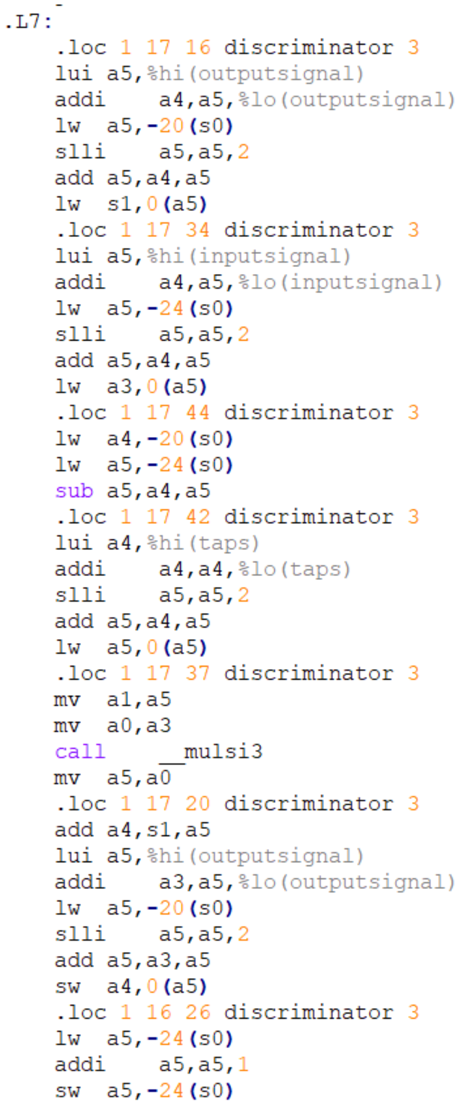
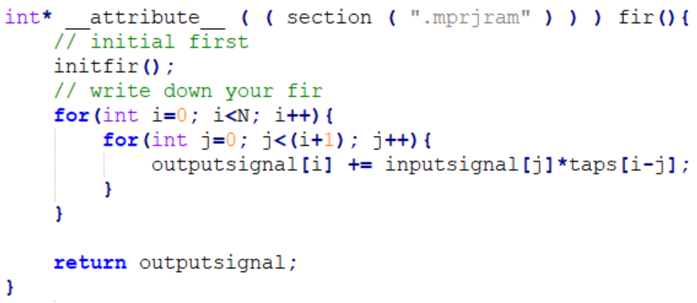
1. Explanation of your firmware code

- How does it execute a multiplication in assembly code

將 a5（來自 taps 陣列）和 a3（來自 inputsignal 陣列）的值作為參數（a1 和 a0）傳遞給一個函數 __mulsi3，這個函數是用來乘以兩個數值的，最後乘法結果被移到 a5 暫存器。



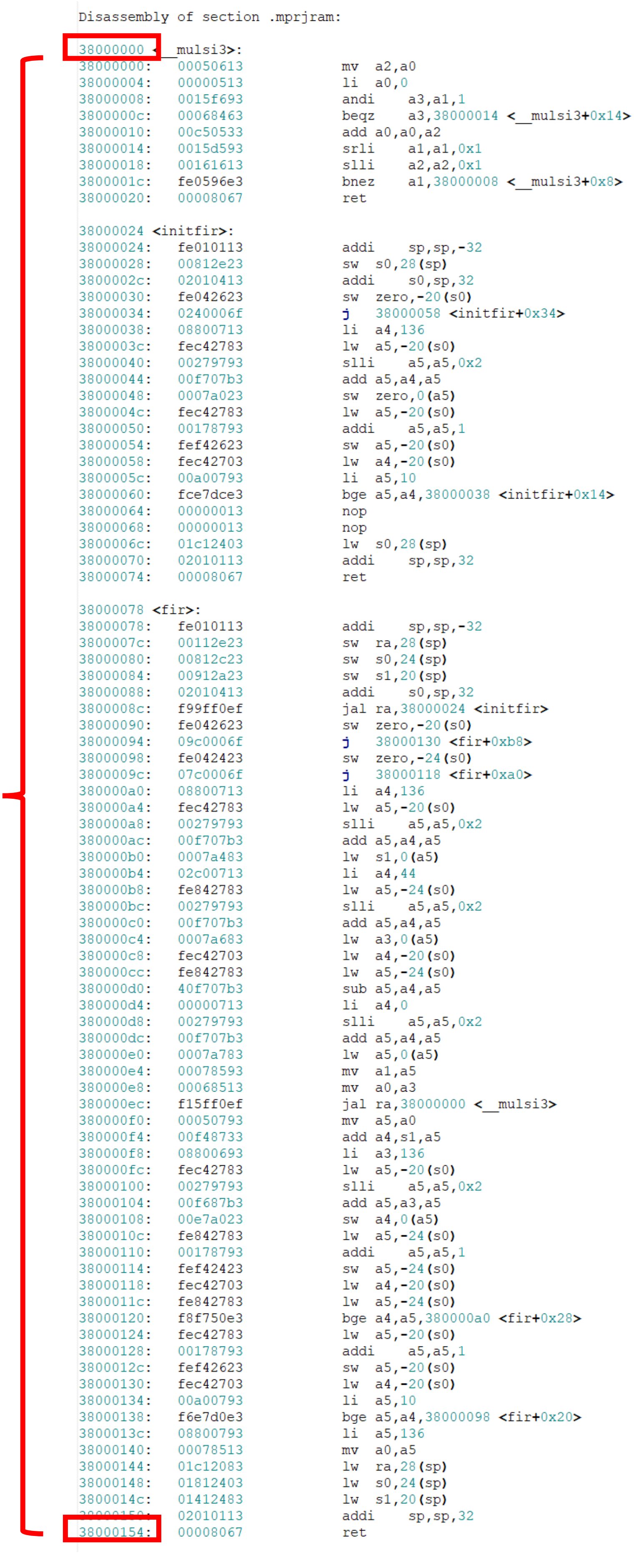
```
.L7:
	.loc 1 17 16 discriminator 3
	lui	a5,%hi(outputsignal)
	addi	a4,a5,%lo(outputsignal)
	lw	a5,-20(s0)
	slli	a5,a5,2
	add	a5,a4,a5
	lw	s1,0(a5)
	.loc 1 17 34 discriminator 3
	lui	a5,%hi(inputsignal)
	addi	a4,a5,%lo(inputsignal)
	lw	a5,-24(s0)
	slli	a5,a5,2
	add	a5,a4,a5
	lw	a3,0(a5)
	.loc 1 17 44 discriminator 3
	lw	a4,-20(s0)
	lw	a5,-24(s0)
	sub	a5,a4,a5
	.loc 1 17 42 discriminator 3
	lui	a4,%hi(taps)
	addi	a4,a4,%lo(taps)
	slli	a5,a5,2
	add	a5,a4,a5
	lw	a5,0(a5)
	.loc 1 17 37 discriminator 3
	mv	a1,a5
	mv	a0,a3
	call	__mulsi3
	mv	a5,a0
	.loc 1 17 20 discriminator 3
	add	a4,s1,a5
	lui	a5,%hi(outputsignal)
	addi	a3,a5,%lo(outputsignal)
	lw	a5,-20(s0)
	slli	a5,a5,2
	add	a5,a3,a5
	sw	a4,0(a5)
	.loc 1 16 26 discriminator 3
	lw	a5,-24(s0)
	addi	a5,a5,1
	sw	a5,-24(s0)
```



```
int* __attribute__ ( ( section ( ".mprjram" ) ) ) fir(){
    // initial first
    initfir();
    // write down your fir
    for(int i=0; i<N; i++){
        for(int j=0; j<(i+1); j++){
            outputsignal[i] += inputsignal[j]*taps[i-j];
        }
    }

    return outputsignal;
}
```

- What address allocate for user project and how many space is required to allocate to firmware code

分配給 mprjram 是從 0x38000000 開始，我們的 firmware code 的大小是到 0x38000154，也就是 340bytes(hex 154)。

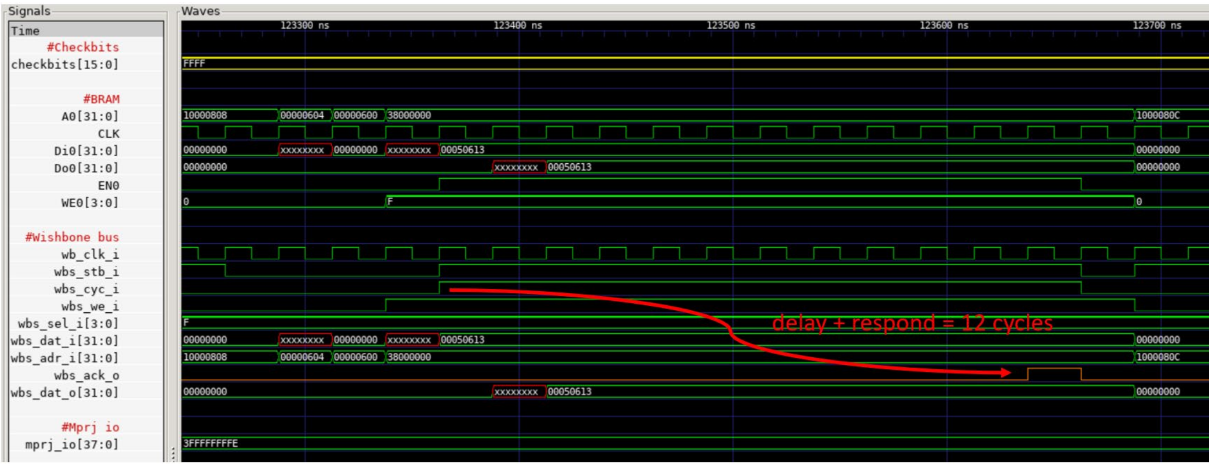


```
Disassembly of section .mprjram:

38000000 <__mulsi3>:
38000000:   00050613            mv  a2,a0
38000004:   00000513            li  a0,0
38000008:   0015f693            andi    a3,a1,1
3800000c:   00068463            beqz    a3,38000014 <__mulsi3+0x14>
38000010:   00c50533            add a0,a0,a2
38000014:   0015d593            srli    a1,a1,0x1
38000018:   00161613            slli    a2,a2,0x1
3800001c:   fe0596e3            bnez    a1,38000008 <__mulsi3+0x8>
38000020:   00008067            ret

38000024 <initfir>:
38000024:   fe010113            addi    sp,sp,-32
38000028:   00812e23            sw  s0,28(sp)
3800002c:   02010413            addi    s0,sp,32
38000030:   fe042623            sw  zero,-20(s0)
38000034:   0240006f            j   38000058 <initfir+0x34>
38000038:   08800713            li  a4,136
3800003c:   fec42783            lw  a5,-20(s0)
38000040:   00279793            slli    a5,a5,0x2
38000044:   00f707b3            add a5,a4,a5
38000048:   0007a023            sw  zero,0(a5)
3800004c:   fec42783            lw  a5,-20(s0)
38000050:   00178793            addi    a5,a5,1
38000054:   fef42623            sw  a5,-20(s0)
38000058:   fec42703            lw  a4,-20(s0)
3800005c:   00a00793            li  a5,10
38000060:   fce7dce3            bge a5,a4,38000038 <initfir+0x14>
38000064:   00000013            nop
38000068:   00000013            nop
3800006c:   01c12403            lw  s0,28(sp)
38000070:   02010113            addi    sp,sp,32
38000074:   00008067            ret

38000078 <fir>:
38000078:   fe010113            addi    sp,sp,-32
3800007c:   00112e23            sw  ra,28(sp)
38000080:   00812c23            sw  s0,24(sp)
38000084:   00912a23            sw  s1,20(sp)
38000088:   02010413            addi    s0,sp,32
3800008c:   f99ff0ef            jal ra,38000024 <initfir>
38000090:   fe042623            sw  zero,-20(s0)
38000094:   09c0006f            j   38000130 <fir+0xb8>
38000098:   fe042423            sw  zero,-24(s0)
3800009c:   07c0006f            j   38000118 <fir+0xa0>
380000a0:   08800713            li  a4,136
380000a4:   fec42783            lw  a5,-20(s0)
380000a8:   00279793            slli    a5,a5,0x2
380000ac:   00f707b3            add a5,a4,a5
380000b0:   0007a483            lw  s1,0(a5)
380000b4:   02c00713            li  a4,44
380000b8:   fe842783            lw  a5,-24(s0)
380000bc:   00279793            slli    a5,a5,0x2
380000c0:   00f707b3            add a5,a4,a5
380000c4:   0007a683            lw  a3,0(a5)
380000c8:   fec42703            lw  a4,-20(s0)
380000cc:   fe842783            lw  a5,-24(s0)
380000d0:   40f707b3            sub a5,a4,a5
380000d4:   00000713            li  a4,0
380000d8:   00279793            slli    a5,a5,0x2
380000dc:   00f707b3            add a5,a4,a5
380000e0:   0007a783            lw  a5,0(a5)
380000e4:   00078593            mv  a1,a5
380000e8:   00068513            mv  a0,a3
380000ec:   f15ff0ef            jal ra,38000000 <__mulsi3>
380000f0:   00050793            mv  a5,a0
380000f4:   00f48733            add a4,s1,a5
380000f8:   08800693            li  a3,136
380000fc:   fec42783            lw  a5,-20(s0)
38000100:   00279793            slli    a5,a5,0x2
38000104:   00f687b3            add a5,a3,a5
38000108:   00e7a023            sw  a4,0(a5)
3800010c:   fe842783            lw  a5,-24(s0)
38000110:   00178793            addi    a5,a5,1
38000114:   fef42423            sw  a5,-24(s0)
38000118:   fec42703            lw  a4,-20(s0)
3800011c:   fe842783            lw  a5,-24(s0)
38000120:   f8f750e3            bge a4,a5,380000a0 <fir+0x28>
38000124:   fec42783            lw  a5,-20(s0)
38000128:   00178793            addi    a5,a5,1
3800012c:   fef42623            sw  a5,-20(s0)
38000130:   fec42703            lw  a4,-20(s0)
38000134:   00a00793            li  a5,10
38000138:   f6e7d0e3            bge a5,a4,38000098 <fir+0x20>
3800013c:   08800793            li  a5,136
38000140:   00078513            mv  a0,a5
38000144:   01c12083            lw  ra,28(sp)
38000148:   01812403            lw  s0,24(sp)
3800014c:   01412483            lw  s1,20(sp)
38000150:   02010113            addi    sp,sp,32
38000154:   00008067            ret
```

2. Interface between BRAM and wishbone

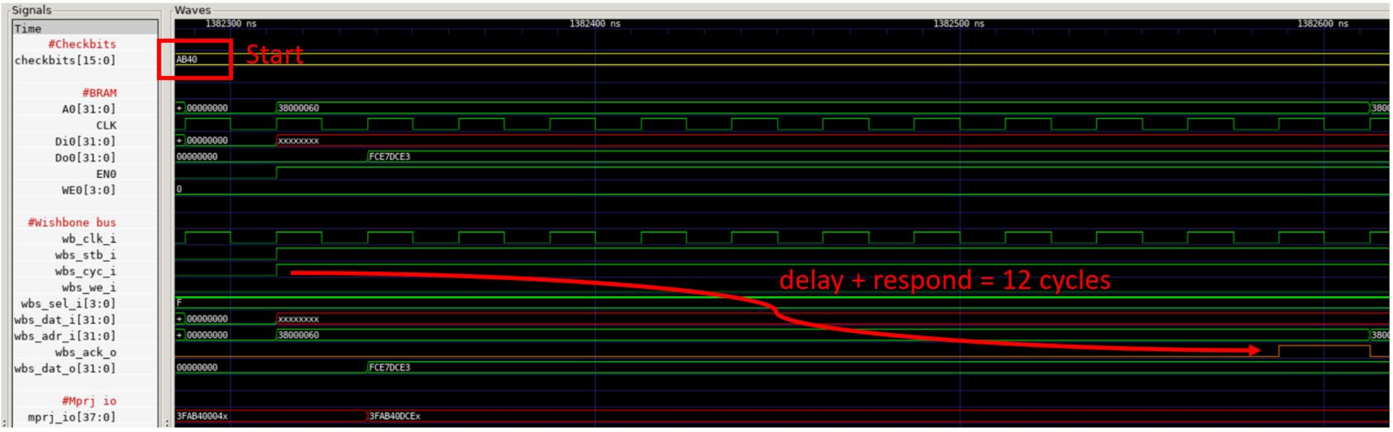
- Waveform

Write bram:



delay + respond = 12 cycles

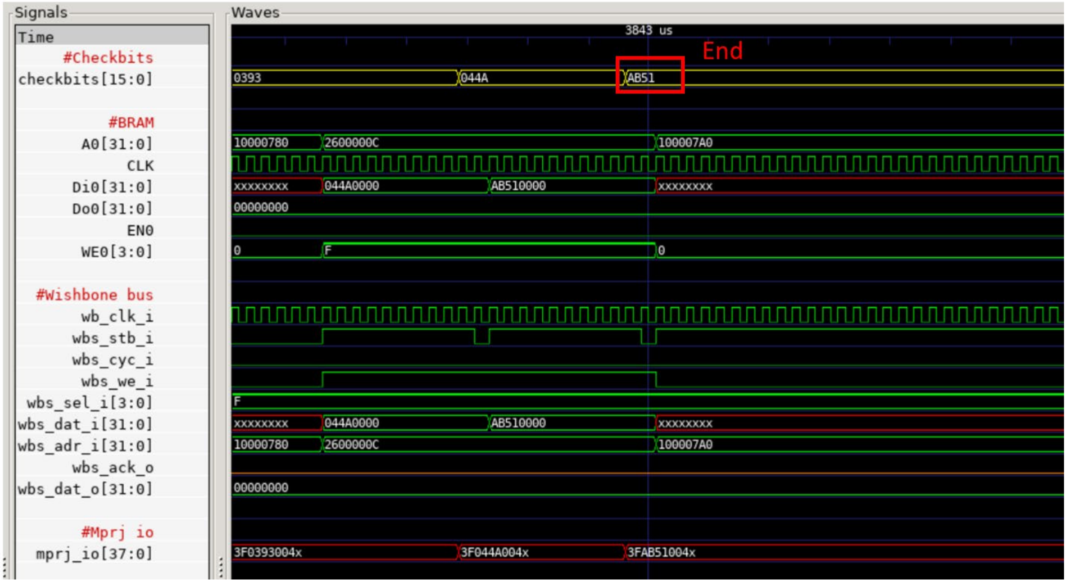
AB40:



Start

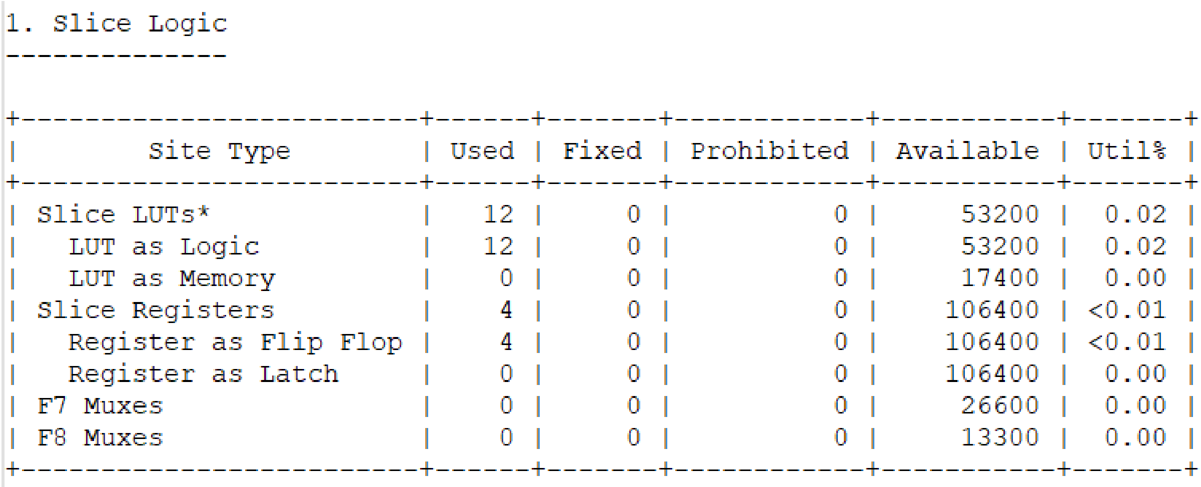
delay + respond = 12 cycles

AB51:



End

3. Synthesis report



```
1. Slice Logic
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+-------------------------+------+-------+------------+-----------+-------+
|        Site Type        | Used | Fixed | Prohibited | Available | Util% |
+-------------------------+------+-------+------------+-----------+-------+
| Slice LUTs*             |   12 |     0 |          0 |     53200 |  0.02 |
|   LUT as Logic          |   12 |     0 |          0 |     53200 |  0.02 |
|   LUT as Memory         |    0 |     0 |          0 |     17400 |  0.00 |
| Slice Registers         |    4 |     0 |          0 |    106400 | <0.01 |
|   Register as Flip Flop |    4 |     0 |          0 |    106400 | <0.01 |
|   Register as Latch     |    0 |     0 |          0 |    106400 |  0.00 |
| F7 Muxes                |    0 |     0 |          0 |     26600 |  0.00 |
| F8 Muxes                |    0 |     0 |          0 |     13300 |  0.00 |
+-------------------------+------+-------+------------+-----------+-------+
```

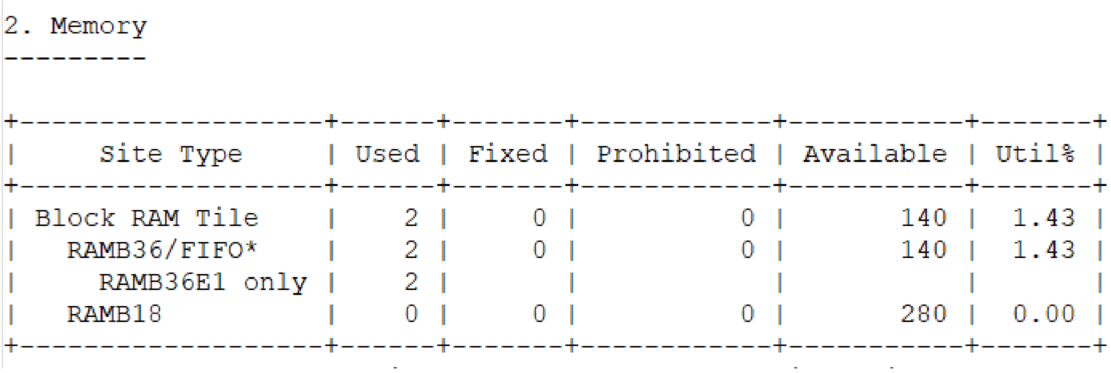

```
2. Memory
---------

+-------------------+------+-------+------------+-----------+-------+
|     Site Type     | Used | Fixed | Prohibited | Available | Util% |
+-------------------+------+-------+------------+-----------+-------+
| Block RAM Tile    |    2 |     0 |          0 |       140 |  1.43 |
|   RAMB36/FIFO*    |    2 |     0 |          0 |       140 |  1.43 |
|     RAMB36E1 only |    2 |       |            |           |       |
|   RAMB18          |    0 |     0 |          0 |       280 |  0.00 |
+-------------------+------+-------+------------+-----------+-------+
```