1. Calculations

To design a CMOS circuit consisting of a two-input NOR gate. First, we know the following circuit diagram and data:

V_{DD}	4 V
V_{Tn}	0.25 V
V_{Tp}	-0.25 V
C_o	$5 \times 10^{-4}\ Fm^{-2}$
Electron mobility	$0.1\ m^2V^{-1}s^{-1}$
Hole mobility	$0.05\ m^2V^{-1}s^{-1}$
Minimum feature size	$0.2\ \mu m$
Maximum alignment error	$0.1\ \mu m$

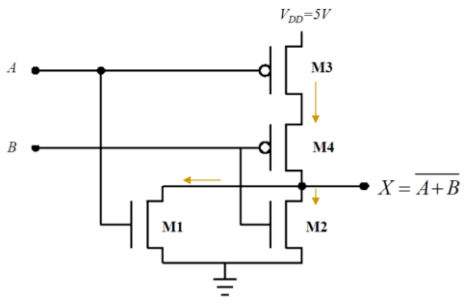
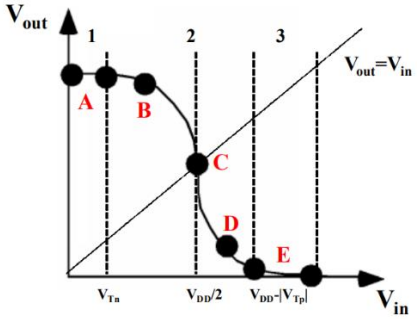


Fig.1. The CMOS NOR gate with two-inputs [1]



According to the lecture hints, the operating point of MOSFET is assumed to be point C. Therefore:

$$V_A = V_B = V_{out} = \frac{V_{DD}}{2} = 2\ V$$

First, we assume that M3 works in the linear region and M4 works in the saturation region. And, we already know the current relationship for each transistor as follows: $I_{d3} = I_{d4} = 2I_{d1} = 2I_{d2}$. Second, the equation for the current in the linear region is: $I_D = \beta[(V_{GS} - V_T) \times V_{DS} - \frac{V_{DS}^2}{2}]$. The equation for the current in the saturation region is: $I_D = \frac{\beta}{2}(V_{GS} - V_T)^2$ Thus:

$$I_{D3} = I_{D4} = \beta[(V_{GS3} - V_{Tp}) \times V_{DS3} - \frac{V_{DS3}^2}{2}] = \frac{\beta}{2}(V_{GS4} - V_{Tp})^2$$

We assume that the voltage difference between M3 and M4 is V_1, then we know

$V_{GS3} = 2 - 4 = -2V, V_{DS3} = (V_1 - 4)V, V_{GS4} = (-2 - V_1)V$.

Thus, we can obtain the following equation:

$$\beta[(-2 - (-0.25)) \times (V_1 - 4) - \frac{(V_1 - 4)^2}{2}] = \frac{\beta}{2}((-2 - V_1) - (-0.25))^2$$

Solving the equation gives: $V_1 = 0.25V$

We can determine the operating area of each transistor based on the PMOS operating area determination conditions, as shown in the following table:

Regime	N-MOS	P-MOS
Cut off	$V_{GS} > V_T$	$V_{GS} < V_T$
Linear	$V_{DS} < V_{GS} - V_T$	$V_{DS} > V_{GS} - V_T$
Saturation	$V_{DS} > V_{GS} - V_T$	$V_{DS} < V_{GS} - V_T$

For M3 MOSFET, V_{DS} (-3.75) < V_{GS} (-2) - V_T (-0.25). Therefore, M3 works in the saturation region, this is contrary to our previous assumptions. However, M3 does not work in the linear region but should work in the saturation region.

For M4, V_{DS} (-3.75) < V_{GS} (-2.25) - V_T (-0.25). Thus, M4 is in the saturation region.

For M1, V_{DS} (2) > V_{GS} (2) - V_T (0.25). Therefore, M1 works in the saturation region.

For M2, V_{DS} (2) > V_{GS} (2) - V_T (0.25). Therefore, M2 works in the saturation region.

Thus: $I_{d1} = I_{d2} = \frac{\beta}{2}(V_{GS} - V_{Tn})^2$, and $2I_{d1} = 2I_{d2} = I_{d3} = I_{d4},\ \beta \equiv \mu C_O \frac{W}{L}$

Therefore: $2I_{d2} = I_{d4} = 2\mu_n C_o \frac{W_n}{L_n}(V_{GS2} - V_{Tn})^2 = \mu_p C_o \frac{W_p}{L_p}(V_{GS4} - V_{Tp})^2$

Simplification gives: $4\frac{W_n}{L_n} = \frac{W_p}{L_p}$, In addition, there are two transistors connected in parallel, doubling the length. To ensure that the β remains the same, so the width is also doubled. Since there are two inputs, they are related as follows:

$$8\frac{W_n}{L_n} = \frac{W_p}{L_p}$$

According to the lecture hints, we can define the channel length of N-MOS and P-MOS as $2\lambda\ i.e.,\ L_n = L_p = 2\lambda$. And we can define the width of the N-MOS as $4\lambda, i.e., W_n = 4\lambda$. Furthermore, based on the ratio between $\frac{W_n}{L_n}$ and $\frac{W_p}{L_p}$, we can conclude that $W_p = 8 \times W_n = 8 \times 4\lambda = 32\lambda$. Finally, we know that the minimum feature size is 0.2 μm, so the channel length L should be 0.2 μm, which means that λ should be 0.1 μm.

2. Layout

- **Design:**

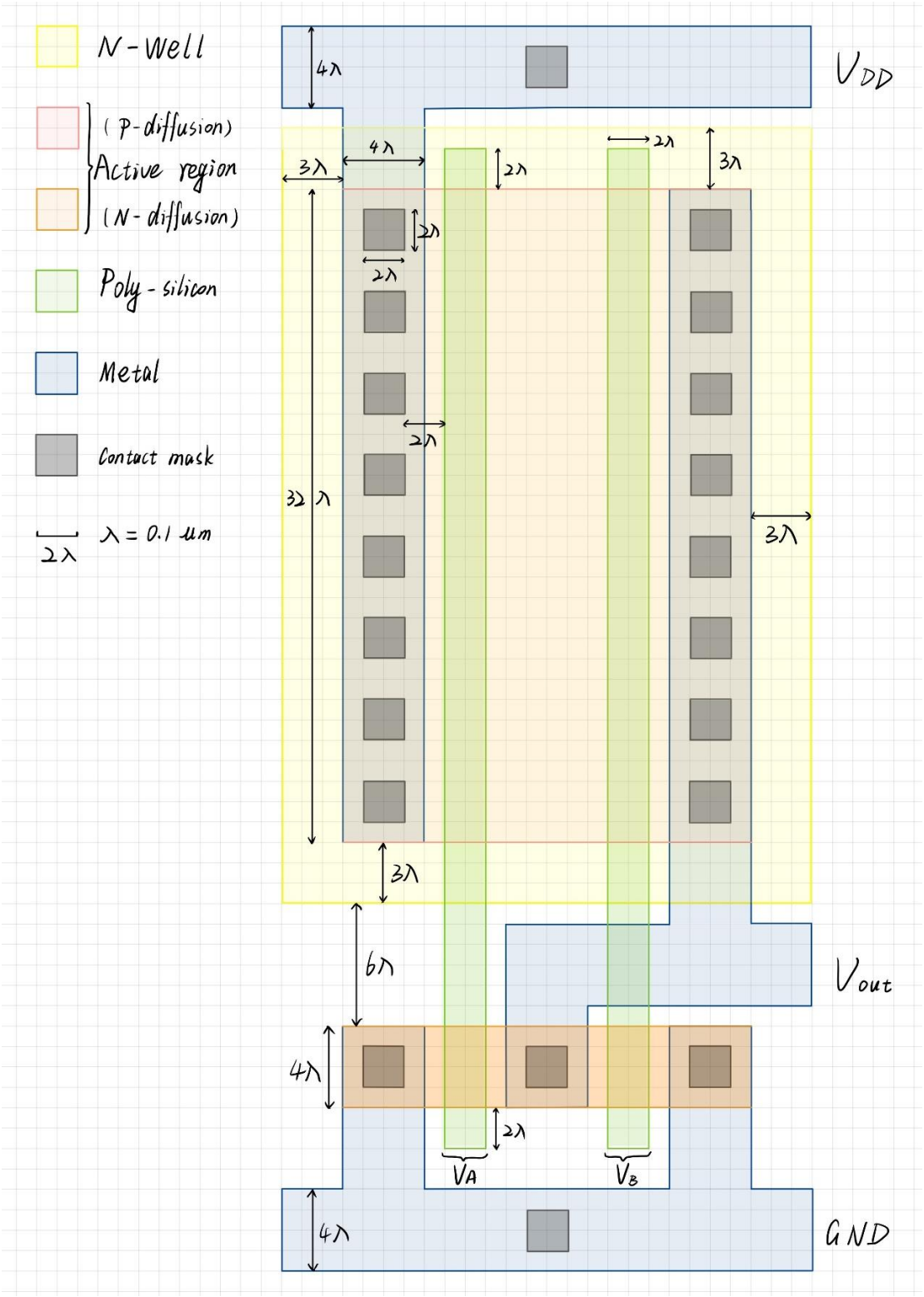


Fig.2. The design for two input NOR gate

- **The design rules and explanation:**

For N-well region, the minimum distance between N-well region and active region of PMOS must at least 3λ [2]. And, the minimum distance between N-well region and active region of NMOS must at least 5λ, this is to prevent N-well region diffusion into the n-channel leading to a short circuit [2].

For active region, the contact must be surrounded by the active region and have a width of at least λ to prevent short circuits [2].

For poly-silicon region, it must extend from the active region at least 2λ. The minimum distance between the edge of the active region and poly-silicon must be λ. The minimum width of poly-silicon should be 2λ [2].

For metal, the minimum width of metal is 3λ. The minimum width of V_{DD} and GND is 4λ, and the minimum width of the V_{out} is 3λ. Metal must be overlapped with contacts [2].

For contact, the minimum size of the active region contacts is 2λ and the spacing between them is 2λ. To prevent short circuits, the minimum distance between the contact and the edge of the active region is λ [2].

References:

[1] I. MITROVIC, "ELEC212_SlidesLects7-9," canvas. [Online]. Available: https://liverpool.instructure.com/courses/60802/pages/week-7-lectures-8-and-9-cmos-circuits-+-design-assignment-2023?module_item_id=1689286. [Accessed: 26-Apr-2023].
[2] I. MITROVIC, "REVISION + Design Assignment," canvas. [Online]. Available: https://liverpool.instructure.com/courses/60802/files/9139976?module_item_id=1716440. [Accessed: 26-Apr-2023].