Jinsong Zhang

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Education

University of California, Santa Barbara *Santa Barbara, USA* *Sep 2024 - Present*
M.S. in Computer Engineering - GPA: 3.9/4.0
University of Liverpool *Liverpool, UK* *Sep 2022 - Jun 2024*
B.Eng. in Electrical and Electronic Engineering - GPA: 3.7/4.0
Xi'an Jiaotong-Liverpool University *Suzhou, China* *Sep 2020 - Jun 2022*
B.Eng. in Electronic Science and Technology - GPA: 3.5/4.0

Skills

Programming: C/C++, Verilog, Python (PyTorch, OpenCV), MATLAB, Assembly, HTML, CSS
Software: Vivado, Quartus, Vitis, Cadence, VS Code, MATLAB, PyCharm, Multisim

Research Experience

Low-precision tensorized transformer training *University of California, Santa Barbara, USA* *Sep 2024 – Present*
Researcher, *Research Assistant*
Developed and integrated a Tucker Tensor Layer into Fully Connected Neural Networks to improve parameter efficiency and computational cost.
- Designed and implemented tensor decomposition techniques to reduce the dimensionality of weight matrices while maintaining model accuracy.
- Conducted extensive experiments on MNIST & CIFAR-10 datasets to evaluate the performance of Tucker tensorized layers in comparison to standard fully connected layers.

YOLOv5s-Powered Vision System for Distributing Robot Swarms *Westlake University, China* *Jun 2023 – Sep 2023*
Researcher, *Visiting Student*
Developed and implemented an innovative vision system, integrating the YOLO v5s model with ROS (Robot Operating System), for real-time object detection within a distributed robot swarm.
- Curated a comprehensive object detection dataset by leveraging ROS in conjunction with cameras.
- Conducted YOLOv5s model training with a custom dataset and deployed Triton Inference Servers with YOLO v5s model on each robot in the swarm.
- Reduced latency by converting image preprocessing and ROS topic publishing Python code to C++. Implemented object detection for a swarm of robots, enhancing overall intelligence and coordination capabilities.

Real-time Slope Perception Module for UAV *Westlake University, China* *May 2023 – Jul 2023*
Researcher, *Visiting Student*
Designed and implemented a cutting-edge perception module for unmanned aerial vehicles (UAVs) utilizing a combination of four laser distance sensors and an Inertial Measurement Unit (IMU).
- Developed a sophisticated slope perception algorithm tailored for real-time monitoring of inclined surfaces.
- Developed a visually intuitive real-time interface to communicate with the microcontroller, facilitating the monitoring and analysis of slope data.
- Integrated the slope perception algorithm seamlessly with the sensor module using Keil, enabling UAVs to perceive and navigate inclined terrains in real-time.

Projects

Recurrent Neural Network based Aircraft Trajectory Prediction Final *Year Project* *Oct 2023 – May 2024*
Implemented Recurrent Neural Networks (RNNs) using PyTorch, specifically focusing on Long Short-Term Memory (LSTM) and Gated Recurrent Unit (GRU) models, to predict aircraft trajectories based on ADS-B data.
- Processed the Aircraft Localization Competition dataset by handling data imputation, cleaning, and structuring to ensure high-quality inputs for model training.
- Designed and tested both single-feature and multi-feature input-output models to assess the impact of feature selection on prediction accuracy.

Image Processing for Object Recognition *Year 2 Project* *Sep 2022 - May 2023*
Developed and implemented an autonomous visual tracking system on a small car using Jetson Nano as the main processing unit, integrating computer vision, deep learning and automatic control technologies.
- Developed a small car equipped with a camera for perception capabilities and generated a runway dataset through camera-based trials.
- Conducted training sessions for the ResNet model using the custom dataset, enabling the small car to make informed decisions for autonomous navigation and path following based on visual inputs.
- Implemented a PID controller as the motor control module to ensure precise and responsive adjustments, facilitating stable and accurate movements in accordance with the visual feedback.

Custom 32-bit 5-Stage Pipelined RISC-V Processor VLSI *Project* *Sep 2024 – Dec 2024*
Designed and implemented a custom 32-bit RISC-V processor featuring a 5-stage pipeline architecture to enhance instruction throughput and processing efficiency.
- Developed the processor using Verilog, ensuring modularity and clarity in the RTL design for ease of understanding and future scalability.
- Created a single-cycle processor circuit using Cadence tools, laying the groundwork for the pipelined version and facilitating performance comparisons.