# Jinsong Zhang

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## Education

**University of Liverpool** *Liverpool, UK* *Sep 2022 - June 2024*
B.Eng. in Electrical and Electronic Engineering
**Xi'an Jiaotong-Liverpool University** *Suzhou, China* *Sep 2020 - June 2022*
B.Eng. in Electronic Science and Technology
Major GPA: 3.69/4.00

## Computer Skills

**Programming:** Linux, ROS, C/C++, Verilog, Python, MATLAB, Assembly, HTML, CSS
**Software:** Git, VS Code, MATLAB, PyCharm, Anaconda, Jupyter Notebook, Arduino, Quartus II, Multisim

## Research Experience

**FPGA Accelerated Convolutional Neural Network for Digit Recognition** *University of Liverpool, UK* *Fall 2023*
Researcher, *Undergraduate Research Fellowship*
Designed and implemented a Convolutional Neural Network (CNN) using Verilog on ALTERA's FPGA board for real-time handwritten digit recognition using the MNIST dataset.

- Developed a customized CNN architecture optimized for real-time processing on FPGA hardware.
- Created a seamless integration between the FPGA board and a display module, enabling real-time visualization of handwritten digit recognition results on the FPGA display.
- Utilized ALTERA's FPGA resources efficiently to achieve high-performance and low-latency inference for real-time applications.

**YOLOv5s-Powered Vision System for Distributing Robot Swarms** *Westlake University, China* *Summer 2023*
Researcher, *Visiting Student*
Developed and implemented an innovative vision system using YOLOv5s model for real-time object detection within a distributed robot swarm.

- Curated a comprehensive object detection dataset, encompassing humans and robots, using ROS (Robot Operating System) and cameras.
- Conducted YOLOv5s model training with a custom dataset and deployed Triton Inference Servers with YOLO v5s model on each robot in the swarm.
- Implemented object detection functionality for the robot swarm through the collaborative integration of ROS and Triton Inference Servers, enhancing the overall intelligence and coordination capabilities.

**Real-time Slope Perception Module for UAV** *Westlake University, China* *Summer 2023*
Researcher, *Visiting Student*
Designed and implemented a cutting-edge perception module for unmanned aerial vehicles (UAVs) utilizing a combination of four laser distance sensors and an Inertial Measurement Unit (IMU).

- Developed a sophisticated slope perception algorithm tailored for real-time monitoring of inclined surfaces.
- Created a visually intuitive real-time interface for monitoring and analyzing slope data.
- Integrated the slope perception algorithm seamlessly with the sensor module, enabling UAVs to perceive and navigate inclined terrains in real-time.

**Comparative Analysis of FedAvg in Non-IID dataset** *Xi'an Jiaotong-Liverpool University, China* *Summer 2023*
Undergraduate Researcher, *Summer Undergraduate Research Fellowship*
Conducted experiments and evaluations on the Federated Averaging (FedAvg) algorithm using the MNIST dataset to compare the performance of various methods in handling non-identically distributed data.

- Implemented and executed experiments applying FedAvg algorithm to assess its efficacy in federated learning scenarios, specifically focusing on non-iid data distributions.
- Analyzed and compared the performance of FedAvg with different approaches, shedding light on its suitability for scenarios involving non-identically distributed data in the context of MNIST digit recognition.

## Projects

**Image Processing for Object Recognition** *Year 2 Project* *Fall 2022*
Developed and implemented an autonomous visual tracking system on a small car using Jetson Nano as the main processing unit, integrating computer vision, deep learning and automatic control technologies.

- Developed a small car equipped with a camera as a perception module, capturing and assembling a dataset of road information.
- Conducted training sessions for the ResNet model using the custom dataset, enabling the small car to make informed decisions for autonomous navigation and path following based on visual inputs.
- Implemented a PID controller as the motor control module to ensure precise and responsive adjustments, facilitating stable and accurate movements in accordance with the visual feedback.

**UART Serial Communication Implemented in Verilog HDL on FPGA** *Digital System Design* *Spring 2023*
Developed and implemented a versatile UART communication module in Verilog, seamlessly integrating transmitter and receiver functionalities on an Altera FPGA board for establishing reliable bidirectional communication with a computer.

- Crafted dedicated transmit and receive modules for UART serial communication, incorporating essential components such as shift registers, baud rate generators, and controllers to facilitate efficient data transmission and reception.
- Utilized ModelSim to meticulously simulate and analyze each module, ensuring optimal stability, robustness, and portability of the transmission and reception processes.