

# Jinsong Zhang

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## Education

<b>University of Liverpool</b> <i>Liverpool, UK</i>	<i>Sep 2022 - Jun 2024</i>
B.Eng. in Electrical and Electronic Engineering	
<b>Xi'an Jiaotong-Liverpool University</b> <i>Suzhou, China</i>	<i>Sep 2020 - Jun 2022</i>
B.Eng. in Electronic Science and Technology	
Major GPA: 3.69/4.00	

## Skills

**Programming:** Linux, ROS, C/C++, Verilog, Python, MATLAB, Assembly, HTML, CSS

**Software:** Git, VS Code, MATLAB, PyCharm, Anaconda, Jupyter Notebook, Arduino, Quartus II, Multisim

## Research Experience

<b>FPGA Accelerated CNN for Digit Recognition</b> <i>University of Liverpool, UK</i>	<i>Nov 2022 – Nov 2023</i>
Researcher, <i>Undergraduate Research Fellowship</i>	
Designed and implemented a Convolutional Neural Network (CNN) using Verilog on Altera's FPGA board for real-time handwritten digit recognition using the MNIST dataset.	
<ul style="list-style-type: none"><li>Designed fixed-point computation in place of floating-point operations for easy implementation on FPGA.</li><li>Implemented a Register-Transfer Level CNN on FPGA using ReLU activation, optimizing by reducing the number of fully connected layers and filters per convolutional layer.</li><li>Utilized FPGA efficiently to achieve high-performance and low-latency inference for real-time applications.</li></ul>	
<b>YOLOv5s-Powered Vision System for Distributing Robot Swarms</b> <i>Westlake University, China</i>	<i>Jun 2023 – Sep 2023</i>
Researcher, <i>Visiting Student</i>	
Developed and implemented an innovative vision system, integrating the YOLO v5s model with ROS (Robot Operating System), for real-time object detection within a distributed robot swarm.	
<ul style="list-style-type: none"><li>Curated a comprehensive object detection dataset by leveraging ROS in conjunction with cameras.</li><li>Conducted YOLOv5s model training with a custom dataset and deployed Triton Inference Servers with YOLO v5s model on each robot in the swarm.</li><li>Reduced latency by converting image preprocessing and ROS topic publishing Python code to C++. Implemented object detection for a swarm of robots, enhancing overall intelligence and coordination capabilities.</li></ul>	
<b>Real-time Slope Perception Module for UAV</b> <i>Westlake University, China</i>	<i>May 2023 – Jul 2023</i>
Researcher, <i>Visiting Student</i>	
Designed and implemented a cutting-edge perception module for unmanned aerial vehicles (UAVs) utilizing a combination of four laser distance sensors and an Inertial Measurement Unit (IMU).	
<ul style="list-style-type: none"><li>Developed a sophisticated slope perception algorithm tailored for real-time monitoring of inclined surfaces.</li><li>Developed a visually intuitive real-time interface to communicate with the microcontroller, facilitating the monitoring and analysis of slope data.</li><li>Integrated the slope perception algorithm seamlessly with the sensor module using Keil, enabling UAVs to perceive and navigate inclined terrains in real-time.</li></ul>	
<b>Verification Analysis of FedAvg in Non-IID dataset</b> <i>Xi'an Jiaotong-Liverpool University, China</i>	<i>Jun 2022 - Sep 2022</i>
Undergraduate Researcher, <i>Summer Undergraduate Research Fellowship</i>	
Conducted experiments and evaluations on the Federated Averaging (FedAvg) algorithm using the MNIST dataset to compare the performance of various methods in handling non-identically distributed data.	
<ul style="list-style-type: none"><li>Implemented and executed experiments applying FedAvg algorithm to assess its efficacy in federated learning scenarios, specifically focusing on non-IID data distributions.</li><li>Analyzed and compared the performance of FedAvg with different approaches, shedding light on its convergence for scenarios involving non-identically distributed dataset in the context of MNIST digit recognition.</li></ul>	

## Projects

<b>UART Serial Communication Implemented in Verilog HDL on FPGA</b> <i>Digital System Design</i>	<i>Oct 2023 – Nov 2023</i>
Developed and implemented a versatile UART communication module in Verilog, seamlessly integrating transmitter and receiver functionalities on an Altera FPGA board for establishing reliable bidirectional communication with a computer.	
<ul style="list-style-type: none"><li>Crafted dedicated transmit and receive modules for UART serial communication, incorporating essential components such as shift registers, baud rate generators, and controllers to facilitate efficient data transmission and reception.</li><li>Utilized ModelSim to meticulously simulate and analyze each module, ensuring optimal stability, robustness, and portability of the transmission and reception processes.</li></ul>	
<b>Image Processing for Object Recognition</b> <i>Year 2 Project</i>	<i>Sep 2022 - May 2023</i>
Developed and implemented an autonomous visual tracking system on a small car using Jetson Nano as the main processing unit, integrating computer vision, deep learning and automatic control technologies.	
<ul style="list-style-type: none"><li>Developed a small car equipped with a camera for perception capabilities and generated a runway dataset through camera-based trials.</li><li>Conducted training sessions for the ResNet model using the custom dataset, enabling the small car to make informed decisions for autonomous navigation and path following based on visual inputs.</li><li>Implemented a PID controller as the motor control module to ensure precise and responsive adjustments, facilitating stable and accurate movements in accordance with the visual feedback.</li></ul>	