Experiment 5 – Design of an Operational Amplifier Using Multisim

Abstract

This experiment explores the basic principles of operational amplifiers and their characteristics. We designed an operational amplifier based on Multisim software. The designed circuit consists of four stages: differential amplifier, emitter follower, common emitter, and emitter follower. The experiments focused on the basic information of the amplifier circuit through transient simulations, DC transfer characteristic simulations with probes. The frequency response of the amplifier was then obtained from the gain and phase Bode plots of the amplifier. In addition, the response of this amplifier to a common mode signal is also investigated.

Declaration

I confirm that I have read and understood the University's definitions of plagiarism and collusion from the Code of Practice on Assessment. I confirm that I have neither committed plagiarism in the completion of this work nor have I colluded with any other party in the preparation and production of this work. The work presented here is my own and in my own words except where I have clearly indicated and acknowledged that I have quoted or used figures from published or unpublished sources (including the web). I understand the consequences of engaging in plagiarism and collusion as described in the Code of Practice on Assessment.

Contents

1 Introduction

1.1 Objectives

The objective of this experiment is to design an operational amplifier using Multisim software. At the end of the experiment, it was possible to gain a deeper understanding of operational amplifiers. Meanwhile, to be able to combine different stages to produce an effective operational amplifier circuit. In addition, to be aware of the main challenges and issues in designing an operational amplifier to meet operational amplifier design specifications.

a) Differential input impedance greater than 100 kΩ.
b) Voltage gain (that is, 'open loop gain') greater than 500,000.
c) Output impedance less than 1 kΩ.
d) Output voltage to be approximately zero volts for zero input.
e) Frequency response down to dc (0 Hz).
f) Supply voltage ± 9 V.
g) Total current consumption not greater than 5 mA.

Fig.1. Operational amplifier design specifications [1]

1.2 Theoretical Background

Operational amplifiers were originally intended to perform mathematical calculations such as addition, subtraction, multiplication, division, and function operations. In current technological conditions, the mathematical operation function of operational amplifiers is no longer prominent and is now mainly used in signal amplification and active filter design [2]. In most conventional designs, we use the ideal model of an op-amp and ignore its internal structure. Think of it as an 'amplifying component' that can be connected to a power supply and made to work as an amplifier. An ideal op-amp has an infinite input impedance and zero output impedance. Common amplification circuits include the following: non-inverting amplification circuits, inverting amplification circuits, adders, differential amplification circuits, etc. Its circuit symbol

is shown in Figure 2.

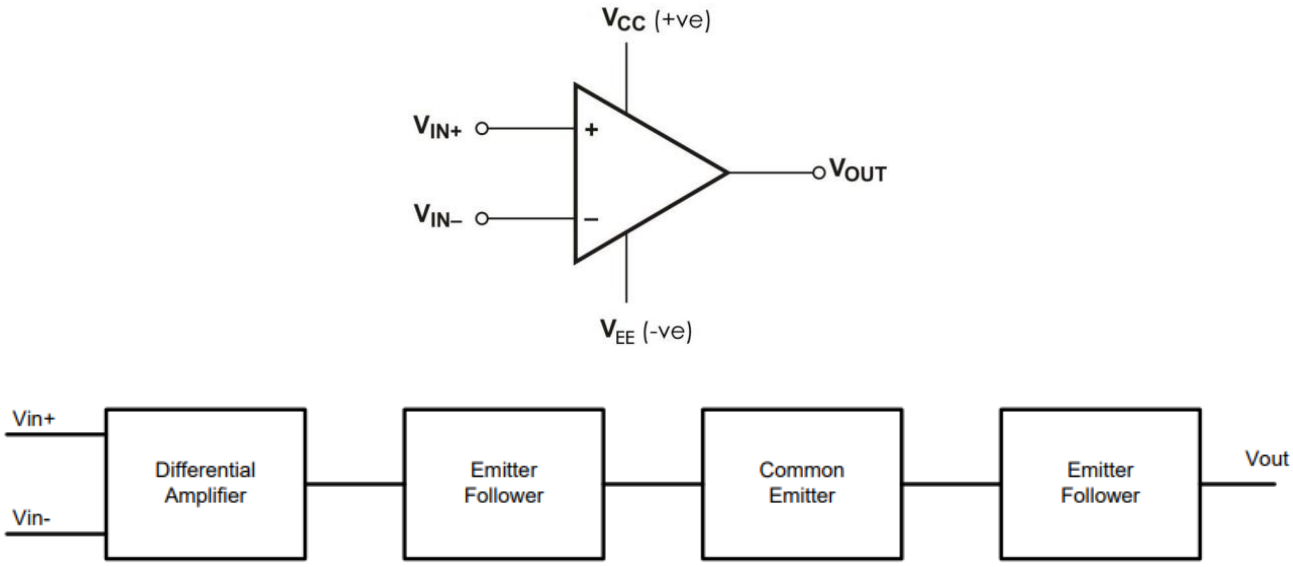


Fig.2. Op-amp symbol and block diagram [1]

2 Materials and Methods/Procedure

2.1 Materials

Because this experiment is a 'simulation', all operations are performed on a computer using Multisim circuit simulation software. Therefore, the only actual material for it is the Multisim software. However, many electronic components were used in the process of using the software, such as PN2222 transistors, PN2907 transistors, several different types of resistors and power supplies.

- BJT (NPN): PN2222
- BJT (PNP): PN2907
- Power supply (AC and DC)
- Resistors (Calculation required)
- NI Multisim 14.3 (all work is based on this software)

3 Results and Analysis

3.1 Part I: Transistor output characteristics

- Task 1: Designing circuit diagrams

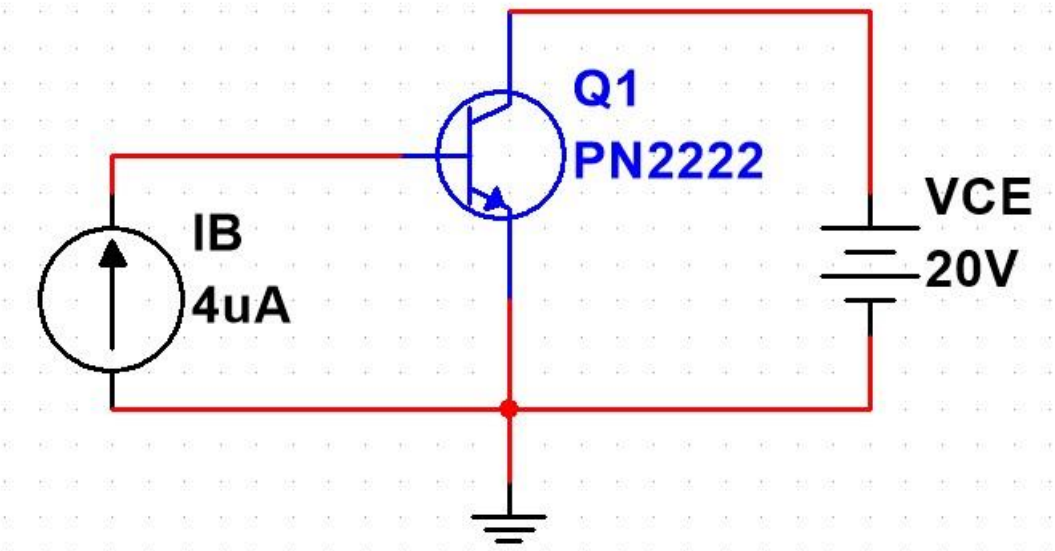


Fig.3. Circuit for PN2222

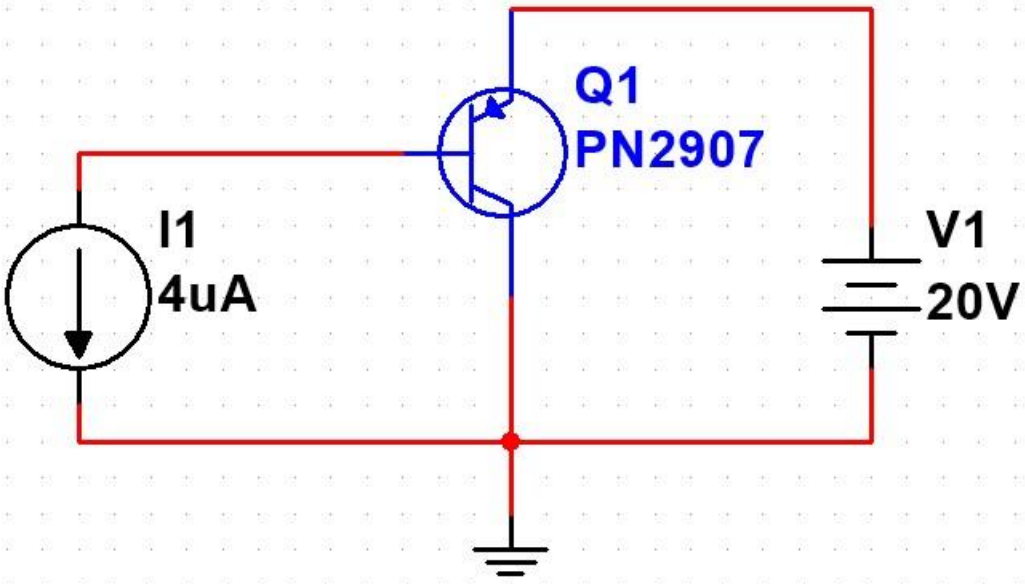


Fig.4. Circuit for PN2907

- **Task 2 & Task 3: Circuit simulation results**

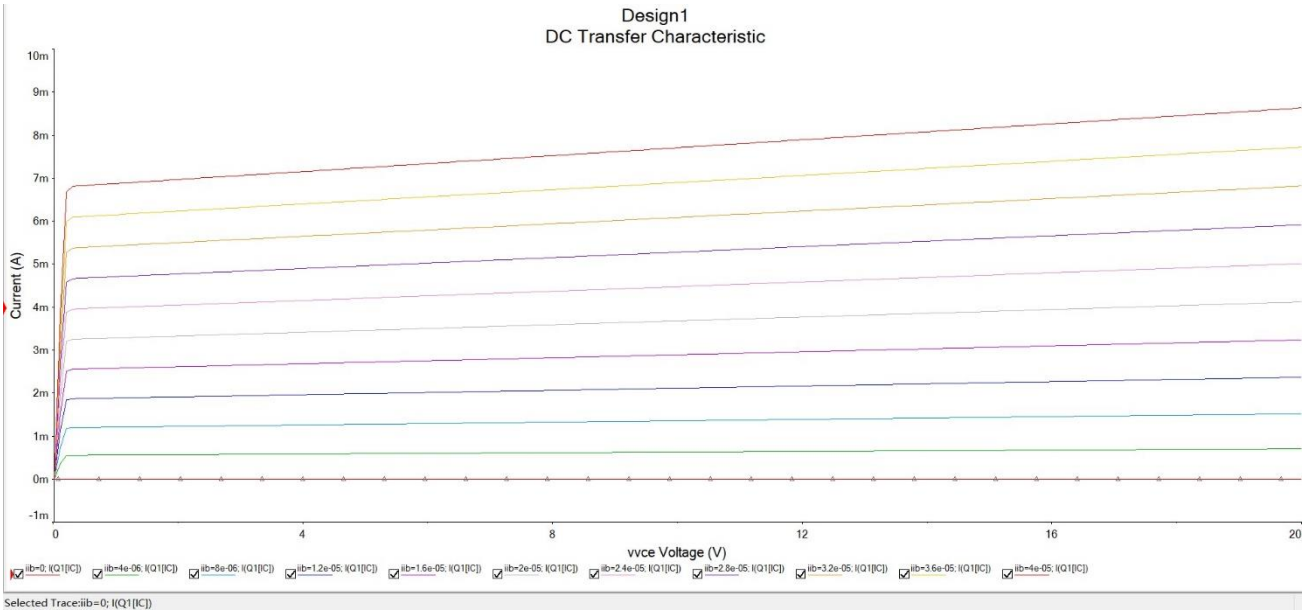


Fig.5. DC Transfer Characteristic for PN2222

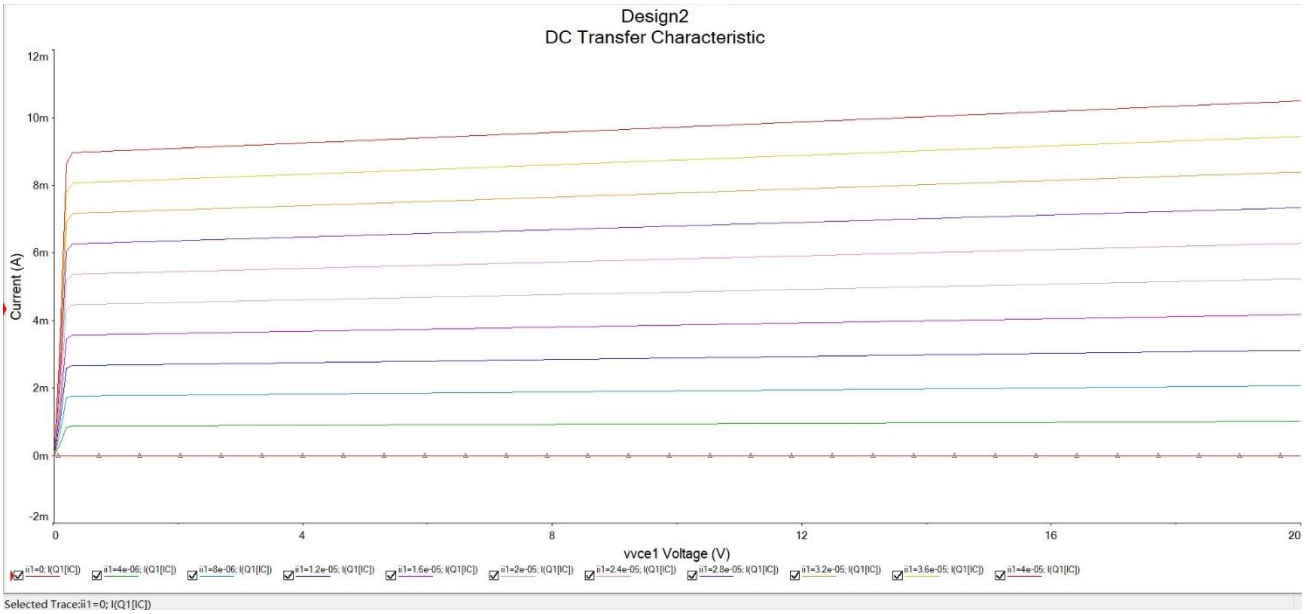


Fig.6. DC Transfer Characteristic for PN2907

- **Task 4: Calculation of current gain**

PN2222:

First, we can estimate the DC current gain β for Ic at 2mA by looking at the graph above. the formula for the DC current gain is as follows:

$$\beta = \frac{I_C}{I_B} = \frac{2mA}{12\mu A} \approx 166.67$$

The AC current gain (small signal) can also be obtained by the following equation as follows:

$$\beta_0 = \frac{\Delta I_C}{\Delta I_B} \approx \frac{2mA - 1.35mA}{12\mu A - 8\mu A} = 162.5$$

PN2907:

As with the above calculation, we can obtain its DC current gain versus AC (small signal) current gain by the following equation:

DC:

$$\beta = \frac{I_C}{I_B} = \frac{2mA}{8\mu A} = 250$$

AC:

$$\beta_0 = \frac{\Delta I_C}{\Delta I_B} \approx \frac{2.90mA - 1.95mA}{12\mu A - 8\mu A} = 237.5$$

As the accuracy of the images is not very high, only the results obtained by estimation can be used to calculate the current gain for DC and AC. Therefore, the current gain values calculated from the estimated values are still estimates and are not perfect.

3.2 Part II: Achieving the specification of the operational amplifier

- **Task 1: Build a complete amplifier**

The construction of a complete operational amplifier circuit requires the calculation of all four resistors, as follows:

The calculation of R_2

Input resistance:

$$R_{id} = \frac{V_{id}}{i_i} = 2r_{be} = \frac{2\beta_0}{g_m} = \frac{2\beta_0}{40I_C}$$

Hence, the current in amplifier is:

$$I_0 = 2I_C = \frac{2 \times 2 \times \beta_0}{40R_{id}}$$

Since the PN2907 has a maximum forward beta value of approximately 232 and assumes an input resistance of 120k ohms. We can obtain:

$$I_0 = \frac{2 \times 2 \times 232}{40 \times 120000} = 0.1933mA$$

For the application of Widlar current mirror:

$$I_{ref} = I_0 \times e^{\frac{I_0 \times R_2}{V_T}}$$

Hence:

$$R_2 = \frac{V_T}{I_0} \times \ln 10$$

We know that V_T is about 25mA and I_0 is about 0.1933, so we get:

$$R_2 = \frac{25}{0.1933} \times \ln 10 \approx 297.799$$

The calculation of R_1

By Ohm's law we can easily obtain:

$$R_1 = \frac{V_{CC} - V_{EE} - 0.6}{I_{ref}}$$

We have $V_{CC} = 9$, $V_{EE} = -9$, $I_{ref} = 0.1933$ mA, brought in to give:

$$R_1 = \frac{9 - (-9) - 0.6}{1.933} = 9.00016\ k\Omega$$

The calculation of R_4

The output resistance of a differential amplifier can be shown by the following equation:

$$R_{ce2} = \frac{V_{APNP}}{I_{C1}}, \quad R_{ce4} = \frac{V_{ANPN}}{I_{C1}}, \quad R_O = R_{ce2} // R_{ce4}$$

First, we know that the forward early voltage of transistor PN2907 is 115.7. The forward early voltage of transistor PN2222 is 74.03. In addition, the current Ic is

equal to 0.5Io, which is approximately 0.0967mA. Taking this into the equation gives:

$$R_O = 1196.484//765.564 = 466.852\ k\Omega$$

We know that the input impedance of an emitter follower is approximately 10 times the output impedance of a differential amplifier, thus:

$$R_{in}^{EF} \approx 10 \times R_O = 4668.52\ k\Omega$$

For the input impedance of the coupling stage:

$$R_i = R_{be} + (1 + \beta_0) \times R_4//R_L$$

Since

$$R_{be} = \frac{\beta_0}{40I_C}$$

Then

$$R_{be} = \frac{\beta_0 \times R_4}{40V_{be}} = \frac{256 \times R_4}{40 \times 0.6}$$

We can calculate R_L from the following equation:

$$R_L = \frac{256}{40 \times 1.933} = 3.311\ k\Omega$$

At this point, we have only one unknown, R4, which is obtained by solving the equation:

$$4668.52 = \frac{256 \times R_4}{40 \times 0.6} + (1 + 256) \times R_4//3.311$$

$$\text{R4} \approx 258.629\ \text{k}\Omega$$

The calculation of R_3

We assume that the output resistance of the op-amp is 800Ω:

$$R_O = \frac{R_{be} + R_{CE}}{1 + \beta_0}//R_3 = 800\ \Omega$$

R_{CE} is the output resistor of the CE stage, thus:

$$R_{CE} = r_{ce8}//r_{ce9} = \frac{V_{APNP}}{I_C}//\frac{V_{ANPN}}{I_C}$$

Where $I_C = 1.933$ mA $V_{PNP} = 74.03$ V and $V_{NPN} = 115.7$ V

$$R_{CE} = 23.349\ \text{k}\Omega$$

$$I_C = \frac{0 - V_{EE}}{R_3} = \frac{9}{R_3}$$

$$R_{be} = \frac{\beta_0}{40I_C} = \frac{256}{40I_C}$$

Since then, we have only one unknown quantity and solving the equation gives R_3:

$$R_O = \frac{R_{be} + R_{CE}}{1 + \beta_0} // R_3 = 800\ \Omega$$

$$R_3 = 256.41\ \text{k}\Omega$$

At this point, we can build the complete op-amp circuit as shown below:

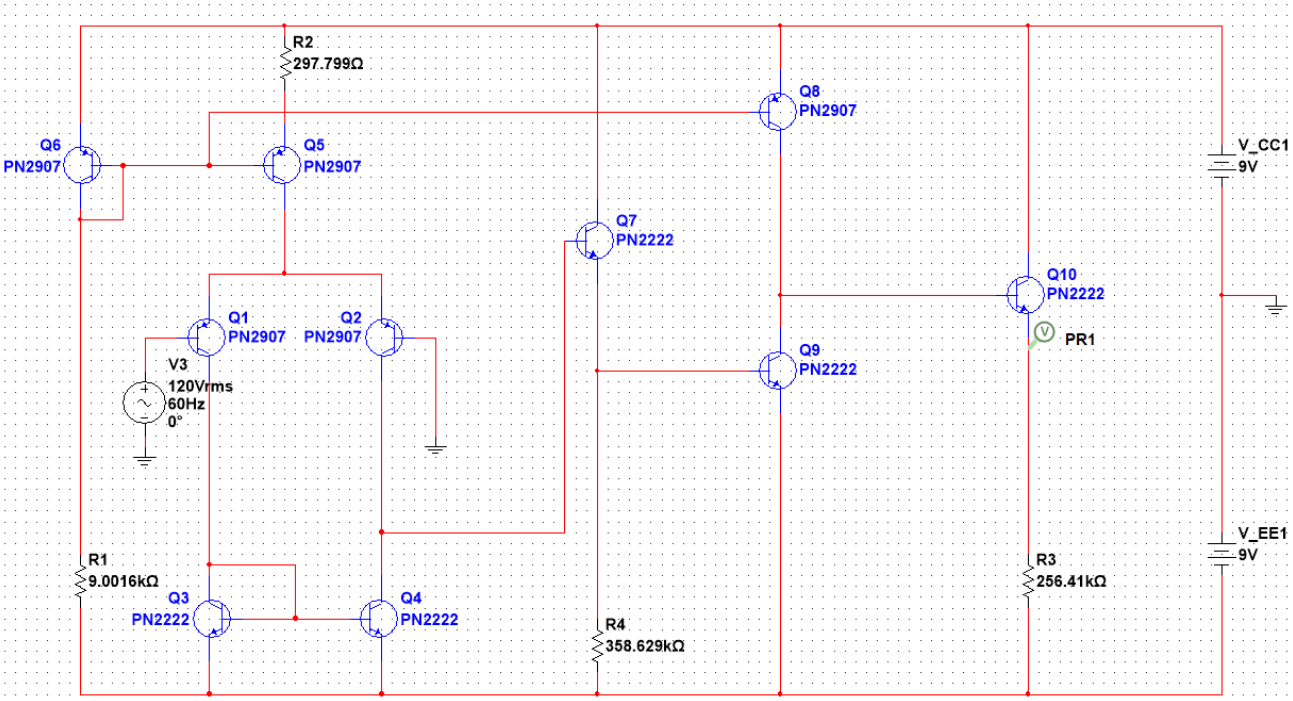


Fig.7. Complete operational amplifier

- **Task 2 Transfer characteristics of the amplifier**

  First, we perform a DC sweep from -9 to 9. We can observe from Fig. 8 that more accurate values are obtained around a voltage of 0. Therefore, by narrowing the range we obtain Fig. 9.

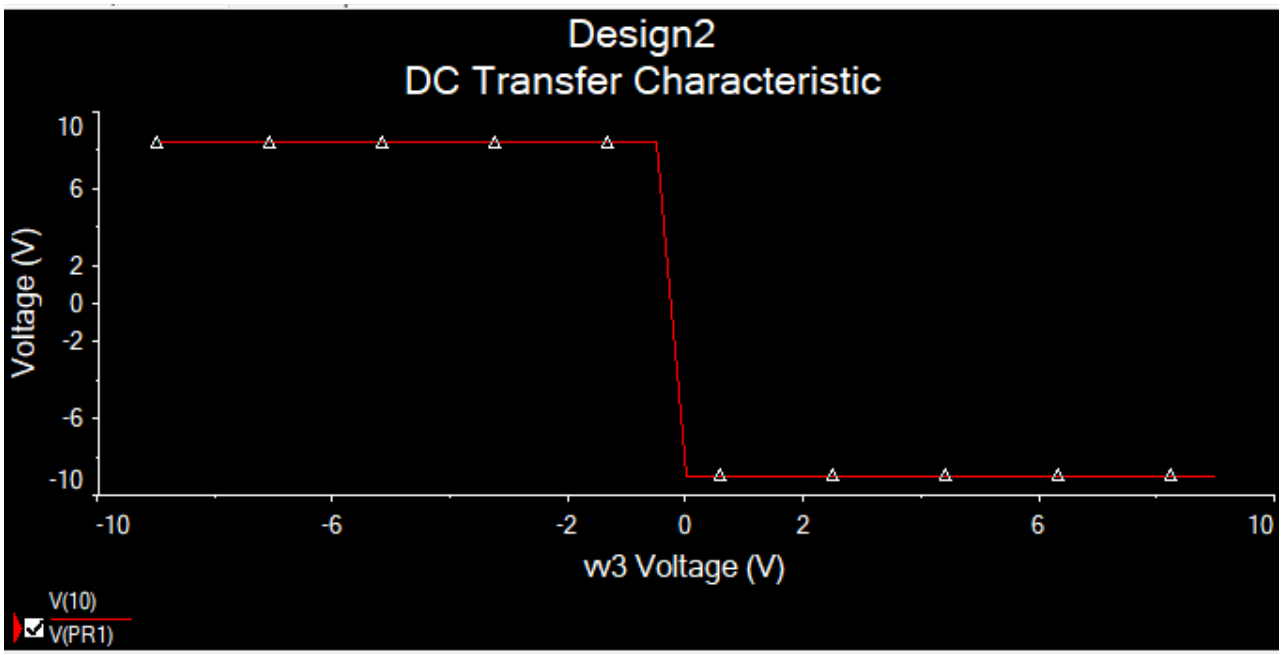


Fig.8. DC Transfer Characteristic (-9 ~ 9)

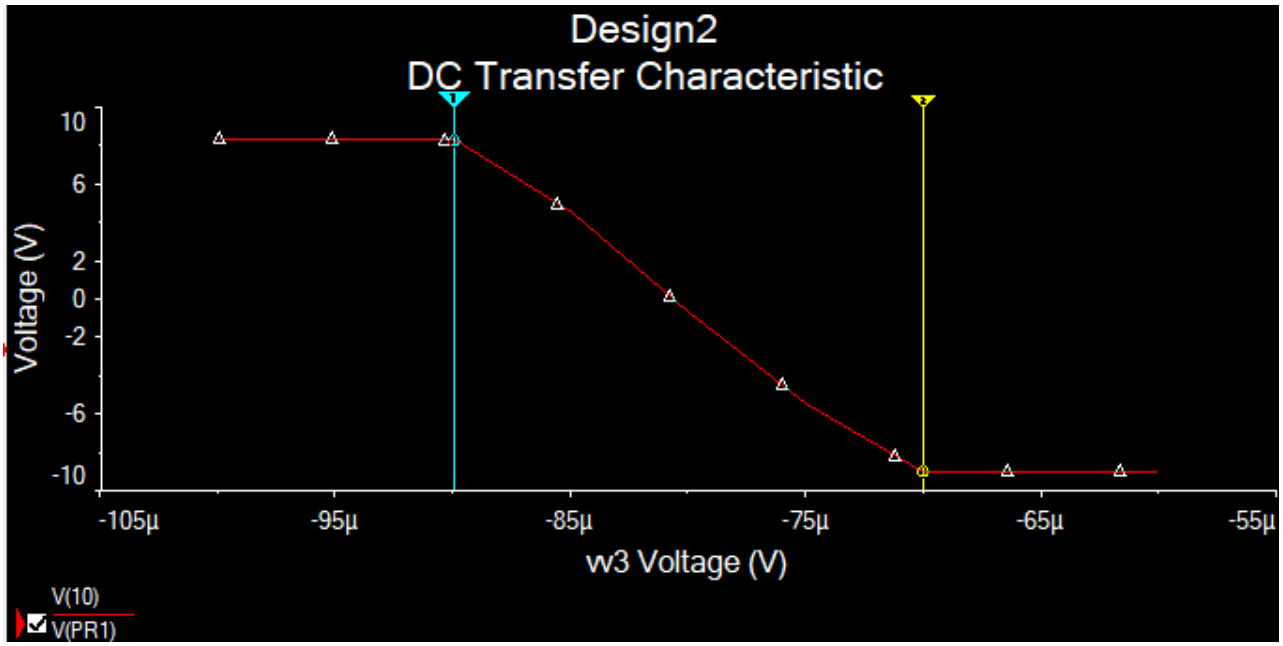


Fig.9. DC Transfer Characteristic (-105uV ~ -55uV)

At this point we can open more clearly to the DC transfer characteristics.

- **Task 3 Open loop gain (A_{ol})**

  Firstly, in the previous task, we knew the more precise scope. And we know the following parameters:

Cursor	
	V(10)
	V(PR1)
x1	-90.0216µ
y1	8.3194
x2	-69.9784µ
y2	-9.0000
dx	20.0431µ
dy	-17.3194
dy/dx	-864.1054k
1/dx	49.8925k

Fig.10. Paramenters

At this point, we can calculate its open-loop gain by using the following equation:

$$A_{ol} = \left|\frac{\Delta V_o}{\Delta V_i}\right| = \frac{8.319 + 9}{90.0216 - 69.9784} \times 10^6 = 855783.2945$$

At this point we find an open circuit gain of 855783.2945, which is greater than the experimental requirement of 500000.

- **Task 4 DC voltage offset**

As can be seen from the work already done, the DC transfer characteristic curve is shifted by a voltage offset. As the center of the transfer characteristic curve obtained in the previous circuit does not correspond to the horizontal coordinate 0, a DC offset needs to be set to shift the curve to the right. The value of the DC offset can be determined from the horizontal coordinate of the center of the amplification range curve. The circuit diagram, together with the coordinates, is shown below:

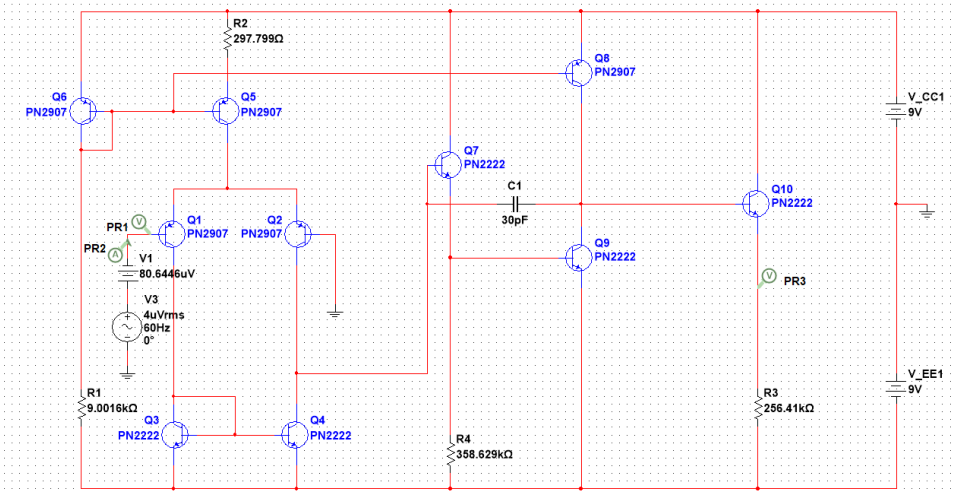


Fig.11. Circuit with DC offset

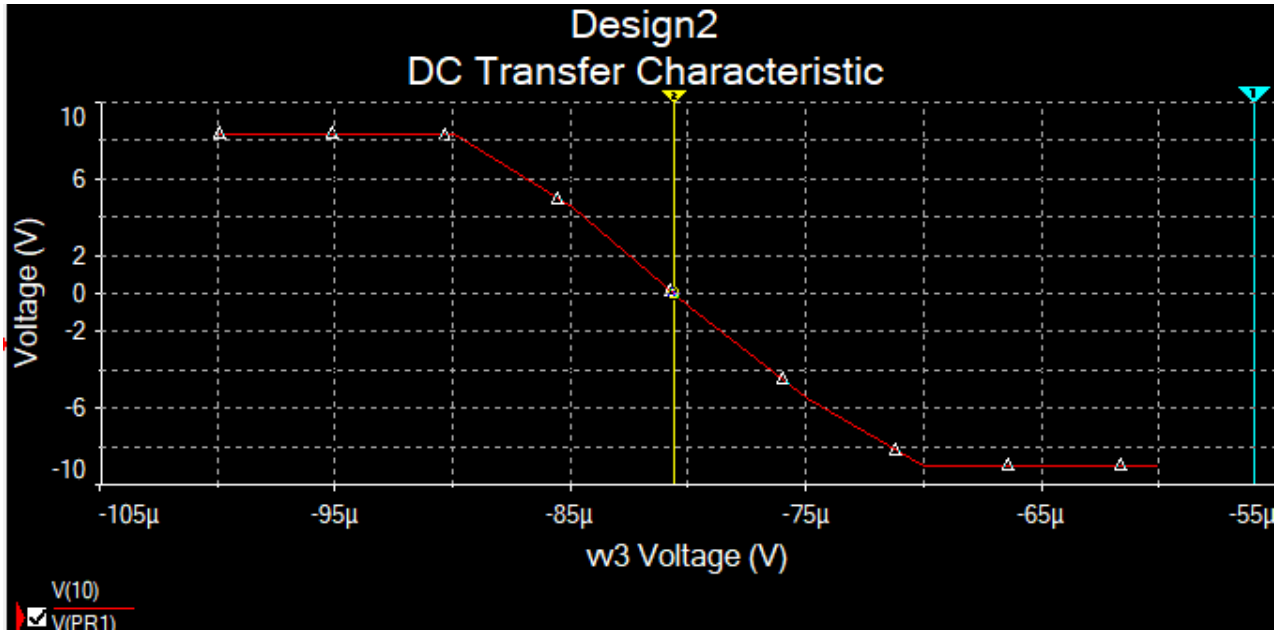


Fig.12. DC Transfer

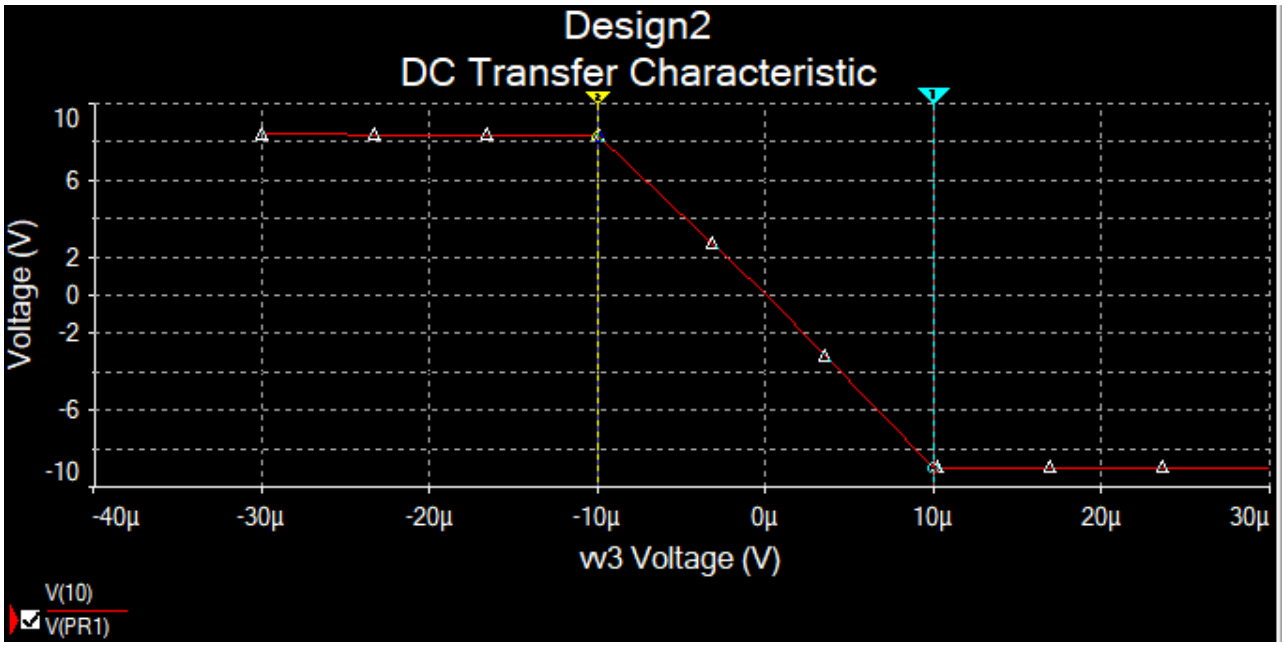


Fig.13. DC Transfer with offset

From the parameters of the coordinates, we know that we need to set a DC offset of 80.6446uV to move the curve.

- **Task 5 Transient simulation and gain**

First we know the relationship between the maximum value of the waveform and the RMS value, from which we can obtain the RMS value as follows:

$$V_{RMS} = \frac{9.9989}{\sqrt{2}} = 7.07\ \mu V$$

We then chose 4 uV to be used as the experiment. Furthermore, we know that the maximum value of V_{out} is here 5.8894V

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{5.8894}{4 \times \sqrt{2}} \times 10^6 = 1041108.669$$

We can see that the above result meets the requirement that the voltage gain should be greater than 500000. The circuit and waveform diagram is then as follows:

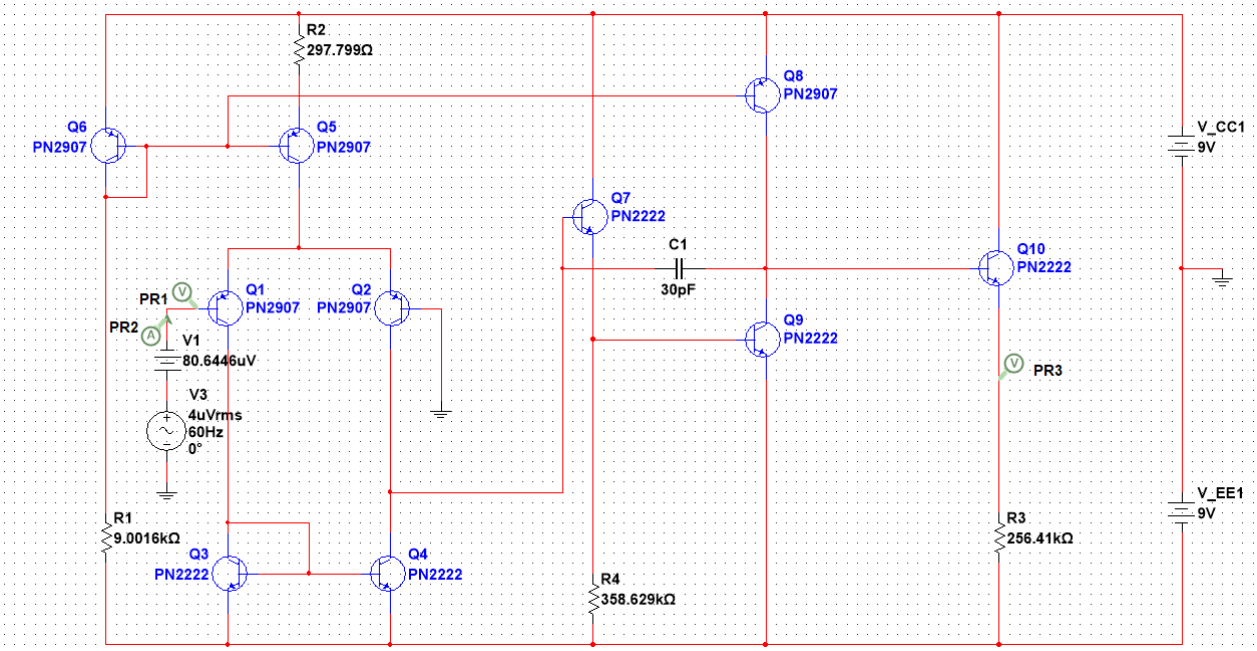


Fig.14. Circuit

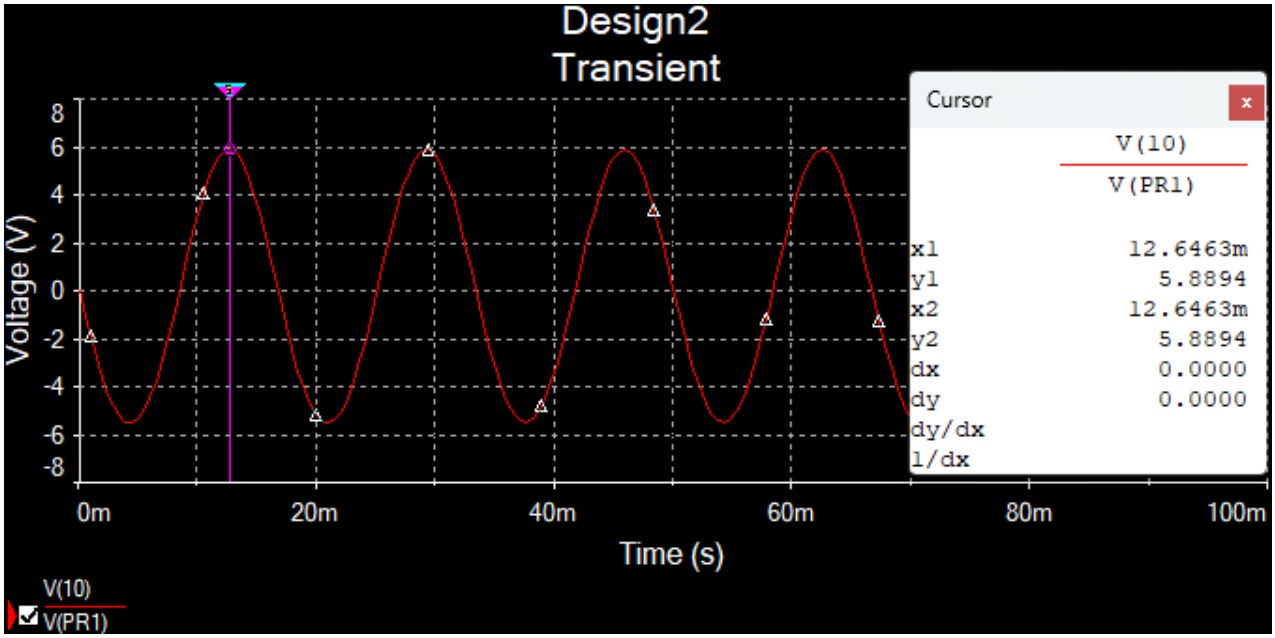
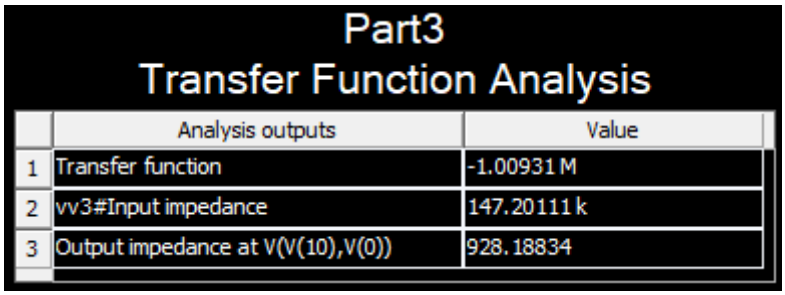


Fig.15. Waveform of Transient

- **Task 6 Transfer function simulation and comparison**

The results of the transfer function simulation are as follows:



	Analysis outputs	Value
1	Transfer function	-1.00931 M
2	vv3#Input impedance	147.20111 k
3	Output impedance at V(V(10),V(0))	928.18834

Fig.16. Transfer simulation

For voltage gain, we can see that the voltage gain is 1009310, which is relatively close to the result we obtained. In addition, this result is exactly in line with the experimental requirement of greater than 500000 gain.

For the input impedance, the experimental requirement is greater than 100 kΩ, and we can see that the simulation results are also fully consistent with the experimental requirements.

For the output impedance, the experimental requirement is less than 1 kΩ, and we

can see that the simulation results are also fully consistent with the experimental requirement. We have assumed an output impedance of 800 Ω, which is also within a reasonable range.

- **Task 7 Interactive simulation**

  By placing voltage, current and power probes, we obtain the following circuit diagram:

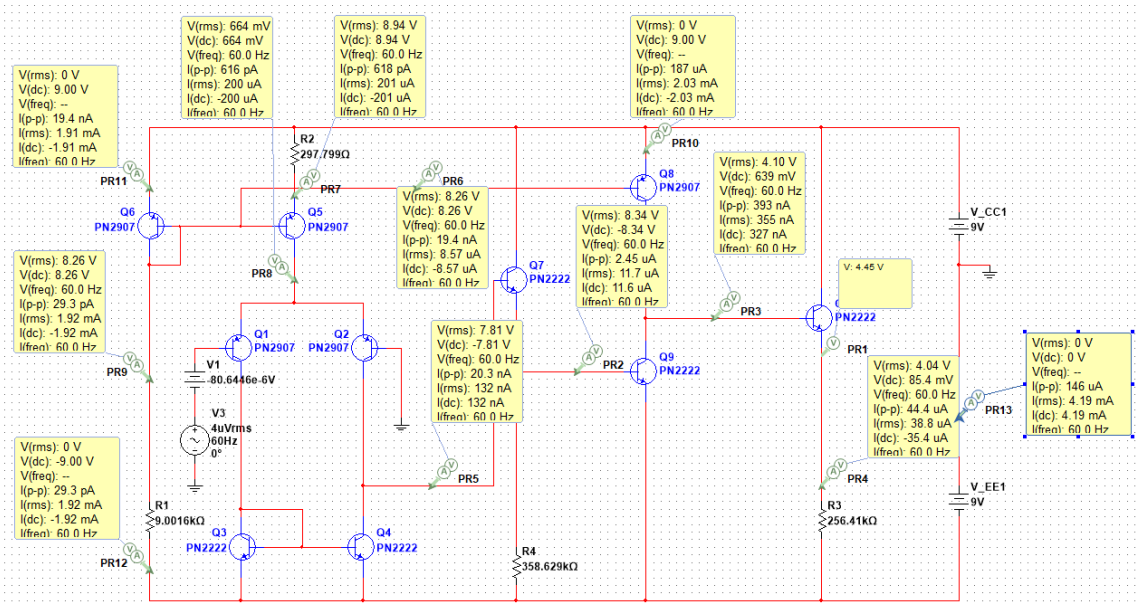


Fig.17. Schematic diagram with voltage probe

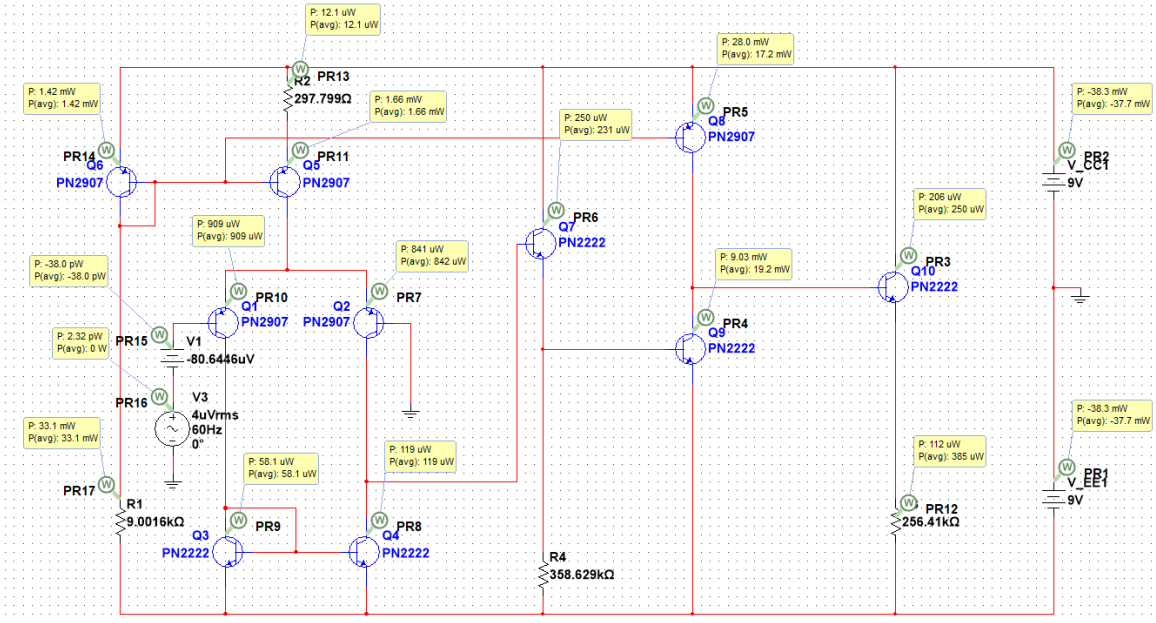


Fig.18. Schematic diagram with power probe

After looking at the circuit diagram with the voltage-current as well as the power probe, we find that the output voltage has an RMS value of 4.04 V when the input voltage has an RMS value of 4 uV. Thus, the voltage gain of the circuit can be calculated. It has a voltage gain of 1010000, which is in accordance with the results obtained previously.

3.3 Part III: Obtaining the frequency response of the designed amplifier

- **Task 1 Frequency response**

We obtained the frequency response of the amplifier by AC sweep simulation as follows:

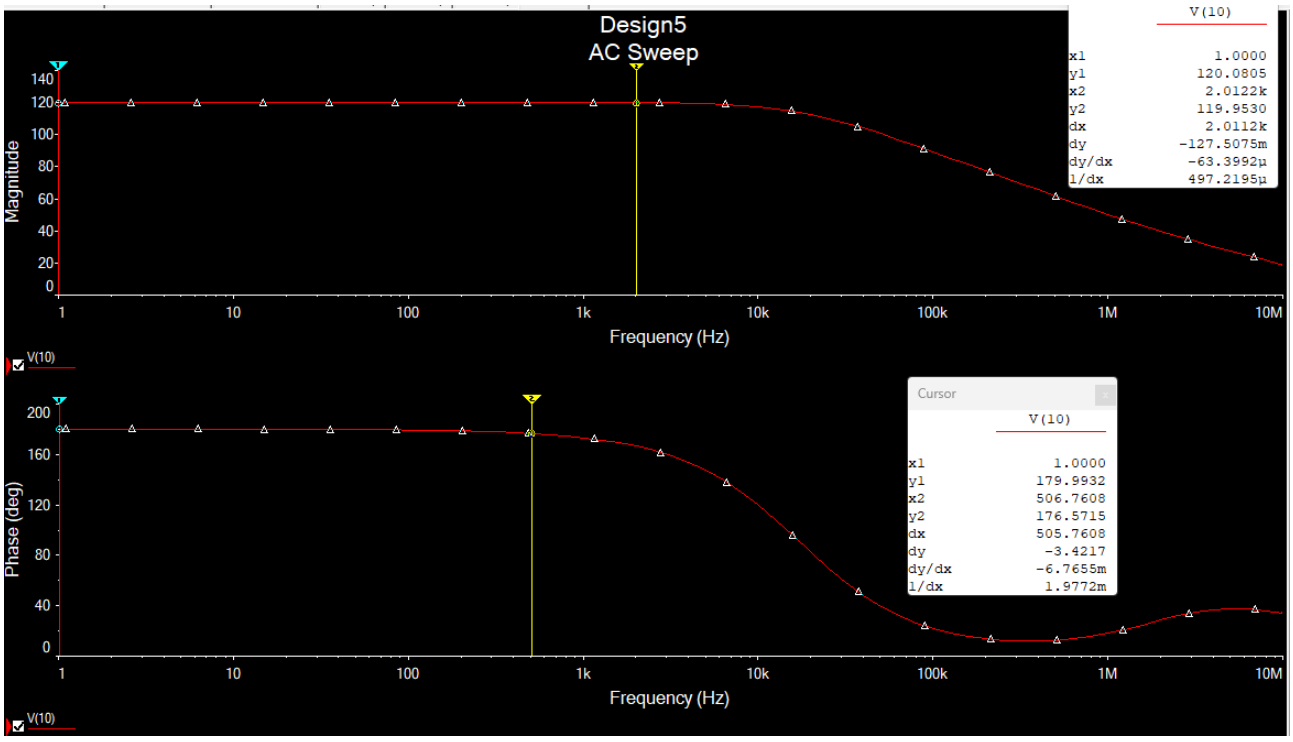


Fig.19. AC Sweep and Frequency response

As can be seen from the AC sweep plots, the amplitude of the bode plot remains 120 dB over the frequency range 1-10 kHz. after 10 kHz the amplitude decreases with increasing frequency. Thus, from the first amplitude plot, a bandwidth of approximately 13 kHz can be derived.

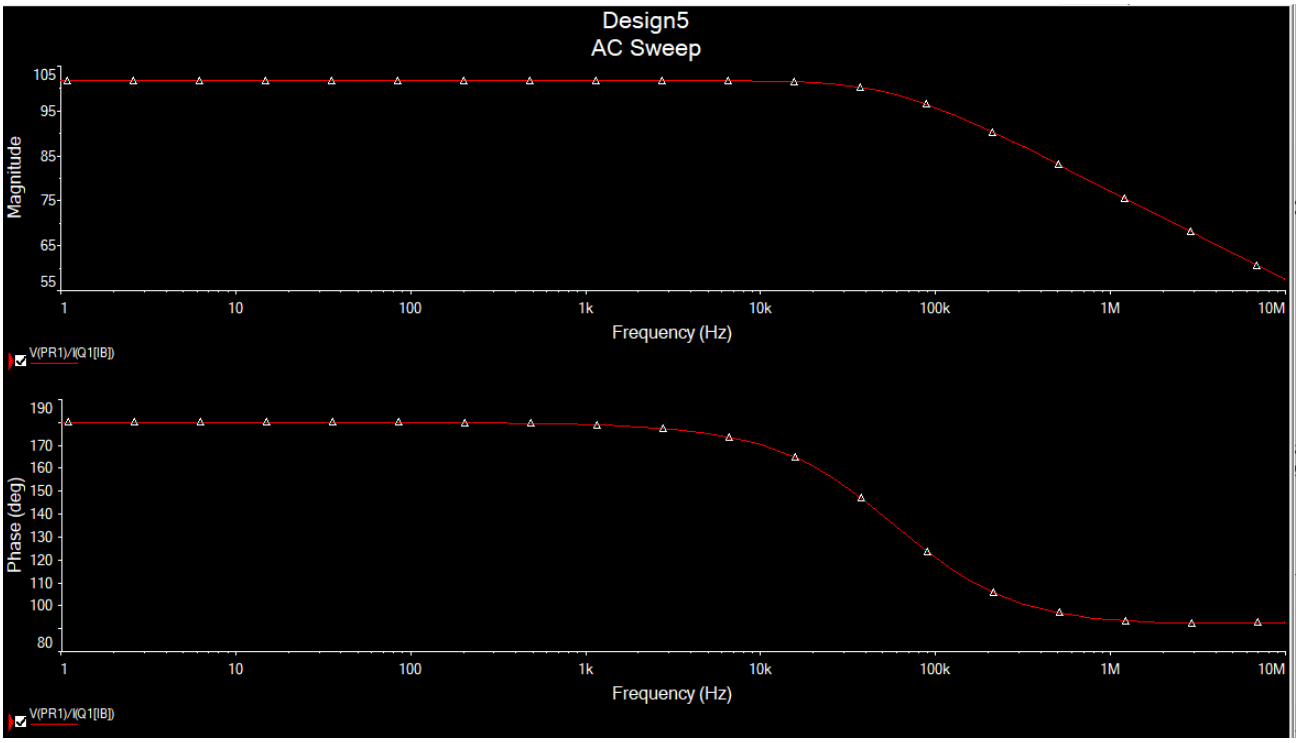


Fig.20. AC Sweep and Frequency response of input impedance

We can see from the graph above that the amplitude stays at around 102dB when the frequency range is 1-10kHZ. When the frequency is 10kHZ-10MHZ the value of the amplitude gradually decreases.

- **Task 2 Frequency response with phase compensating capacitor**

  With the addition of the phase compensating capacitor, we get the following circuit diagram:

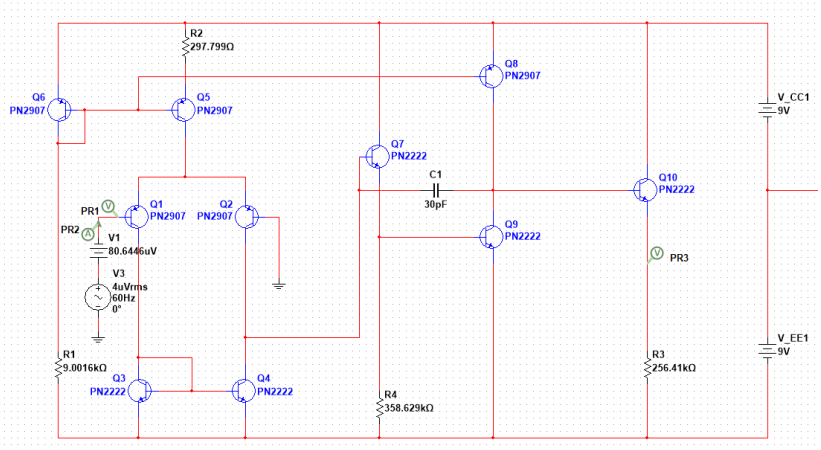


Fig.21. Circuit with phase compensating capacitor

Similarly, we can also obtain its frequency response:

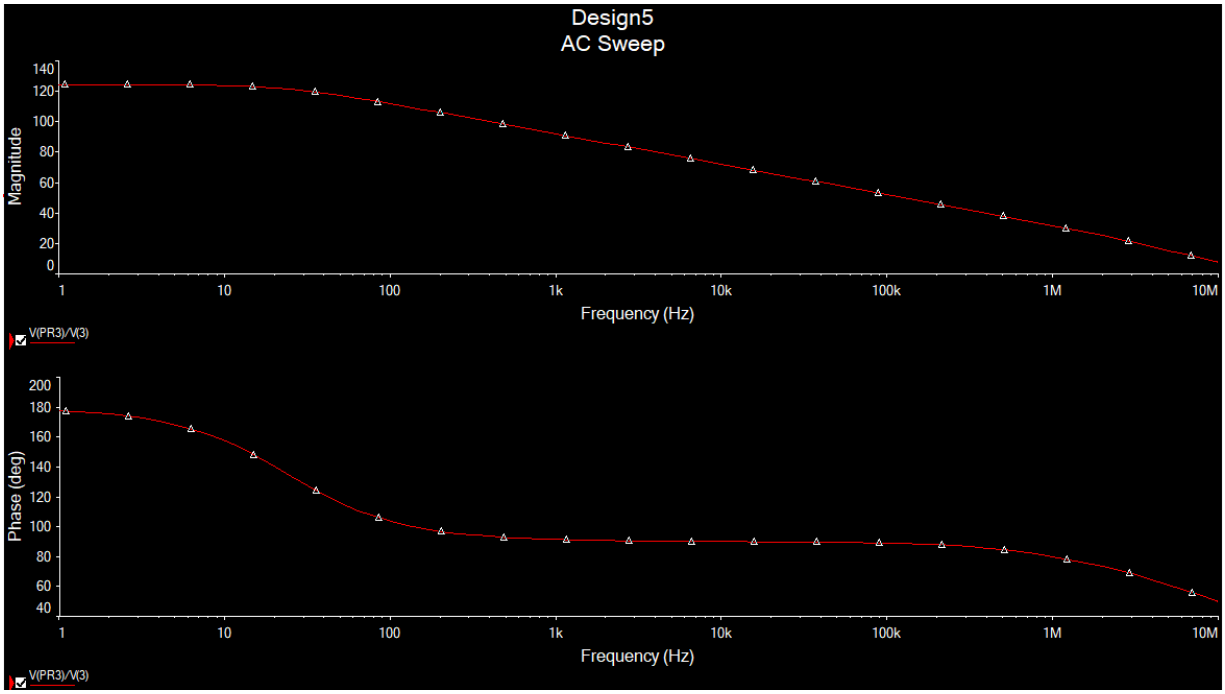


Fig.22. Frequency response with phase compensating capacitor

We can observe from the above graph that the amplitude remains at 120 dB for frequencies from 1 to 10 Hz. The magnitude gradually decreases as the frequency becomes greater than 10 Hz. At a frequency of 10 MHz the magnitude is at its lowest, about 2 dB. by definition, the gain is reduced by -3 dB when f = fβ. Therefore, the bandwidth of the amplifier is approximately 10Hz in the presence of the compensation capacitor. In addition, the magnitude of the phase decreases in the frequency range 0-1KHz. In the frequency range of 1KHz-100KHz the phase remains at around 90 degrees. In the frequency range of 100KHz-10MHz the phase decreases with increasing frequency. We can therefore conclude that the circuit with the addition of the phase compensation capacitor has a stable phase over a larger frequency range, which means that the circuit can operate properly over a larger frequency range.

Similarly, we can obtain the frequency response of the impedance:

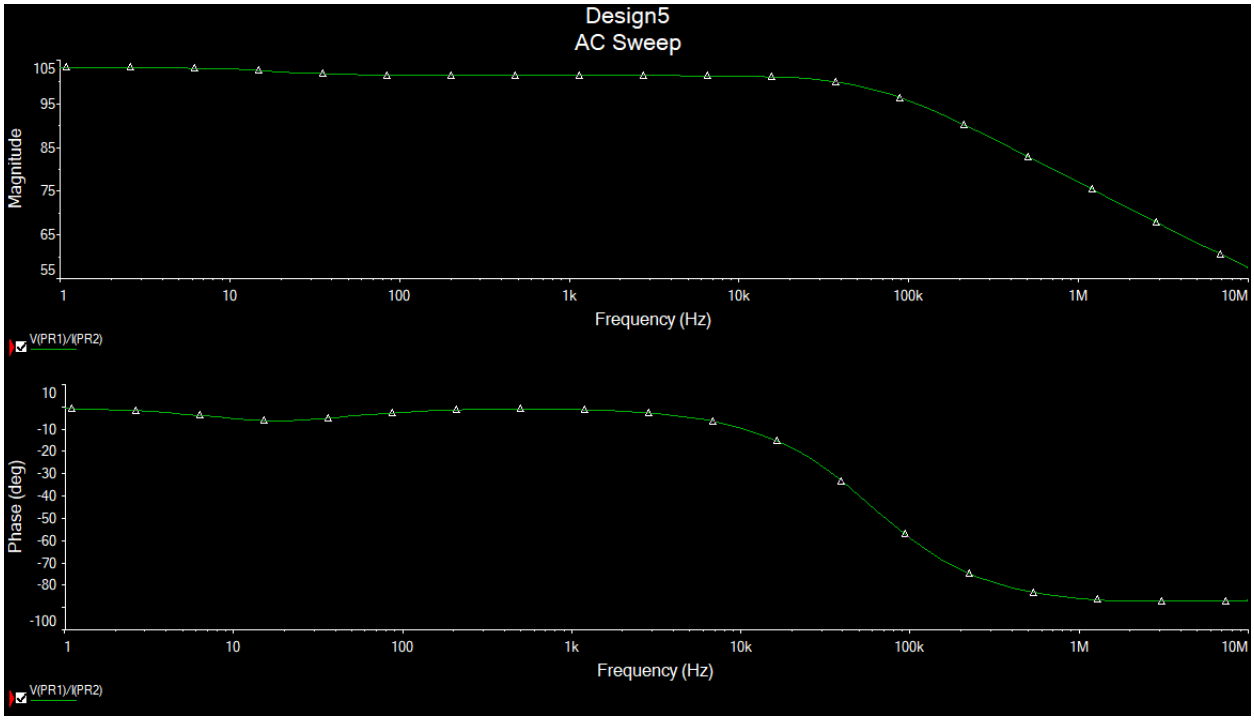


Fig.23. Frequency response of input impedance with phase compensating capacitor

We can observe that the magnitude also remains at around 103dB in the range of 1-100KHz. The magnitude gradually decreases when the frequency is in the range 100KHz-10MHz. These results are like those obtained in previous experiments without the use of capacitors. For phase, the phase remains essentially 180 degrees in the 1-10 KHz range. However, in the frequency range of 1-100Hz there is a slight drop in the phase value and then a rebound. In the frequency range 10K-1MHz the phase is decreasing. In the frequency range 1M-10MHz the phase stays at about 90 degrees.

3.4 Bonus Part: Response to common-mode signal

After replacing the input signal with a common mode signal, the circuit diagram of the new design is as follows:

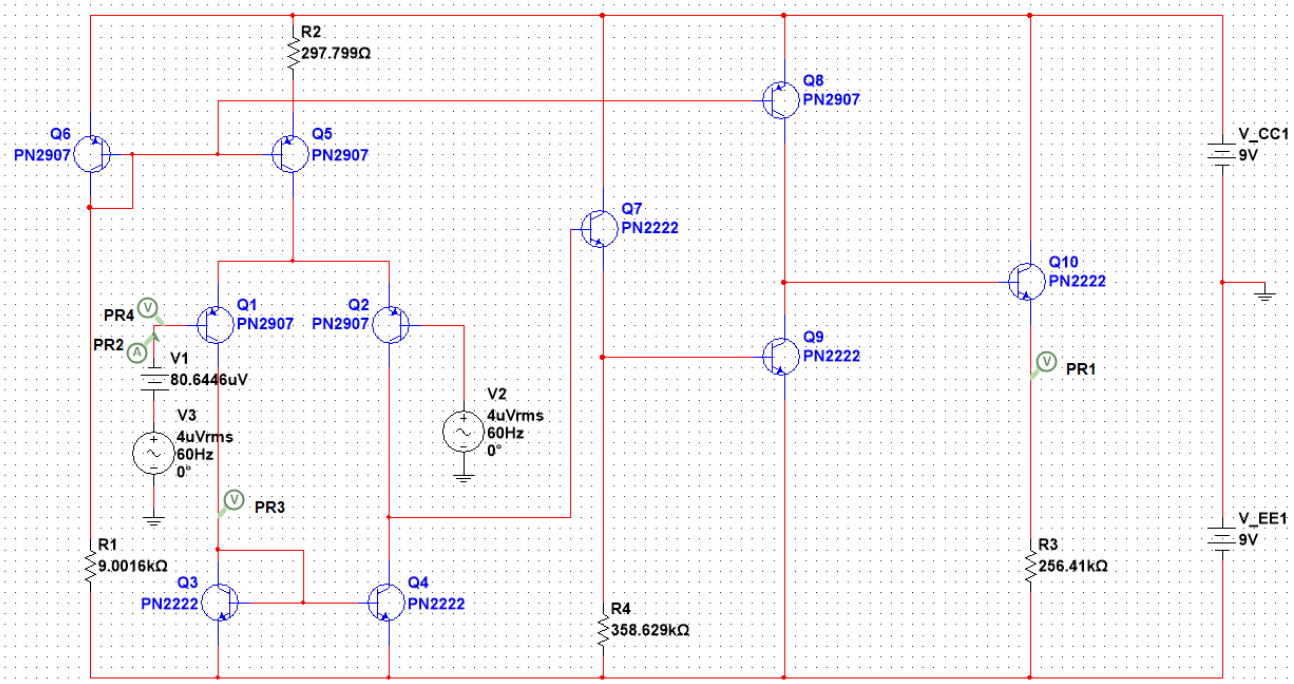


Fig.24. Circuit for common-mode signal

The frequency response of the common-mode signal as follow:

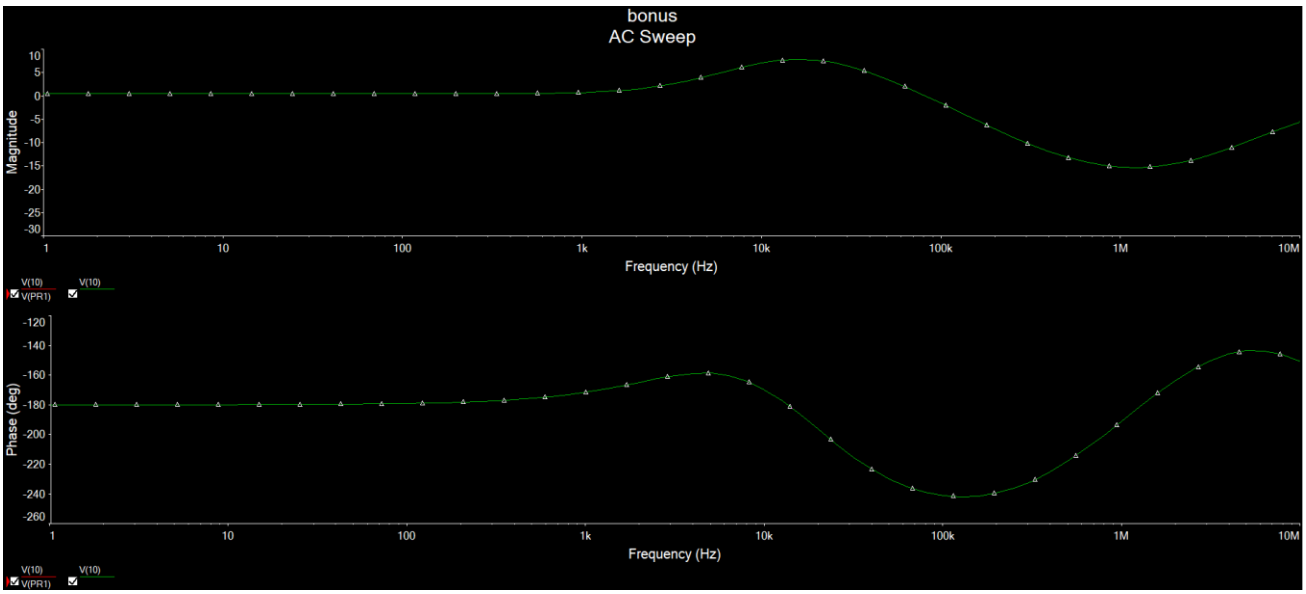


Fig.25. The frequency response to the common-mode signal

For the magnitude, the magnitude is approximately 0.529mdB in the frequency range 0-10KHz. in the frequency range 10K-10MHz there is a slight change in magnitude. However, the gain remains small in the frequency range 0-10MHz because the two common mode signals check each other. For the phase section, the phase value remains at around -180 degrees in the frequency range 0-1KHz. In the frequency range 1K-10KHz the phase shows a crest, but it is not significant. In the frequency range of 10K-10MHz the phase drops and then rises.

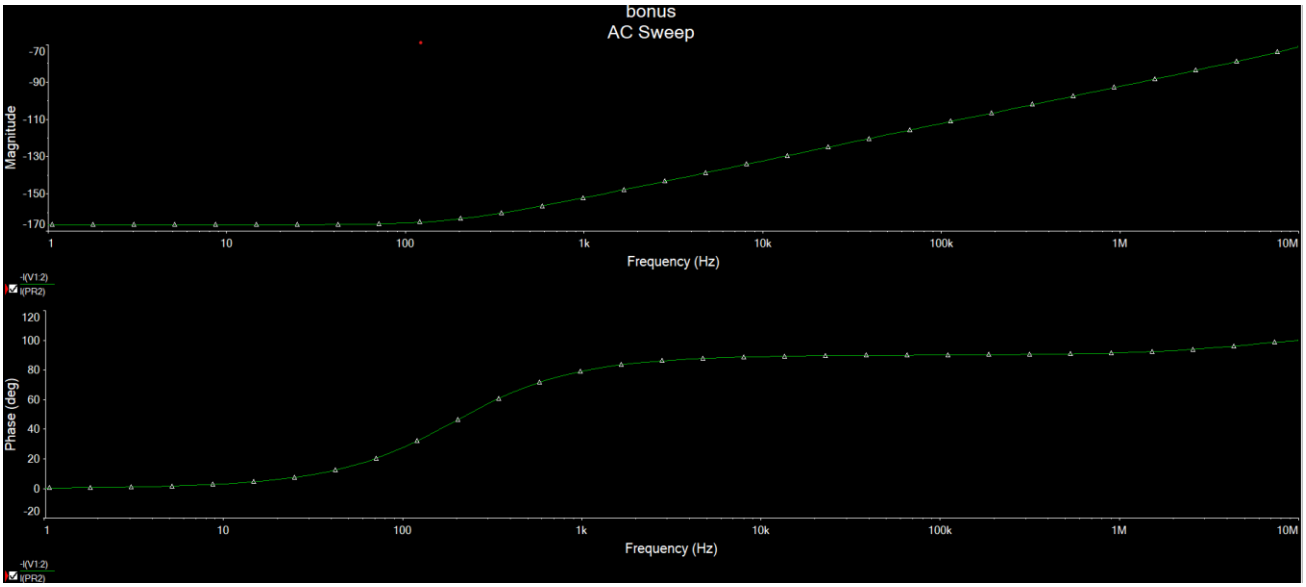


Fig.25. The frequency response of input impedance to the common-mode signal

For the magnitude, the magnitude is around 157 dB in the frequency range 1-10 KHz. in the frequency range 10 K-10 MHz, the magnitude gradually decreases. For the phase section, in the frequency range 1-1KHz, the phase value stays at around -180 degrees. In the frequency range 1K-10KHz, it gradually decreases to 90 degrees. In the frequency range 10K-10MHz the value stays at 90 degrees.

3.5 Design specifications table

Parameter	**Specification**	**My value**
Differential input impedance	$>$ 100 kΩ	147.2 kΩ
Voltage gain (open loop)	$>$ 500000	1009310
Output impedance	$<$ 1 kΩ	928.188 Ω
DC output voltage	= 0 V	80.6 mV
DC offset voltage	NULL	80.6 uV
Frequency response	Done to DC (0 Hz)	Maximum gain = 120 dB, f = 10 kHz
Total current consumption	$<$ 5 mA	4.19 mA
Bandwidth with compensation capacitor	NULL	= 10 Hz

Comments:

Differential input impedance: The input impedance assumed in the calculation of the required resistance value is 120 KΩ, whereas the actual value in the transfer function simulation is 147.2 KΩ. Since the required input impedance is very large the error between the actual and calculated value is within a reasonable range.

Voltage gain (open loop): In the transfer function simulation experiments, the open-loop voltage gain was approximately 101000. in task 3, the voltage gain calculated using the slope was approximately 855000. in task 5, the amplification was approximately 10400000 by measuring the amplified sine wave signal. the experimental requirement was for the open-loop gain to be greater than 500000, and the results obtained in all three cases

met the experimental requirements.

Output impedance: In the experiments, an output impedance of 800 Ω was assumed and used in the calculations. The transfer function simulation gives a result of 928.188 Ω. There is some error between the calculated and actual values, but both values meet the experimental requirement of less than 1 KΩ.

DC output voltage: We know that the circuit has an internal voltage offset because of this. Therefore, an additional DC offset voltage needs to be connected to the circuit and this is used to regulate and balance the output voltage to approximately 0V.

DC offset voltage: In the above experiments, the DC offset voltage obtained is approximately equal to 80.6uV, a value that can vary depending on the design of the circuit. In the second part, this value is calculated from the difference between the horizontal coordinates of the amplification center and the other parameters.

Frequency response: From this experiment we already know that at a frequency of 0Hz the gain is approximately equal to 120dB, and that this value remains constant after the addition of the phase compensation capacitor. It is only when the frequency is gradually increased above 100 kHz that the amplitude starts to decrease significantly.

Total current consumption: As can be seen from task 7 in part 2, the total current consumption is approximately 4.19 mA. this value meets the experimental requirement of less than 5 mA. this is designed to reduce power and increase efficiency.

Bandwidth with compensation capacitor: We know that the gain is reduced by -3dB when f=fβ and that the corner frequency fβ defines the bandwidth of the amplifier. The bandwidth of the amplifier with the addition of the phase compensation capacitor is

approximately 10 Hz.

4 General questions

- **What can you deduce about the stability of your amplifier from the Bode plots in Part III?**

  Ans: Firstly, the Bode plot is an effective way to determine the stability of a system. We know that calculating phase margin from Bode diagrams is a way to determine the stability of a system. When the phase margin is greater, the system is more stable. Therefore, we can estimate the stability of an amplification circuit by calculating the phase margin of the amplification circuit. We can use the following formula:

  PM = Φ - (- 180°) where Φ is the lag less than 0 [4].

  In the experimentally derived Bode plot, the frequency corresponding to this point when the gain is equal to 0 is approximately 11.81 mHz. 11.81 MHz corresponds to a phase of approximately 45 degrees. Similarly, we can obtain that the amplifier circuit without a phase compensation capacitor has a phase margin of only 20. Furthermore, we find that the phase margin of the system is positive. Therefore, the system is relatively stable. Furthermore, the amplifier circuit with phase compensation capacitors has a larger margin compared to the amplifier circuit without phase compensation capacitors, indicating that the system is more stable.

- **What is the purpose of the 'Phase compensating capacitor'?**

  Ans: In the AC scan simulation experiments we added a 30pF capacitor as a phase compensation capacitor between the collector of the common emitter stage and the

base of the first emitter follower. We know that the frequency range is too small when the compensation capacitor is not added. However, with the addition of the compensation capacitor, the phase stability range increases. Before the addition of the compensation capacitor, the phase was maintained in the frequency range of 1-1 KHz. With the addition of the phase compensation capacitor, the phase remains in the 100Hz-1MHz range and the bandwidth of the frequency response becomes larger. Therefore, the circuit before the addition of the compensation capacitor is not as stable as the circuit after the addition of the compensation capacitor. In summary, the purpose of adding a compensation capacitor is to make the entire amplifier circuit more stable.

5 Conclusions

The aim of this experiment was to design a complete operational amplifier and to design our own operational amplifier circuit based on the experimental requirements. First, we calculate the resistance of each resistor in the op-amp circuit. During the calculation we need to assume some values, if those values are within a reasonable range. After this has been done, we build an operational amplifier. In addition, the transmission characteristics of the circuit were found by means of a DC sweep and an AC sweep operation. In this section parameters such as open loop gain, dc voltage offset, frequency response and the effect of compensation capacitors are found. Overall, the experiment was relatively successful, with all parameters meeting the given specifications. This experiment has given us a deeper understanding of differential amplifiers.

6 References

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